PRELIMINARY DATA SHEET

Si82Fx Isolated Gate Driver with SelVCD™, Miller Clamp, and Low Channel-to-Channel Skew

The Si82Fx combines two isolated gate drivers into a single package for high-power applications. The Si82Fx includes devices with single or dual control inputs with independent or high-side/low-side outputs. These drivers can operate with a 3 V to 20 V input supply and a maximum gate driver supply voltage of 30 V. The inputs are CMOS, which provides robust noise margin.

The Si82Fx is ideal for driving power silicon MOSFETs, IGBTs, SiC FETs, and GaN FETs used in various switched power and motor control applications. These drivers utilize Skyworks' proprietary silicon isolation technology, supporting up to 6 kV_{RMS} for 1-minute isolation voltage. This technology enables high CMTI (200 kV/µs), lower propagation delays and skew, little variation with temperature and age, and tight part-to-part matching. The Si82Fx family offers longer service life and higher reliability than optocoupled gate drivers.

The output stage features Selectable Variable Current Drive (SelVCD™) technology that adjusts output current between eight selectable levels, eliminating the need for gate resistors and clamping any Miller effect currents. SelVCD™ operates as a current source that maintains current output within a tight tolerance of the target across all operating conditions. The driver family also offers features such as Undervoltage Lockout (UVLO), dead time programmability, and defined output states in all operating conditions.

Automotive Grade is available. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Applications

- Isolated switched-mode supplies
- Motor drives
- Power inverters
- Uninterruptable power supplies
- Onboard chargers
- DC-DC converters

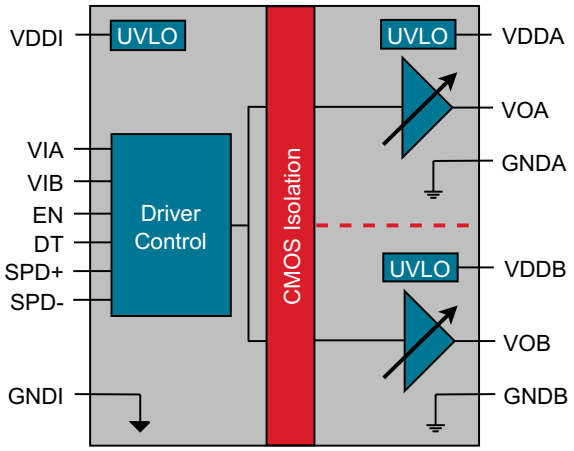
Safety Regulator Approvals (Pending)

- UL 1577 recognized
  - Up to 6000 V_{RMS} for one minute
- CSA certification conformity
  - 62368-1 (reinforced insulation)
  - 60601-1 (2 MOPP)
- VDE certification conformity
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1

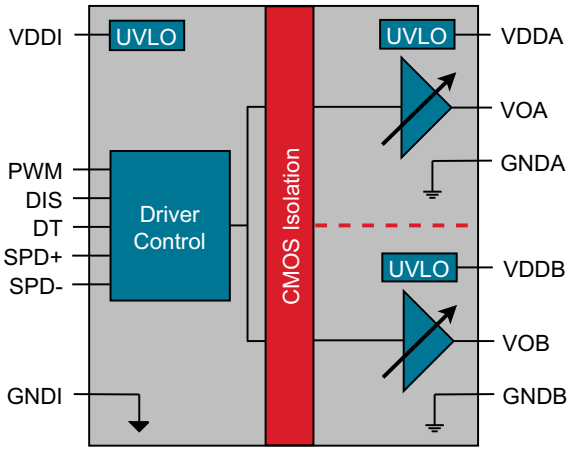
Key Features

- Wide input range of 3 to 20 V
- Wide gate supply voltage of 5 to 30 V
- CMOS input with an optional deglitch filter
- Channel-to-channel skew < 5 ns
- Dead time control and overlap protection
- Universal and High-Side/Low-Side pinouts
- Selectable Variable Current Drive (SelVCD™)
- Integrated Miller clamp
- High precision current source output
- CMTI > 200 kV/µs
- 1500 V_{RMS} working voltage
- Optimized UVLO of 4 V, 8 V, 12 V, or 15 V
- 4 kV HBM ESD rating
- No unknown output states
- Increased channel-to-channel creepage
- 6 kV_{RMS} safety rated isolation
- 10 kV bipolar surge
- Wide temperature range: –40 to 125 °C
- Narrow-body 16-pin SOIC and wide-body 14-pin SOIC packages
- AEC-Q100 qualification
- Automotive-grade OPNs available

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.



Si82F39x



Si82F89x

1. Pin Descriptions

1.1. Device Pinouts

The Si82Fx consists of multiple dies in packages with different bond-outs for different customer needs. Each bond-out corresponds to a pin-out below. See “10. Ordering Guide” on page 55 for the part numbers and features of these products.

1.1.1. NB SOIC-16 Pinouts

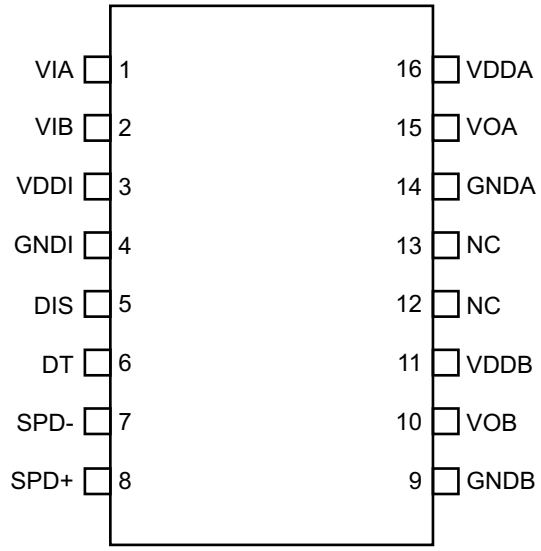


Figure 1. Si82F29x Pinout

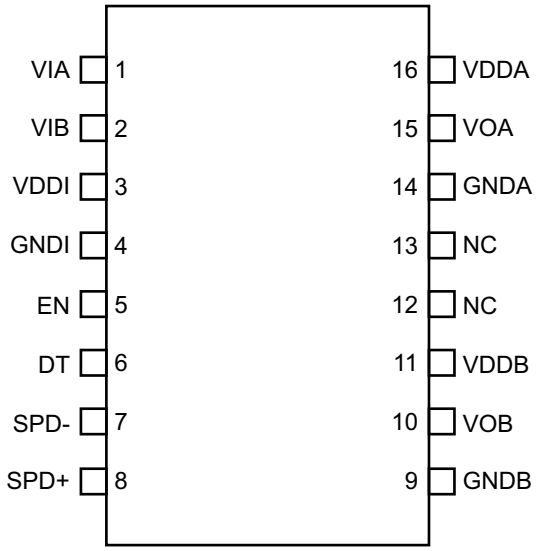


Figure 2. Si82F39x Pinout

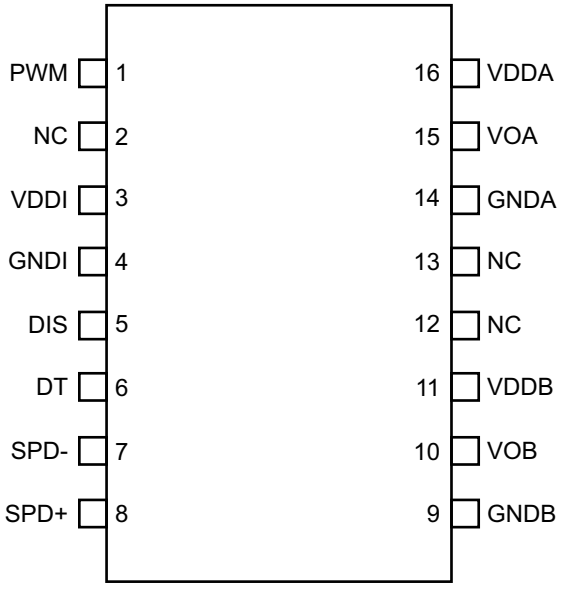


Figure 3. Si82F89x Pinout

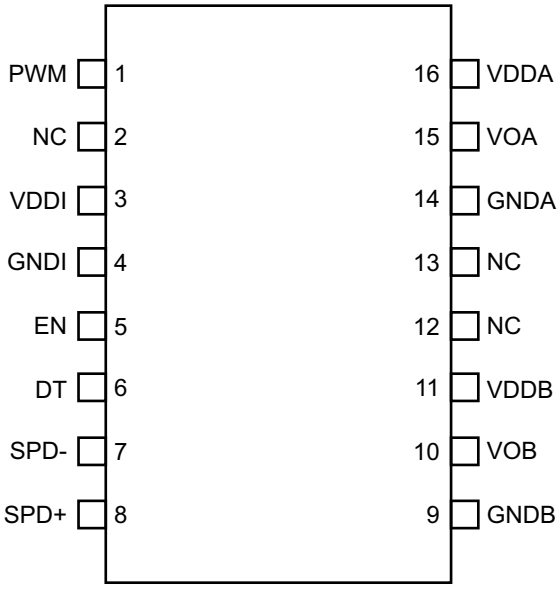


Figure 4. Si82F99x Pinout

1.1.2. WB SOIC-14 Pinouts

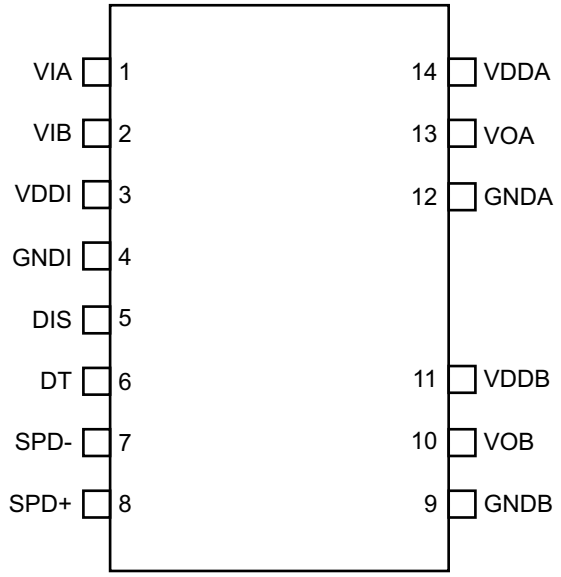


Figure 5. Si82F29x Pinout

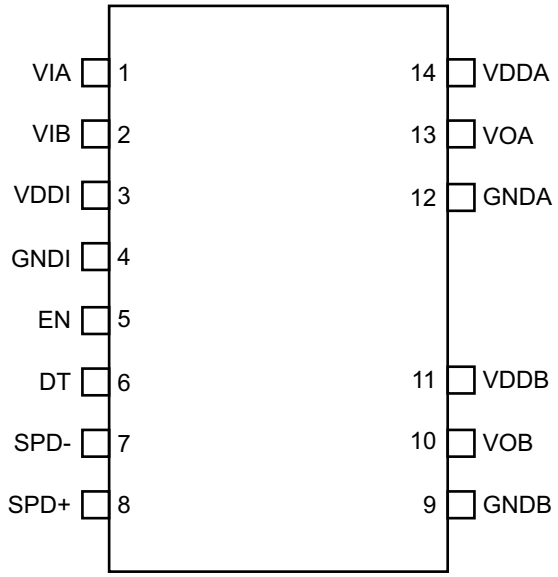


Figure 6. Si82F39x Pinout

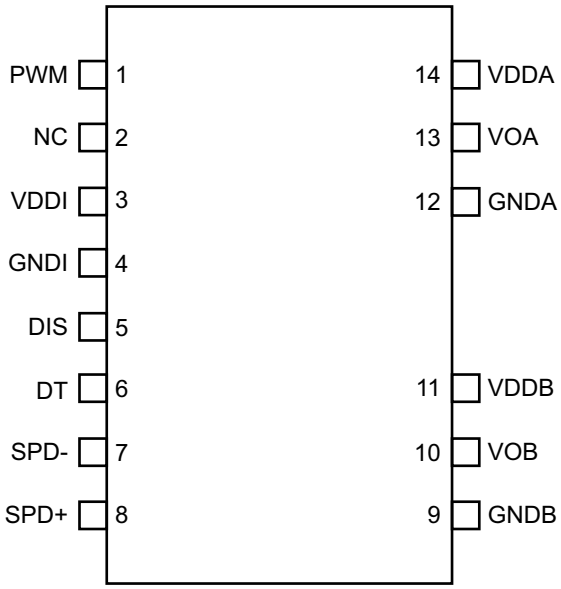


Figure 7. Si82F89x Pinout

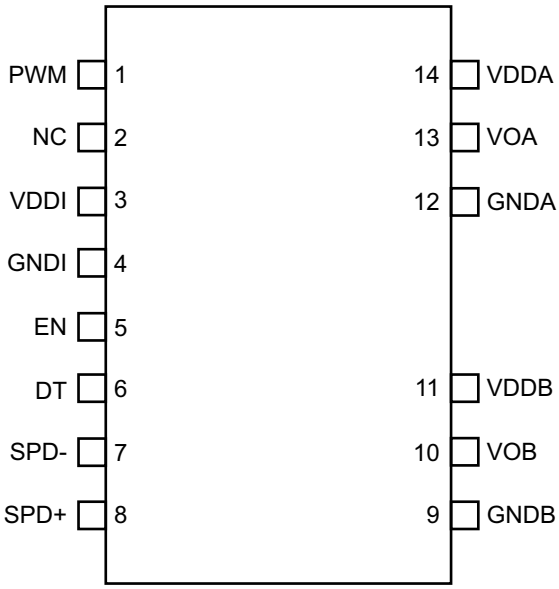


Figure 8. Si82F99x Pinout

1.2. Pin Details

Table 1. Si82Fx Pin Details

Pin Name	Pin Description
VDDI	Logic input power supply.
GNDI	Logic input ground terminal.
PWM	PWM logic input for gate driver A and gate driver B.
VIA	Non-inverting logic input terminal for gate driver A.
VIB	Non-inverting logic input terminal for gate driver B.
EN	Active high device ENABLE signal. When asserted (logic high), the device is enabled to perform in normal operating mode. When deasserted (logic low), this input unconditionally drives the output VOA and VOB logic low.
DIS	Active high device DISABLE signal. When asserted (logic high), this input unconditionally drives the output VOA and VOB logic low. When deasserted (logic low), the device is enabled to perform in normal operating mode.
DT	Dead time programming input. The value of the resistor connected from DT to GNDI sets the dead time between output transitions of VOA and VOB. Connecting DT to VDDI will disable dead time insertion on High-Side/Low-Side drivers. Connecting DT to VDDI will disable dead time insertion and overlap protection on Universal drivers.
SPD+	Driver strength programming input for sourcing current of driver A and driver B. The value of the resistor connected from SPD+ to GNDI sets the controlled sourcing current of the drivers. Connect SPD+ to GNDI to set the controlled sourcing current of the drivers to its minimal value. Connect SPD+ to VDDI to set the controlled sourcing current of the drivers to its maximal value.
SPD–	Driver strength programming input for sinking current of driver A and driver B. The value of the resistor connected from SPD– to GNDI sets the controlled sinking current of the drivers. Connect SPD– to GNDI to set the controlled sinking current of the drivers to its minimal value. Connect SPD– to VDDI to set the controlled sinking current of the drivers to its maximal value.
VDDA	Gate driver A power supply.
GNDA	Gate driver A ground terminal.
VDDB	Gate driver B power supply.
GNDB	Gate driver B ground terminal.
VOA	Gate driver A output.
VOB	Gate driver B output.
NC	No connection. The user should not connect anything to this pin.

2. Device Overview

The Si82Fx is an isolated two-channel gate driver available in a Universal or High-Side/Low-Side configuration. Each configuration can be purchased with either an asynchronous enable or disable input. Additional features such as undervoltage lockout (UVLO) level and deglitch filter time can be configured through device selection. Refer to “10. Ordering Guide” on page 55 for more details. Safety-rated isolation is provided from logic input to gate driver output by a pair of high-voltage silicon dioxide (SO_2) capacitors. These capacitors are duplicated to form a differential path for signals modulated with an RF carrier and using an on-off keying (OOK) modulation scheme. This approach optimizes for fault tolerance and timing performance between input and output.

The digital logic inputs are high-voltage capable, CMOS-compatible, Schmitt triggered, and deglitched for high noise immunity and a wide range of compatibility. See “4.4. Logic Input Signals” on page 12 for more details. Devices with a dead time input will operate as a High-Side/Low-Side driver for half-bridge circuits, inserting dead time between the two output channels and preventing shoot-through current. Additionally, for devices with a universal configuration, the dead time input can be connected to the VDDI supply to disable dead time insertion and overlap protection, enabling the device to operate as a dual driver. See “4.5. Dead Time Control and Overlap Protection” on page 13 for more information. The analog speed control inputs (SPD±) are also high-voltage tolerant and include a high-voltage clamp to protect the device's internal low-voltage circuits. The gate driver outputs operate as a current source. Output current is selectable between eight different levels, eliminating the need for gate resistors and enabling a built-in Miller clamp to operate directly on the gate driver output (VOA/B). See “4.6. Selectable Variable Current Drive (SelVCD™)” on page 15 for more information.

3. Functional Block Diagrams

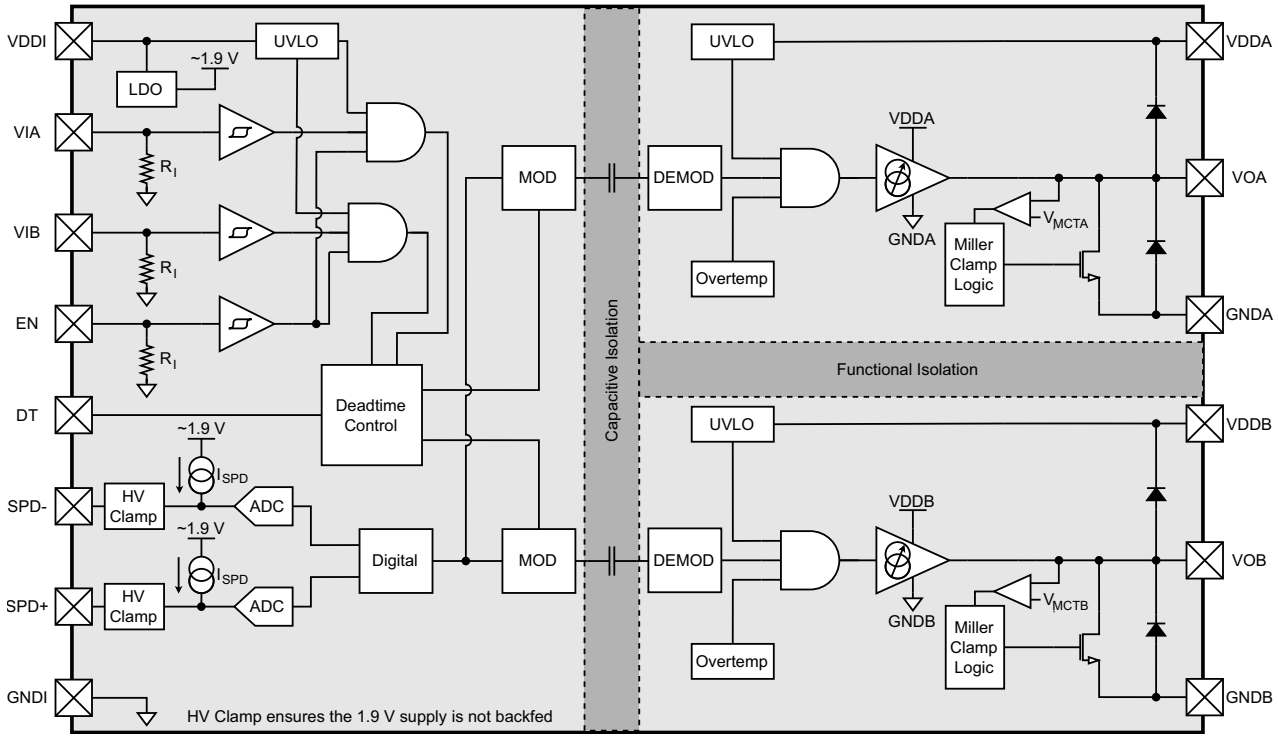


Figure 9. Si82F39x Device with Universal Configuration and Enable Input

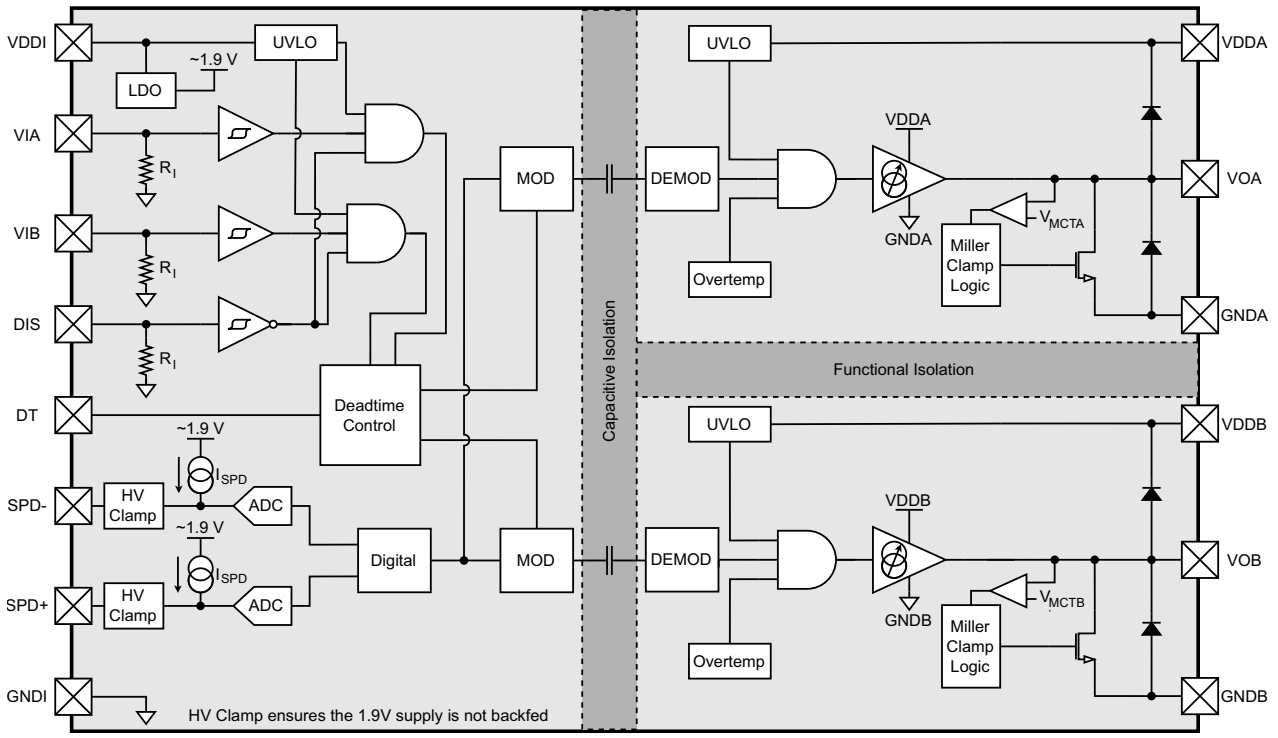


Figure 10. Si82F29x Device with Universal Configuration and Disable Input

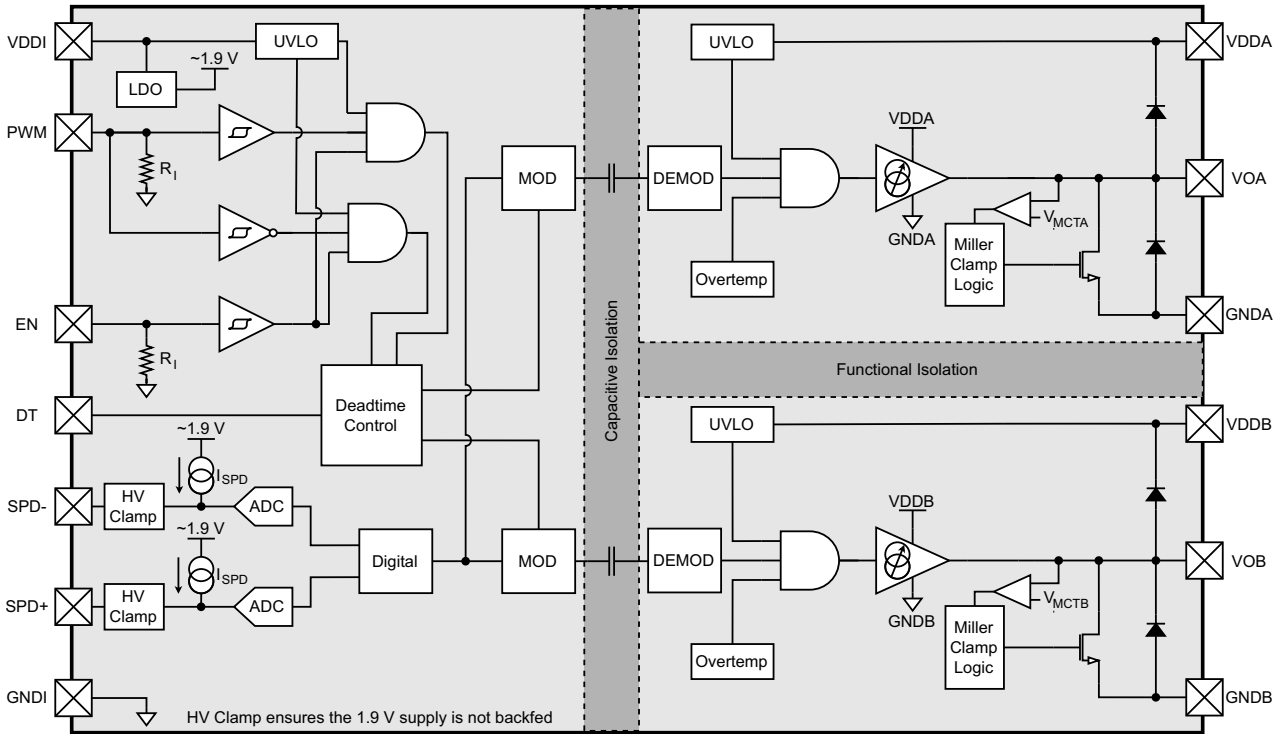


Figure 11. Si82F99x Device with High-Side/Low-Side Configuration and Enable Input

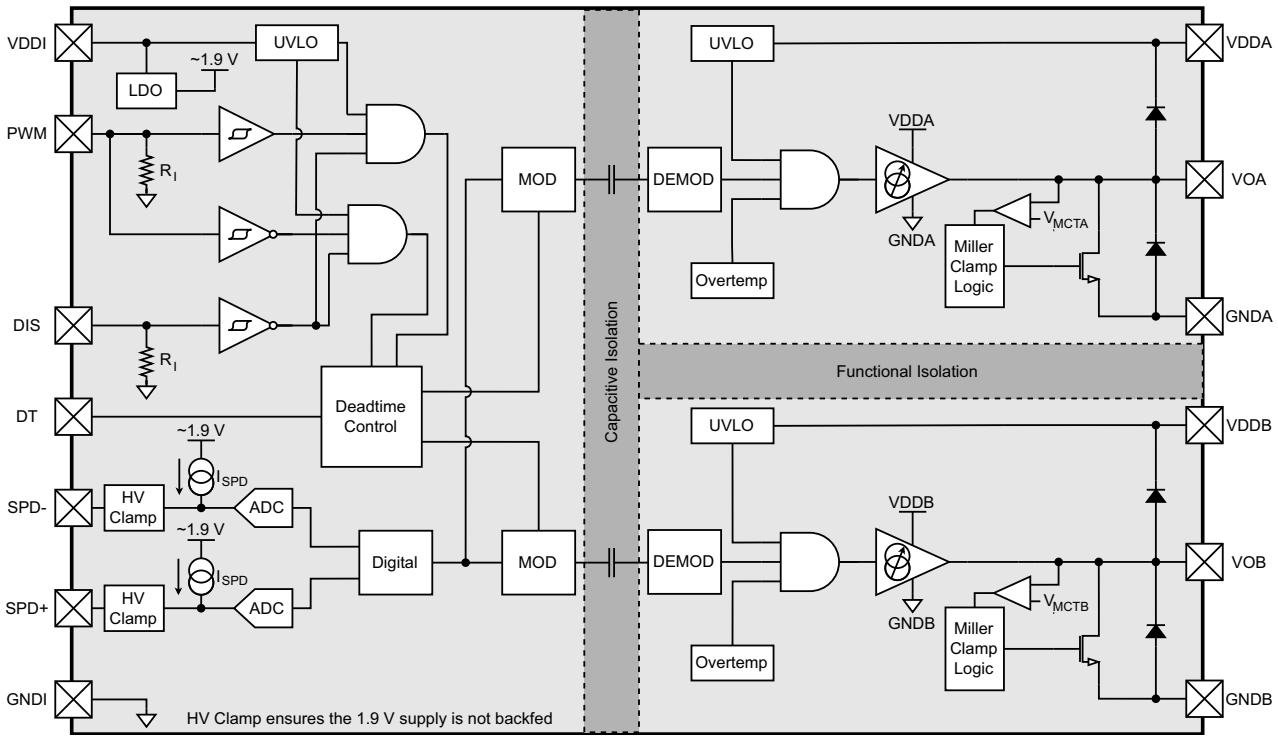


Figure 12. Si82F89x Device with High-Side/Low-Side Configuration and Disable Input

4. Device Operation

This section describes the capabilities of the device and how it should be used to achieve different goals within a design. Refer to "5.1. Recommended Application Circuits" on page 19 and "10. Ordering Guide" on page 55 for information on how to best utilize each device for different applications.

4.1. Truth Tables

The following tables describe the logical behavior of the Si82Fx Isolated Gate Driver devices.

Table 2. Si82F2x-3x Truth Table

Inputs[1]			Power Supply State[2]			Outputs[3]	
VIA	VIB	DIS/EN	VDDI[4]	VDDA[5]	VDDB[5]	VOA	VOB
H	L	E	P	P	—	H	L
L	H	E	P	—	P	L	H
H	H	E	P	P	P	H/L[6]	H/L[6]
L	L	X	—	—	—	L	L
X	X	D	—	—	—	L	L
X	X	X	NP	—	—	L	L
L	X	X	P	—	NP	L	L
H	H	E	P	P	NP	H/L[6]	L
X	L	X	P	NP	—	L	L
H	H	E	P	NP	P	L	H/L[6]

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. "E" indicates the driver is enabled (DIS = L or EN = H), "D" indicates the driver is disabled (DIS = H or EN = L). Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. "NP" is the "not powered" state; "P" is the "powered" state, and "—" is an irrelevant state.
3. "H" is a logic high (true) value, and "L" is a logic low (false). The logic low (L) value is enforced by the Shutdown Clamp (see "4.9. Shutdown Clamp" on page 17) if the same side gate driver's power supply (VDDA/B) is not powered (NP).
4. "Not powered" (NP) state is defined as VDDI < $VDDI_{UV}$. "Powered" (P) state is defined as VDDI > $VDDI_{UV}$.
5. "Not powered" (NP) state is defined as VDDA/B < $VDDA/B_{UV}$. "Powered" (P) state is defined as VDDA/B > $VDDA/B_{UV}$.
6. The output state depends on the dead time pin (DT). If the dead time pin is connected to VDDI, the output will be a logic high (H). If the dead time pin is not connected to VDDI, the output will be a logic low (L). See "4.5. Dead Time Control and Overlap Protection" on page 13 for more information.

Table 3. Si82F8x-9x Truth Table

Inputs[1]		Power Supply State[2]			Outputs[3]	
PWM	DIS/EN	VDDI[4]	VDDA[5]	VDDB[5]	VOA	VOB
H	E	P	P	—	H	L
L	E	P	—	P	L	H
X	D	P	—	—	L	L
X	X	NP	—	—	L	L
H	E	P	P	NP	H	L
L	E	P	—	NP	L	L
H	E	P	NP	—	L	L
L	E	P	NP	P	L	H

1. “X” is any logic value, “H” is a logic high (true) value, and “L” is a logic low (false) value. “E” indicates the driver is enabled (DIS = L or EN = H), “D” indicates the driver is disabled (DIS = H or EN = L). Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. “NP” is the “not powered” state; “P” is the “powered” state, and “—” is an irrelevant state.
3. “H” is a logic high (true) value, and “L” is a logic low (false). The logic low (L) value is enforced by the Shutdown Clamp (see “4.9. Shutdown Clamp” on page 17) if the same side gate driver's supply (VDDA/B) is not powered (NP).
4. “Not powered” (NP) state is defined as VDDI < $VDDI_{UV}$. “Powered” (P) state is defined as VDDI > $VDDI_{UV}$.
5. “Not powered” (NP) state is defined as VDDA/B < $VDDA/B_{UV}$. “Powered” (P) state is defined as VDDA/B > $VDDA/B_{UV}$.

4.2. Power Sequence and Timing Behavior

The device exhibits different timing behavior depending on the state of the power supplies as well as the driver inputs. Figure 13, "Gate Driver Timing Behavior," below shows how the analog power supply voltages are plotted against the digital input and output state of the device, with relevant device timings listed.

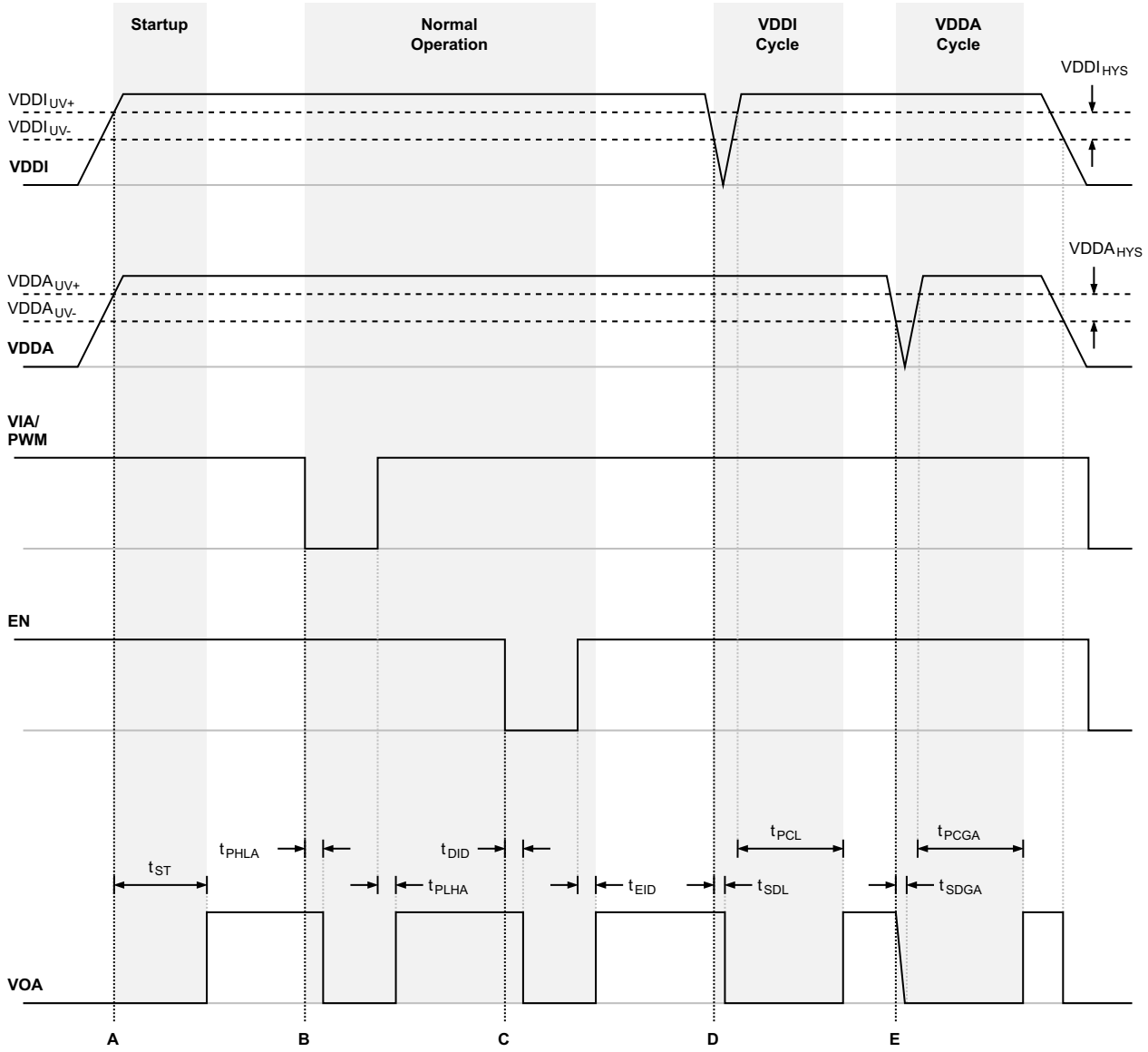


Figure 13. Gate Driver Timing Behavior

Note that this diagram shows the timing relationship between VDDA, VIA/PWM and VOA. However, the same timing relationship applies for VDDB, VIB and VOB.

4.3. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDDI or VDDA/B is below its specified operating circuits range. The power supplies associated with the logic input, gate driver A, and gate driver B each have undervoltage lockout monitors. The device's logic input enters UVLO when VDDI ≤ $VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The gate driver outputs, VOA and VOB, remain low when the logic input supply of the device is in UVLO, and their respective power supply (VDDA/B) is within the specified range. Each gate driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$, while simultaneously VOB will behave as described in "4.1. Truth Tables" on page 9 if its related power supply, VDDB, is not in UVLO. See "4.2. Power Sequence and Timing Behavior" on page 11 and "4.1. Truth Tables" on page 9 for more details.

4.4. Logic Input Signals

4.4.1. Control Inputs

VIA, VIB, PWM, EN, and DIS inputs are CMOS level-compatible, active-high inputs. When VDDI is in undervoltage lockout (UVLO), the inputs of these pins are ignored and the gate driver's outputs are pulled low. Disregarding the overlap protection behavior, for VIA/VIB input devices, the output follows the corresponding VIA or VIB input logic. For PWM input devices, VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low. Please refer to "4.1. Truth Tables" on page 9 and "4.5. Dead Time Control and Overlap Protection" on page 13 for detailed information on overlap protection behavior.

4.4.2. Enable and Disable Input

For devices with an enable (EN) input, when the EN input is driven low, it unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within t_{DID} after EN falls below V_{IL} and resumes within t_{EID} after EN rises above V_{IH}. For devices with a disable (DIS) input, when the DIS input is brought high, it unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within t_{DID} after DIS rises above V_{IH} and resumes within t_{EID} after DIS falls below V_{IL}. See Figure 13, "Gate Driver Timing Behavior," on page 11 for more details. The EN and DIS inputs have no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low).

4.4.3. Deglitch Filter

A deglitch feature is provided on some devices. The deglitch feature ignores input noise with a duration shorter than the deglitch filter setting, but also introduces additional propagation delay. See "6.2.4. Timing Characteristics" on page 33 for the delays associated with this feature. The deglitch filter can be adjusted by selecting different product options. See "10. Ordering Guide" on page 55 for more details.

4.5. Dead Time Control and Overlap Protection

Dead time provides a user-programmable delay between the transitions of VOA and VOB. This delay is programmed by connecting a resistor (R_{DT}) between the DT pin and ground. The appropriate value for R_{DT} can be determined from Equation 1 below.

$$t_{DT} = 1.73 \times R_{DT} + 5.74$$

Where:

t_{DT} is the Typical Dead Time delay (ns)

R_{DT} is the Dead Time Resistor (kΩ)

Equation 1.

The DT pin operates by outputting 0.9 V and monitoring the DT pin current. R_{DT} can be varied from 10 kΩ to 110 kΩ. With larger values of R_{DT}, the DT pin current can be very small and influenced by noise in the surrounding system. To aid in noise immunity, place a 0.1 µF ceramic capacitor in parallel with R_{DT}. The capacitor should be placed as close to the DT pin as possible.

An input signal's falling edge activates the programmed dead time for the other signal. The output's dead time is always set to the longer of either the driver's programmed dead time or the input signal's own dead time. If both inputs are high simultaneously, both outputs will be immediately driven low. This overlap protection feature is used to prevent a shoot-through event and does not affect the programmed dead time setting for normal operation. Figure 14, "Dead Time and Overlap Protection Behavior," on page 14 illustrates and explains various driver dead time logic operating conditions.

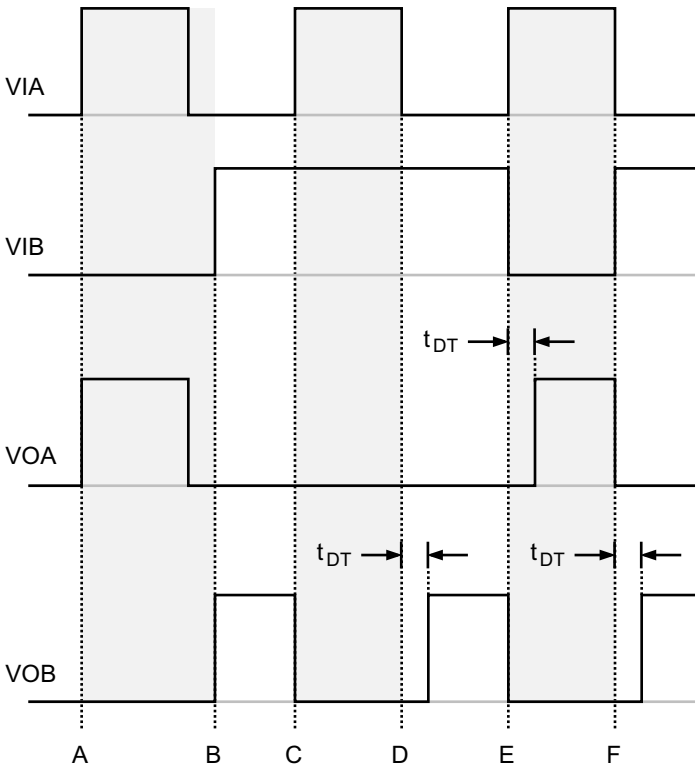


Figure 14. Dead Time and Overlap Protection Behavior

For signal conditions designated A through F in the figure, note the following:

A. The output VOA follows the input VIA exactly because VIB is already low.
B. The output VOB follows the input VIB exactly because VIA is already low.
C. The VIA input transitions high while the VIB input is already high. This causes both outputs, VOA and VOB, to immediately transition low due to overlap protection.
D. The VIA input transitions low and assigns the programmed dead time to VOB. Output VOB is allowed to transition high after the programmed dead time.
E. The VIA input transitions high simultaneously with the VIB input transitioning low. Output VOB immediately transitions low and assigns the programmed dead time to output VOA. The output VOA is allowed to transition high after the programmed dead time.
F. The VIB input transitions high simultaneously with the VIA input transitioning low. Output VOA immediately transitions low and assigns the programmed dead time to output VOB. The output VOB is allowed to transition high after the programmed dead time.

For devices in the Universal configuration, both dead time and overlap protection can be disabled by connecting the DT input pin to VDDI, forcing the device to operate as a dual driver instead of a High-Side/Low-Side driver. The output VOA tracks the VIA input and output VOB tracks the VIB input without any intervening protection mechanisms.

Refer to “10. Ordering Guide” on page 55 for details on which specific OPNs provide dead time and overlap protection.

4.6. Selectable Variable Current Drive (SelVCD™)

The gate driver output of the device operates as a current source, maintaining the driver's output current within ±10% of the typical value over temperature and semiconductor process variation for devices with an undervoltage lockout (UVLO) level of 8 V, 12 V and 15 V. The UVLO 4 V devices maintain their output current within ±15% of the typical value over temperature and semiconductor process variation as well. As the gate driver output behaves as a current source, the output current remains well-regulated over the gate driver supply voltage range. The typical output current is dependent on the gate driver UVLO level as defined in the “10. Ordering Guide” on page 55. The driver output will operate as a current source until it runs out of voltage headroom. In other words, the MOSFETs which comprise the gate drive output transition from the saturated region into the linear operating region. Typical headroom knees for SPD± 7, 5, 3, and 1 are shown in Figure 15, “SPD+ Output Current vs. Output Voltage,” and Figure 16, “SPD– Output Current vs. Output Voltage,” below. Note that SPD± settings not shown do exhibit the same behavior. See “6.2.3. Gate Driver Characteristics” on page 29 for details.

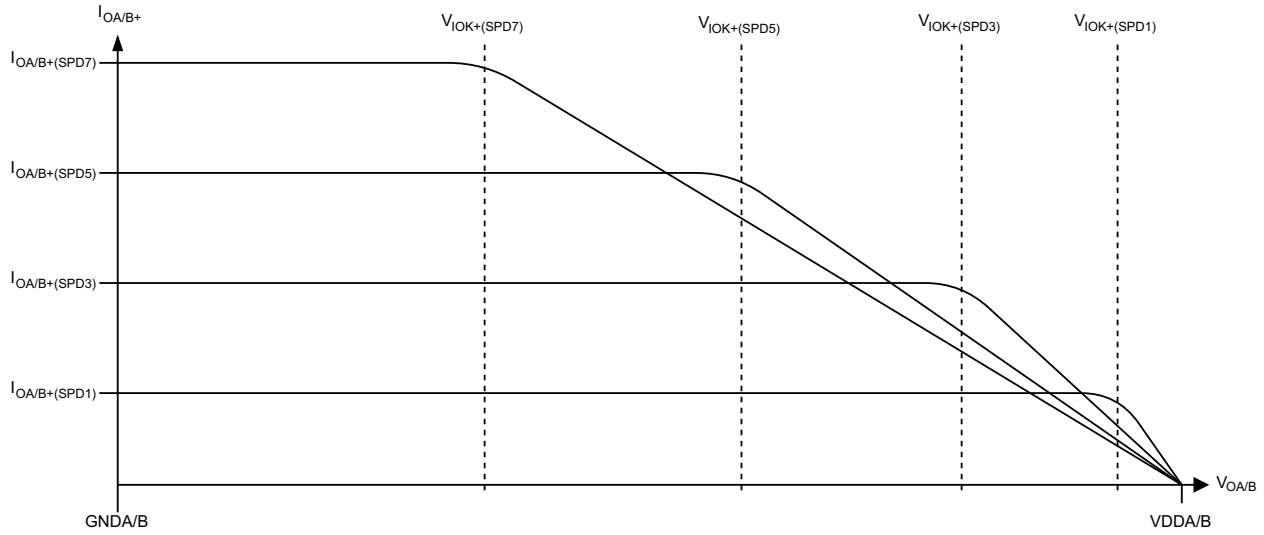


Figure 15. SPD+ Output Current vs. Output Voltage

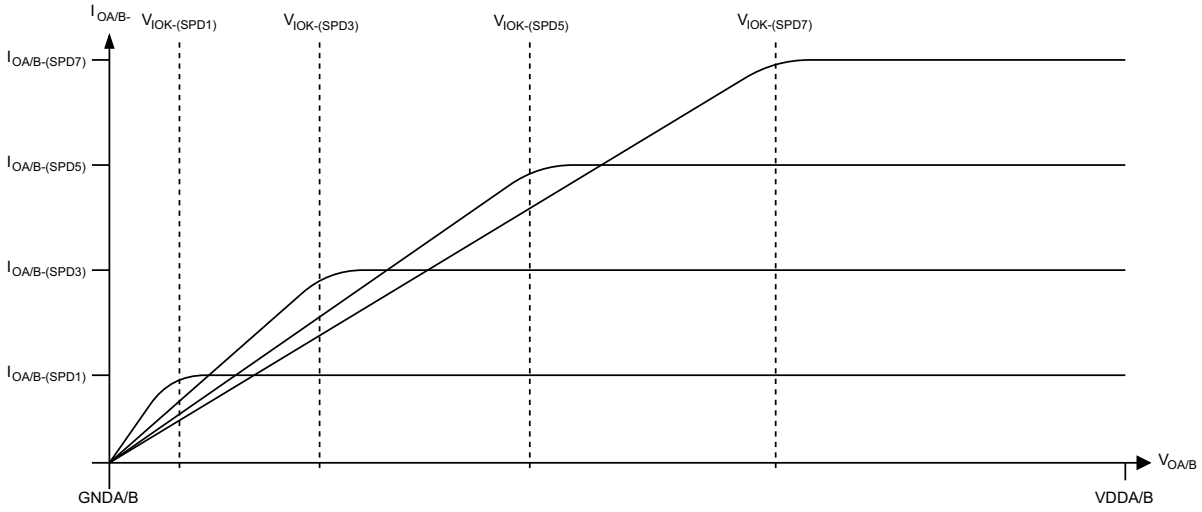


Figure 16. SPD– Output Current vs. Output Voltage

Each driver's output current, both sourcing and sinking, are user selectable among eight output current settings. The SPD+ pin controls the sourcing (turn-on) current and the SPD- pin controls the sinking (turn-off) current. Both outputs (VOA and VOB) are set to the same sourcing and sinking current setting indicated by the SPD± pins.

For static control of the SPD± pins, use 1% resistors between each SPD pin and ground. See "5.1. Recommended Application Circuits" on page 19 and the "SelVCD™ Resistor Settings" section of Table 6, "Logic Input Characteristics," on page 28 for more details. The SPD± pins operate by continuously sourcing $I_{SPD±}$ out of the pin and measuring the voltage at the pin.

If dynamic speed control is utilized, the resistors can be removed and a voltage source can be placed on the SPD± pins. For any specific speed (SPD) setting, ensure that the voltage on the SPD± pin is within the minimum and maximum bounds for the associated SPD level. See the "SelVCD™ Voltage Settings" section of Table 6, "Logic Input Characteristics," on page 28 for information on SPD voltage bounds. Note that the voltage source must be able to sink $I_{SPD±}$ per SPD± pin.

The sourcing and sinking current of VOA/B will change after Speed Update Delay (t_{SUD}). See "AN1390: Methods for Dynamic Speed Control of the Si82Fx Performance Driver" for more details on implementing dynamic speed control.

SelVCD™ eliminates the need for gate resistors and adds an integrated Miller clamp that operates through the gate driver output pin (VOA/B). The Miller clamp engages during the transition from V_{OH} to V_{OL}. When the output voltage, $V_{OA/B}$, falls below $V_{MCTA/B}$, the output speed setting temporarily changes from the current speed setting to SPD7– to maximize the sinking current. An example of the Miller clamp engaging is shown in Figure 17, "Miller Clamp Engagement Behavior," below. Note that if the current speed setting is SPD7–, no change will occur. The Miller clamp will stay engaged until the next V_{OL} to V_{OH} transition. If any voltage transients occur on VOA/B during the Off period, the Miller clamp will strongly clamp these to GNDA/B. The user-selected SPD– setting will be restored at the next V_{OH} to V_{OL} transition.

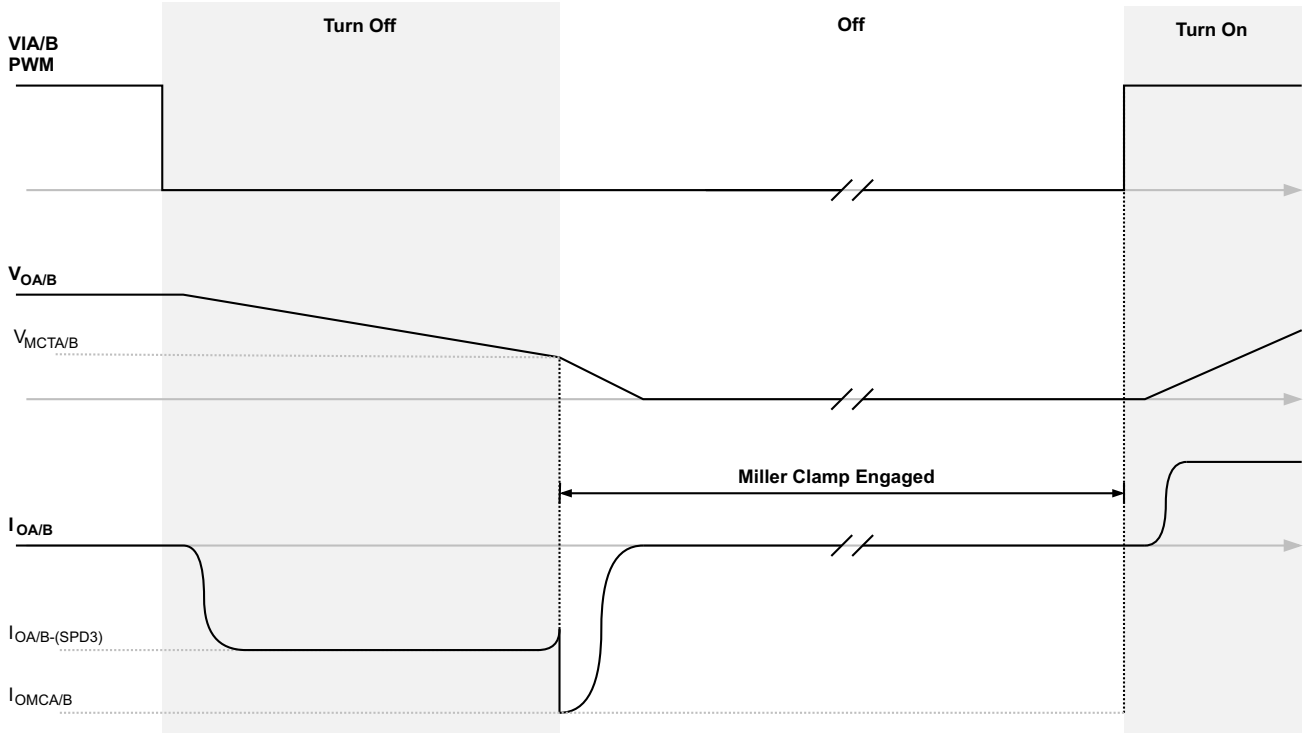


Figure 17. Miller Clamp Engagement Behavior

To achieve maximum Miller clamp performance, do not add any form of gate resistance between the gate driver output (VOA/B) and the power switch's gate or base. Usage of gate resistors will cause a voltage drop across the resistor, which will slow down turn-on and turn-off transitions and reduce the effectiveness of the Miller clamp.

In a traditional voltage-mode gate driver, external gate resistors dissipate a portion of the overall power required to charge and discharge the external power switch. As this power is dissipated internally in the Si82Fx, thermal protection (see "4.8. Thermal Protection" on page 17) will engage if power dissipation becomes excessive. See "5.3. Power Dissipation Considerations" on page 24 for more details.

4.7. Short-Circuit Clamp

The short circuit clamp is used to clamp voltages at the driver output (VOA/B) to slightly higher than the VDDA/B voltage during short circuit conditions. The short circuit clamp helps protect the driven switch gate from overvoltage breakdown or degradation. The clamp is implemented by adding a diode connection between VOA/B and the VDDA/B pins inside the driver. See "6.2.3. Gate Driver Characteristics" on page 29 for detailed specifications of this clamping feature. External diodes between VOA/B and VDDA/B can increase current conduction capability as needed.

4.8. Thermal Protection

The device includes a temperature sensor in each gate driver. Each sensor is monitored continuously. If the temperature exceeds the Trigger Temperature (T_{SD+}), a thermal shutdown fault will occur, and the driver will pull low. After 1 ms, if the driver temperature fails to fall below the Reset Temperature (T_{SD-}), the driver will pull weakly low. The driver will continuously pull weakly low until the temperature falls below T_{SD-}. Once the fault is removed, normal operation resumes.

4.9. Shutdown Clamp

The device includes a voltage clamp between the gate driver output (VOA/B) and ground (GNDA/B) when the gate driver is unpowered (VDDA/B = high-Z). This clamp is sometimes referred to as an "active pull-down clamp". It provides a path to ground for transient currents which could otherwise cause parasitic turn-on of a driven switch when the gate driver is unpowered. See "6.2.3. Gate Driver Characteristics" on page 29 and "4.1. Truth Tables" on page 9 for details.

4.10. ESD Structure

The Si82Fx device's I/O pin electrostatic discharge (ESD) diodes and associated supply pin ESD clamp diodes are illustrated in Figure 18, "Device ESD Structure," below. On the logic input side, a pair of ESD protection diodes are used on each input pin, and all upper diodes are connected to one shared clamp diode. This structure prevents the VDDI pin from being powered up through the input pin when the VDDI power supply is lost. The other clamp diode is present between the VDDI and GNDI pins. The ESD structure of the gate driver output is similar to the logic input, except that the upper diode is connected to a clamp diode at the VDDA/B pins.

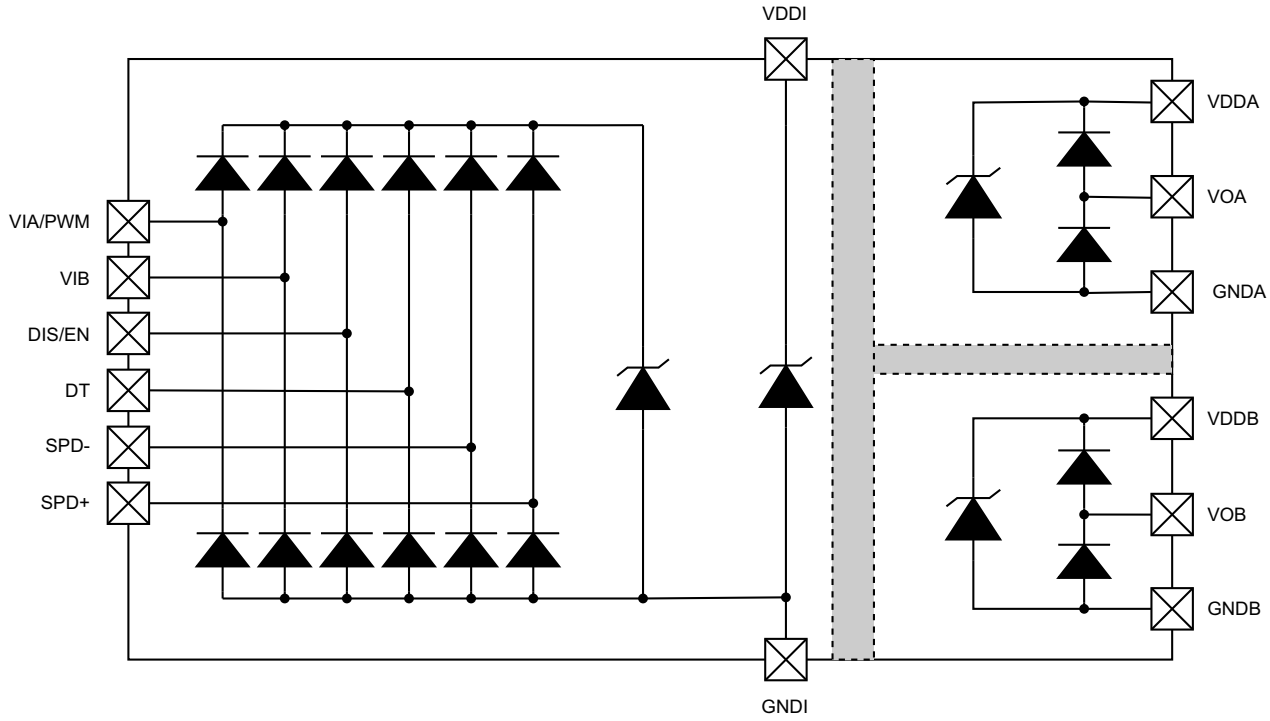


Figure 18. Device ESD Structure

5. Application Information

The Si82Fx is designed to be both flexible and robust to meet a wide range of application requirements, safely survive overloads, and rapidly recover normal operation. To achieve these objectives, the appropriate Si82Fx device must be selected and its circuit carefully designed.

5.1. Recommended Application Circuits

Figure 19, "High-Side/Low-Side Configuration," on page 20 illustrates a typical application circuit for a dual-input Si82Fx device connected in a half-bridge topology. Driver A of the Si82Fx device controls the high-side FET (Q1), and driver B controls the low-side FET (Q2). The controller provides the Si82Fx input signals (VIA and VIB) to control driver A and driver B. The Si82Fx device's input overlap protection feature ensures no concurrent conduction of FETs Q1 and Q2, even if both VIA and VIB input signals are High. The dead time is inserted before the rising edge of the gate drive signals. Since Q1 and Q2 FETs don't turn on or turn off instantly, the inserted dead time guarantees the opposite FET is completely off before the Si82Fx device turns on FETs Q1 or Q2. The dead time is adjustable through the R10 resistor connected to the DT pin. The controller can also use the EN/DIS signal to turn off both drivers immediately once a system fault is detected.

On the gate driver side, the Si82Fx device's SelVCD™ feature eliminates the need for external high power rated gate resistors at the gate driver's output. Resistors R13 and R17 connected to the SPD+/- pins are used to control the gate driver's output current strength, as described in "4.6. Selectable Variable Current Drive (SelVCD™)" on page 15. Their values should be selected to meet the gate voltage rise-time/fall-time requirement based on the actual capacitive loading of FETs Q1 and Q2. G2 is the reference point or the reference ground of the gate drive output circuit. Figure 19, "High-Side/Low-Side Configuration," on page 20 also shows two possible power supply connections for the high-side gate driver A. VDDA can be powered by an isolated supply or powered by the same supply for Gate Driver B through the bootstrap circuit (resistor R1 and diode D1). The bootstrap circuit is the convenient way to power the high-side gate driver for the High-Side/Low-Side circuit configuration. Its basic operation follows. When FET Q2 is turned on, capacitors C4 and C5 are charged by the low-side VDDB supply through diode D1 and the conducting FET Q2. After FET Q2 is off, when FET Q1 is turned on, the reference potential of capacitors C4 and C5 jumps to VBUS, and thus diode D1 is reverse biased. In this situation, capacitors C4 and C5 act as the voltage source supplying current to gate driver A in order to maintain a logic high output. Resistor R1 is used to limit the inrush current of capacitors C4 and C5. Resistor R1 additionally limits the voltage slew rate between gate driver A's supply pins (VDDA and GNDA). More details about the bootstrap circuit can be found in "AN486: High-Side Bootstrap Design Using ISODrivers in Power Delivery Systems".

Two high-voltage Y2-class capacitors (not shown in the diagram) between the logic input reference (GNDI) and the two gate driver references (GNDA and GNDB) are recommended if additional radiated emissions or electrostatic discharge (ESD) mitigation is desired. The typical value for these two Y2 capacitors is between 47 pF and 100 pF. See "AN1131: Design Guide for Reducing Radiated and Conducted Emissions in Isolated Systems Using Skyworks' Isolators" for additional techniques to mitigate radiated and conducted emissions. Note that the Si82Fx device provides excellent common-mode transient immunity (CMTI) without employing any additional components or techniques. However, if your application requires extremely high common mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI), including the no connect (NC) pins. This will help improve the CMTI performance.

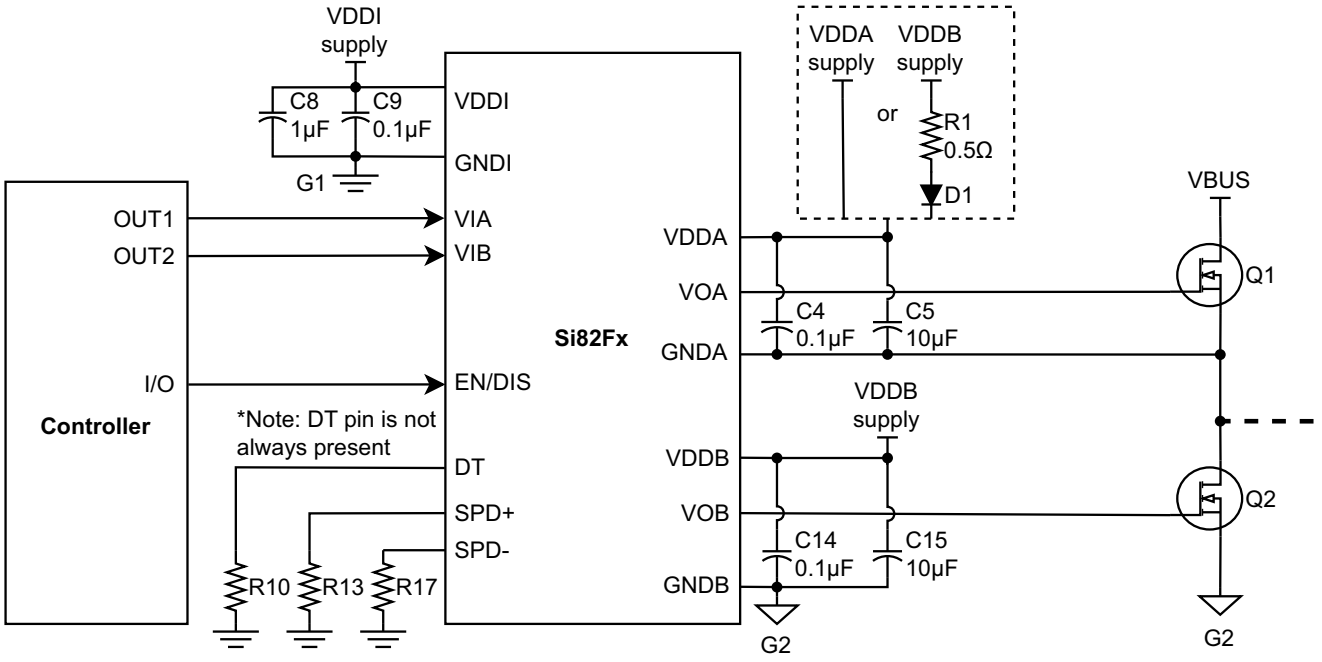


Figure 19. High-Side/Low-Side Configuration

The diagram shown in Figure 20, “Bipolar Output Connection,” on page 21 is similar to the above high-side/low-side configuration except that the drivers produce bipolar V_{GS} output voltage. The bipolar V_{GS} output requires the system to provide positive and negative voltage sources. Please note that the bootstrap circuit cannot be used to share the low-side voltage sources with the high-side Gate Driver A for a bipolar V_{GS} output application. In this example, +15 V and –5 V sources are used for low-side Gate Driver B, and its reference point is also G2. The other set of +15 V and –5 V sources are used for the high-side Gate Driver A. The high-side voltage sources' reference, G3, is electrically connected to FET Q1's source. Please note that the voltage potential at FET Q1's source jumps between VBUS and reference G2. Thus, the high-side voltage sources need to be isolated from reference G2 as well.

For the bipolar V_{GS} output application, the additional bypass capacitors form a capacitor divider which serves to shorten the current flow loop. These capacitors should be placed close to the Si82Fx device’s output power pins (VDDA/B). Taking the high-side gate driver A as an example, the ac component of the gate drive current flows from the VDDA net to the Si82Fx device’s VDDA pin, VOA pin, Q1's gate, Q1's source, the midpoint of capacitors C1 and C2, and back to VDDA. Since the original bypass capacitors, C4 and C5, do not connect to reference G3 (which is connected to FET Q1’s source), without capacitor C2, the return current needs to travel further to the system's +15 V source to complete the loop. This prolonged loop increases the chance of radiated emissions. Capacitors C11 and C12 serve the same purpose for the low-side FET Q2's gate drive return current.

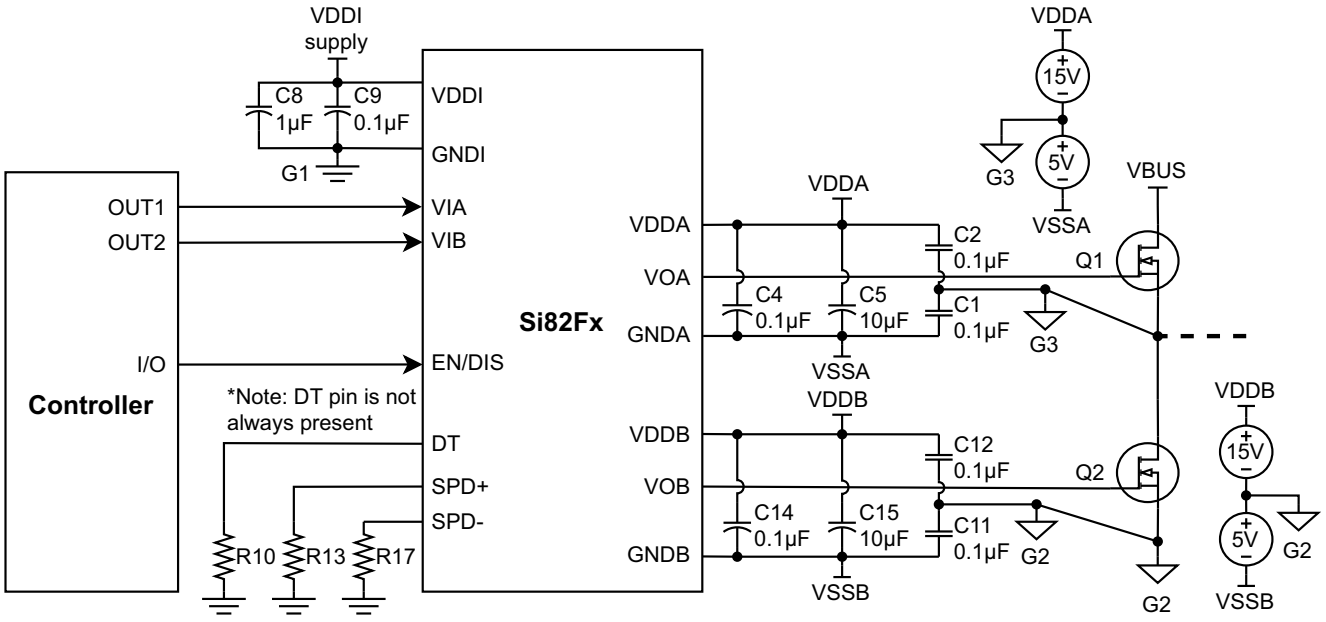


Figure 20. Bipolar Output Connection

Figure 21, "PWM Input Application Circuit," below depicts an Si82Fx device with a high-side/low-side configuration and a PWM input.

This application circuit is similar to Figure 19, "High-Side/Low-Side Configuration," on page 20, except that the controller only provides the PWM input signal. The Si82Fx device will split the input signal phase, insert dead time, and drive the high-side and low-side FETs accordingly.

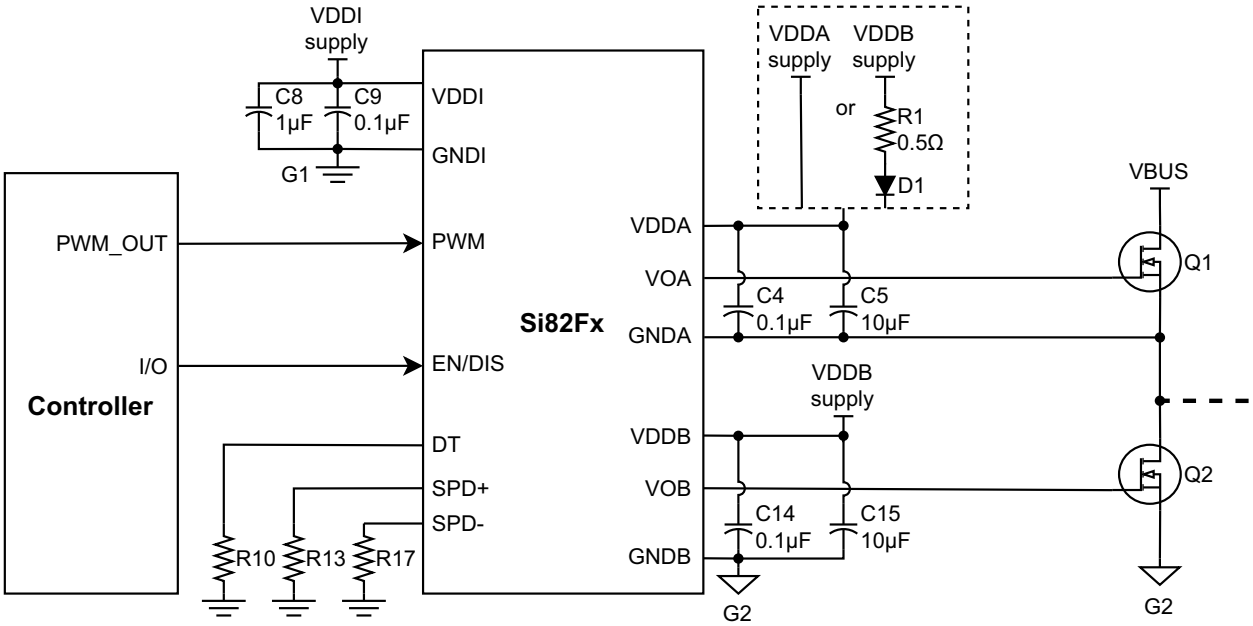


Figure 21. PWM Input Application Circuit

Figure 22, "Dual Low-Side Driver Application Circuit," below depicts the circuit for driving dual low-side FETs. When the dead time pin (DT) is tied to the logic input supply (VDDI), the Si82Fx device operates as a dual gate driver without overlap protection or dead time insertion. In this dual driver mode, the Si82Fx device can be used for high-side/low-side, dual high-side, dual low-side, or any circuit topology. However, the controller is responsible for providing overlap protection and dead-time insertion. In the dual low-side circuit topology depicted below, the +15 V and –5 V sources are shared by Gate Drivers A and B to generate bipolar V_{GS} outputs. For a dual high-side application, Driver A and Driver B cannot share the same power supply and will require the individual isolated power supplies, even if the V_{GS} output is unipolar.

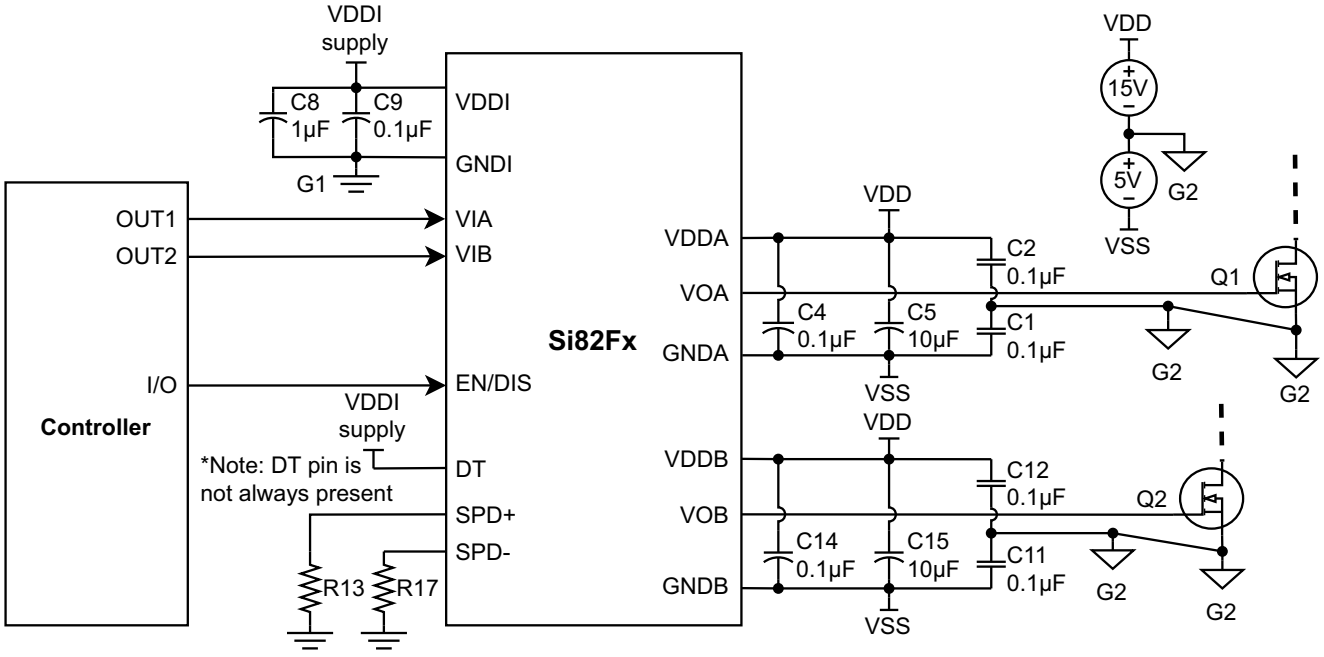


Figure 22. Dual Low-Side Driver Application Circuit

5.2. Layout Considerations

The layout considerations are divided into general considerations for the entire device, the logic input side of the device, and the gate driver side. Please refer to “5.1. Recommended Application Circuits” on page 19 for specific parts referenced.

5.2.1. General Considerations

- The bypass capacitors (usually 0.1 µF || 10 µF) should be placed close to the device's power supply pins and connected to the device with thick and short traces.
- The isolation barrier should have the required distance for the traces, power planes, ground planes, and copper areas on the device's logic input and gate drive sides.
- Safety isolation between gate drivers A and B on the gate driver side is usually not required. If the system needs safety isolation between gate drivers A and B, the trace, power plane, ground plane, and the copper area between the two gate drivers should have the required distance. Even though safety isolation between gate drivers A and B is usually not required, to avoid arcing through the air, the traces operating at high voltage should have some distance (approximately 1 mm per 1 kV) from the low voltage signals.
- The Si82Fx device is often used in high-power systems with significant switching current and transient voltage. Attention should be paid to the proximity and orientation of the Si82Fx device and any high-current switching circuits. This should also apply to the traces and components surrounding the Si82Fx device to avoid unwanted noise coupling.

5.2.2. Logic Input Considerations

- Place resistors R10, R13, and R17 close to the Si82Fx device’s dead time (DT) and speed (SPD±) pins, respectively.
- If your application requires extremely high common mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI), including the no connect (NC) pins. This will help improve the CMTI performance.
- Using ≥6 mil trace width on all logic input pins is recommended. The interconnection between the controller and the Si82Fx device should be kept from any noisy signals in the system.

5.2.3. Gate Driver Considerations

- If the system is designed to provide a bipolar V_{GS} output, additional bypass capacitors (C1, C2, C11, and C12 in Figure 20, "Bipolar Output Connection," on page 21) are required to minimize the return path of the gate drive signals.
- It is recommended to use ≥20 mil trace width for the VOA/B gate driver traces and their return path.
- For a unipolar V_{GS} output, the return path of the V_{GS} gate drive signal is from the power device's source/collector to the Si82Fx device's gate driver ground pin (GNDA/B). Explicitly use ≥20 mil trace width for this return current path and route this trace close to the VOA/B gate driver traces to reduce the loop area of the whole V_{GS} gate drive signal. Moreover, it is a good practice to set the copper keep-out region along the return path trace so the system ground copper will not flood over this return trace.
- For a bipolar V_{GS} output, the return path of the V_{GS} gate drive signal is from the power device's source/collector to the midpoint of capacitors C1/C2 or C11/C12. Therefore, these capacitors must be placed close to the Si82Fx device to minimize this current loop. Explicitly use ≥20 mil trace width for the return current path and route this return trace close to the VOA/VOB gate driver traces to reduce the loop area of the whole V_{GS} gate drive signal. Moreover, it is a good practice to set the copper keep-out region along the return path trace so the system ground copper will not flood over this return trace.
- For a multiple-layer PCB design, ground and power planes are recommended to create a power supply current path with the least inductance. If there is no dedicated power or ground plane on the gate driver side, please use ≥20 mil trace width for the power supply connections.
- If the design utilizes Y2 capacitors between the logic input and gate drivers, the Y2 capacitors across the isolation barrier should be placed as close as possible to the sides of the Si82Fx device without pins.

5.3. Power Dissipation Considerations

The device's average power dissipation is often required in order to estimate the silicon junction temperature. Since the Si82Fx doesn't utilize external gate resistors, the measured power consumption of the device is equal to its power dissipation. This is because the power switch being driven is a pure capacitive load, which doesn't consume real power. The device's power consumption is obtained by measuring the current consumption on each power supply input (VDDI, VDDA, and VDDB) and then multiplying it by its corresponding voltage.

Alternatively, the power dissipation can be estimated using the equation provided in "AN1339: Driver Power Dissipation Considerations". To solve the equation, the intended supply voltages, the load characteristics, and the switching frequency need to be collected. Skyworks provides a Microsoft Excel based calculator as part of "AN1339" to easily estimate the device's power dissipation and its silicon junction temperature.

6. Specifications

6.1. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Condition	Min	Max	Unit
Storage Temperature	T_{STG}		–65	150	°C
Operating Temperature	T_A		–40	125	°C
Junction Temperature	T_J		—	150	°C
Logic Input Supply Voltage	VDDI		–0.30	24	V
Gate Driver Supply Voltage	VDDA, VDDB		–0.30	36	V
Input Signal Voltage	VIA, VIB, PWM, DT, SPD+, SPD-, EN, DIS		–0.30	VDDI + 0.3	V
	VIA, VIB, PWM, SPD+, SPD-, EN, DIS	Transient for 100 ns[2]	–5.00	VDDI + 0.3	V
Output Signal Voltage	VOA, VOB		–0.30	$V_{DDA/B}$ + $V_{SCCA/B}$	V
		Transient for 200 ns[2]	–2.00	$V_{DDA/B}$ + $V_{SCCA/B}$	V
Lead Solder Temperature		Duration = 10 s	—	260	°C
ESD per AEC-Q100					
Human Body Model	HBM		–4	4	kV
Charged Device Model	CDM		–2	2	kV

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This parameter is not subject to production test. It is guaranteed by characterization.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

6.2. Electrical Characteristics

The following tables provide electrical parametric data for this device.

6.2.1. Power Supply Characteristics

Table 5. Power Supply Characteristics[1]

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage						
Logic Input Supply	VDDI		3.00	—	20.0	V
Gate Driver Supply	VDDA, VDDB		5.00	—	30.0	V
Supply Current						
Logic Input Supply						
Quiescent Current	$IDDI_Q$	EN = logic low or DIS = logic high	—	1.57	1.82	mA
Active Current	IDDI	VIA/B = 1 MHz; 50% duty cycle	—	2.45	2.74	mA
Gate Driver Supply						
4 V Undervoltage Lockout (Si82FxxxGx) Devices						
Quiescent Current	$IDDA_Q$, $IDDB_Q$	EN = logic low or DIS = logic high	—	2.93	4.02	mA
Active Current	IDDA, IDDB	VOA/B = 1 MHz; 50% duty cycle; no load; Speed 7	—	5.99	13.2	mA
8 V Undervoltage Lockout (Si82FxxxBx) Devices						
Quiescent Current	$IDDA_Q$, $IDDB_Q$	EN = logic low or DIS = logic high	—	2.95	4.02	mA
Active Current	IDDA, IDDB	VOA/B = 1 MHz; 50% duty cycle; no load; Speed 7	—	7.14	13.2	mA
12 V Undervoltage Lockout (Si82FxxxCx) Devices						
Quiescent Current	$IDDA_Q$, $IDDB_Q$	EN = logic low or DIS = logic high	—	3.00	4.02	mA
Active Current	IDDA, IDDB	VOA/B = 1 MHz; 50% duty cycle; no load; Speed 7	—	8.51	13.2	mA
15 V Undervoltage Lockout (Si82FxxxEx) Devices						
Quiescent Current	$IDDA_Q$, $IDDB_Q$	EN = logic low or DIS = logic high	—	3.06	4.02	mA
Active Current	IDDA, IDDB	VOA/B = 1 MHz; 50% duty cycle; no load; Speed 7	—	9.33	13.2	mA
Undervoltage Lockout						

Table 5. Power Supply Characteristics[1] (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Logic Input Supply						
Positive-Going Threshold	$VDDI_{UV+}$	VDDI rising	2.76	2.88	2.99	V
Negative-Going Threshold	$VDDI_{UV–}$	VDDI falling	2.64	2.78	2.94	
Threshold Hysteresis	$VDDI_{HYS}$		—	100	—	mV
Gate Driver Supply						
4 V Undervoltage Lockout (Si82FxxxGx) Devices						
Positive-Going Threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA/B rising	4.09	4.30	4.54	V
Negative-Going Threshold	$VDDA_{UV–}$, $VDDB_{UV–}$	VDDA/B falling	3.89	4.10	4.33	
Threshold Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$		—	200	—	mV
8 V Undervoltage Lockout (Si82FxxxBx) Devices						
Positive-Going Threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA/B rising	7.58	8.07	8.55	V
Negative-Going Threshold	$VDDA_{UV–}$, $VDDB_{UV–}$	VDDA/B falling	7.14	7.57	8.05	
Threshold Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$		—	500	—	mV
12 V Undervoltage Lockout (Si82FxxxCx) Devices						
Positive-Going Threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA/B rising	11.21	11.90	12.61	V
Negative-Going Threshold	$VDDA_{UV–}$, $VDDB_{UV–}$	VDDA/B falling	10.29	10.90	11.52	
Threshold Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$		—	1.00	—	V
15 V Undervoltage Lockout (Si82FxxxEx) Devices						
Positive-Going Threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA/B rising	14.19	15.15	16.13	V
Negative-Going Threshold	$VDDA_{UV–}$, $VDDB_{UV–}$	VDDA/B falling	13.81	14.70	15.66	
Threshold Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$		—	450	—	mV

1. Adding the suffix A/B to any symbol, parameter, or test condition variable denotes that the term applies interchangeably to either Gate Driver A or Gate Driver B.

6.2.2. Logic Input Characteristics

Table 6. Logic Input Characteristics

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Threshold						
High Input	V_{IH}	VIA, VIB, PWM, EN, DIS rising	VDDI x 0.75	—	—	V
Low Input	V_{IL}	VIA, VIB, PWM, EN, DIS falling	—	—	VDDI x 0.25	V
Hysteresis	V_{HYS}	VIA, VIB, PWM, EN, DIS	VDDI x 0.10	VDDI x 0.15	—	V
Input Pull-Down Resistance	R_I	VIA, VIB, PWM, EN, DIS	125	200	320	kΩ
Input Leakage Current	$\lvert I_{LKG} \rvert$	VIA, VIB, PWM, EN, DIS	—	—	140	µA
SelVCD™ Resistor Settings[1]						
Speed 0	R_{SPD0+}, $R_{SPD0–}$	SPD+, SPD–	—	0.00	—	kΩ
Speed 1	R_{SPD1+}, $R_{SPD1–}$	SPD+, SPD–	—	2.67	—	kΩ
Speed 2	R_{SPD2+}, $R_{SPD2–}$	SPD+, SPD–	—	4.12	—	kΩ
Speed 3	R_{SPD3+}, $R_{SPD3–}$	SPD+, SPD–	—	5.62	—	kΩ
Speed 4	R_{SPD4+}, $R_{SPD4–}$	SPD+, SPD–	—	7.32	—	kΩ
Speed 5	R_{SPD5+}, $R_{SPD5–}$	SPD+, SPD–	—	9.53	—	kΩ
Speed 6	R_{SPD6+}, $R_{SPD6–}$	SPD+, SPD–	—	12.4	—	kΩ
Speed 7[2]	R_{SPD7+}, $R_{SPD7–}$	SPD+, SPD–	—	15.8	—	kΩ
SelVCD™ Voltage Settings						
Speed 0	V_{SPD0+}, $V_{SPD0–}$	SPD+, SPD–	0.00	—	85.0	mV
Speed 1	V_{SPD1+}, $V_{SPD1–}$	SPD+, SPD–	127	—	145	mV
Speed 2	V_{SPD2+}, $V_{SPD2–}$	SPD+, SPD–	197	—	224	mV
Speed 3	V_{SPD3+}, $V_{SPD3–}$	SPD+, SPD–	268	—	306	mV
Speed 4	V_{SPD4+}, $V_{SPD4–}$	SPD+, SPD–	350	—	398	mV
Speed 5	V_{SPD5+}, $V_{SPD5–}$	SPD+, SPD–	455	—	518	mV
Speed 6	V_{SPD6+}, $V_{SPD6–}$	SPD+, SPD–	593	—	674	mV
Speed 7[2]	V_{SPD7+}, $V_{SPD7–}$	SPD+, SPD–	755	—	858	mV
SelVCD™ Resistor Current	I_{SPD+}, $I_{SPD–}$	SPD+, SPD–	49.3	51.0	52.7	µA

1. Specified with E96 1% accuracy resistors. See "4.6. Selectable Variable Current Drive (SelVCD™)" on page 15 for more information.
2. The SPD+ or SPD- pins may also be tied to VDDI to select Speed 7.

6.2.3. Gate Driver Characteristics

Table 7. Gate Driver Characteristics[1]

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} = 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage						
Logic High (Sourcing)	V_{OHA}, V_{OHB}	$I_{OA/B}$ = –20 mA	VDDA/B x 0.98	—	—	V
Logic Low (Sinking)	V_{OLA}, V_{OLB}	$I_{OA/B}$ = 20 mA	—	—	0.10	V
Output Resistance						
Logic High (Sourcing)	R_{ONA+}, R_{ONB+}	15 V UVLO, SPD 7	—	1.00	—	Ω
Logic Low (Sinking)	$R_{ONA–}$, $R_{ONB–}$		—	0.70	—	Ω
Output Current						
4 V Undervoltage Lockout (Si82FxxxGx) Devices						
Logic High (Sourcing)	I_{OA+}, I_{OB+}	Speed 7, VDDA/B = 6 V, $V_{OA/B}$ = 1.5 V	1.27	1.50	1.73	A
Logic Low (Sinking)	$I_{OA–}$, $I_{OB–}$	Speed 7, VDDA/B = 6 V, $V_{OA/B}$ = 4.5 V	1.27	1.50	1.73	A
8 V Undervoltage Lockout (Si82FxxxBx) Devices						
Logic High (Sourcing)	I_{OA+}, I_{OB+}	Speed 7, VDDA/B = 10 V, $V_{OA/B}$ = 3 V	2.25	2.50	2.75	A
Logic Low (Sinking)	$I_{OA–}$, $I_{OB–}$	Speed 7, VDDA/B = 10 V, $V_{OA/B}$ = 7 V	2.25	2.50	2.75	A
12 V Undervoltage Lockout (Si82FxxxCx) Devices						
Logic High (Sourcing)	I_{OA+}, I_{OB+}	Speed 7, VDDA/B = 15 V, $V_{OA/B}$ = 5 V	3.15	3.50	3.85	A
Logic Low (Sinking)	$I_{OA–}$, $I_{OB–}$	Speed 7, VDDA/B = 15 V, $V_{OA/B}$ = 10 V	3.15	3.50	3.85	A
15 V Undervoltage Lockout (Si82FxxxEx) Devices						
Logic High (Sourcing)	I_{OA+}, I_{OB+}	Speed 7, VDDA/B = 18 V, $V_{OA/B}$ = 6 V	3.60	4.00	4.40	A
Logic Low (Sinking)	$I_{OA–}$, $I_{OB–}$	Speed 7, VDDA/B = 18 V, $V_{OA/B}$ = 12 V	3.60	4.00	4.40	A
Output Current Ratio						
Logic High (Sourcing)						
Speed 0	$\Delta_{IOA+(0:7)}$, $\Delta_{IOB+(0:7)}$	$I_{OA/B(SPD0)} \div I_{OA/B(SPD7)}$	5.08	8.75	12.6	%
Speed 1	$\Delta_{IOA+(1:7)}$, $\Delta_{IOB+(1:7)}$	$I_{OA/B(SPD1)} \div I_{OA/B(SPD7)}$	8.93	12.5	16.9	%
Speed 2	$\Delta_{IOA+(2:7)}$, $\Delta_{IOB+(2:7)}$	$I_{OA/B(SPD2)} \div I_{OA/B(SPD7)}$	14.1	17.5	23.3	%
Speed 3	$\Delta_{IOA+(3:7)}$, $\Delta_{IOB+(3:7)}$	$I_{OA/B(SPD3)} \div I_{OA/B(SPD7)}$	20.1	25.0	31.7	%
Speed 4	$\Delta_{IOA+(4:7)}$, $\Delta_{IOB+(4:7)}$	$I_{OA/B(SPD4)} \div I_{OA/B(SPD7)}$	30.9	35.0	42.8	%
Speed 5	$\Delta_{IOA+(5:7)}$, $\Delta_{IOB+(5:7)}$	$I_{OA/B(SPD5)} \div I_{OA/B(SPD7)}$	44.6	50.0	58.6	%

Table 7. Gate Driver Characteristics[1] (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} = 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Speed 6	$\Delta_{IOA+(6:7)}$, $\Delta_{IOB+(6:7)}$	$I_{OA/B(SPD6)} \div I_{OA/B(SPD7)}$	62.9	70.0	79.2	%
Speed 7	$\Delta_{IOA+(7:7)}$, $\Delta_{IOB+(7:7)}$	$I_{OA/B(SPD7)} \div I_{OA/B(SPD7)}$	100	100	100	%
Logic Low (Sinking)						
Speed 0	$\Delta_{IOA-(0:7)}$, $\Delta_{IOB-(0:7)}$	$I_{OA/B(SPD0)} \div I_{OA/B(SPD7)}$	5.67	8.75	14.5	%
Speed 1	$\Delta_{IOA-(1:7)}$, $\Delta_{IOB-(1:7)}$	$I_{OA/B(SPD1)} \div I_{OA/B(SPD7)}$	9.89	12.5	18.4	%
Speed 2	$\Delta_{IOA-(2:7)}$, $\Delta_{IOB-(2:7)}$	$I_{OA/B(SPD2)} \div I_{OA/B(SPD7)}$	15.6	17.5	24.4	%
Speed 3	$\Delta_{IOA-(3:7)}$, $\Delta_{IOB-(3:7)}$	$I_{OA/B(SPD3)} \div I_{OA/B(SPD7)}$	22.9	25.0	32.4	%
Speed 4	$\Delta_{IOA-(4:7)}$, $\Delta_{IOB-(4:7)}$	$I_{OA/B(SPD4)} \div I_{OA/B(SPD7)}$	33.0	35.0	45.6	%
Speed 5	$\Delta_{IOA-(5:7)}$, $\Delta_{IOB-(5:7)}$	$I_{OA/B(SPD5)} \div I_{OA/B(SPD7)}$	45.7	50.0	61.0	%
Speed 6	$\Delta_{IOA-(6:7)}$, $\Delta_{IOB-(6:7)}$	$I_{OA/B(SPD6)} \div I_{OA/B(SPD7)}$	65.9	70.0	81.5	%
Speed 7	$\Delta_{IOA-(7:7)}$, $\Delta_{IOB-(7:7)}$	$I_{OA/B(SPD7)} \div I_{OA/B(SPD7)}$	100	100	100	%
Output Current Knee						
4 V Undervoltage Lockout (Si82FxxxGx) Devices						
Logic High (Sourcing)						
Speed 1	$V_{IOK+(SPD1)}$	VDDA/B = 6 V	—	4.05	—	V
Speed 3	$V_{IOK+(SPD3)}$		—	3.90	—	V
Speed 5	$V_{IOK+(SPD5)}$		—	3.60	—	V
Speed 7	$V_{IOK+(SPD7)}$		—	3.10	—	V
Logic Low (Sinking)[2]						
Speed 1	$V_{IOK-(SPD1)}$	VDDA/B = 6 V	—	$V_{MCTA/B}$	—	V
Speed 3	$V_{IOK-(SPD3)}$		—	$V_{MCTA/B}$	—	V
Speed 5	$V_{IOK-(SPD5)}$		—	$V_{MCTA/B}$	—	V
Speed 7	$V_{IOK-(SPD7)}$		—	$V_{MCTA/B}$	—	V
8 V Undervoltage Lockout (Si82FxxxBx) Devices						
Logic High (Sourcing)						
Speed 1	$V_{IOK+(SPD1)}$	VDDA/B = 10 V	—	6.75	—	V
Speed 3	$V_{IOK+(SPD3)}$		—	6.45	—	V
Speed 5	$V_{IOK+(SPD5)}$		—	6.10	—	V
Speed 7	$V_{IOK+(SPD7)}$		—	5.45	—	V
Logic Low (Sinking)[2]						
Speed 1	$V_{IOK-(SPD1)}$	VDDA/B = 10 V	—	$V_{MCTA/B}$	—	V
Speed 3	$V_{IOK-(SPD3)}$		—	$V_{MCTA/B}$	—	V
Speed 5	$V_{IOK-(SPD5)}$		—	$V_{MCTA/B}$	—	V
Speed 7	$V_{IOK-(SPD7)}$		—	3.40	—	V

Table 7. Gate Driver Characteristics[1] (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} = 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
12 V Undervoltage Lockout (Si82FxxxCx) Devices						
Logic High (Sourcing)						
Speed 1	$V_{IOK+(SPD1)}$	VDDA/B = 15 V	—	9.90	—	V
Speed 3	$V_{IOK+(SPD3)}$		—	9.65	—	V
Speed 5	$V_{IOK+(SPD5)}$		—	9.20	—	V
Speed 7	$V_{IOK+(SPD7)}$		—	8.40	—	V
Logic Low (Sinking)						
Speed 1	$V_{IOK-(SPD1)}$	VDDA/B = 15 V	—	2.50	—	V
Speed 3	$V_{IOK-(SPD3)}$		—	2.95	—	V
Speed 5	$V_{IOK-(SPD5)}$		—	3.65	—	V
Speed 7	$V_{IOK-(SPD7)}$		—	4.60	—	V
15 V Undervoltage Lockout (Si82FxxxEx) Devices						
Logic High (Sourcing)						
Speed 1	$V_{IOK+(SPD1)}$	VDDA/B = 18 V	—	11.75	—	V
Speed 3	$V_{IOK+(SPD3)}$		—	11.45	—	V
Speed 5	$V_{IOK+(SPD5)}$		—	10.95	—	V
Speed 7	$V_{IOK+(SPD7)}$		—	10.15	—	V
Logic Low (Sinking)						
Speed 1	$V_{IOK-(SPD1)}$	VDDA/B = 18 V	—	2.95	—	V
Speed 3	$V_{IOK-(SPD3)}$		—	3.55	—	V
Speed 5	$V_{IOK-(SPD5)}$		—	4.30	—	V
Speed 7	$V_{IOK-(SPD7)}$		—	5.35	—	V

Table 7. Gate Driver Characteristics[1] (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} = 1 MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Miller Clamp						
Threshold Voltage	V_{MCTA}, V_{MCTB}		1.75	2.00	2.35	V
Output Current						
4 V Undervoltage Lockout (Si82FxxxGx) Devices	I_{OMCA}, I_{OMCB}	VDDA/B = 6 V, $V_{OA/B}$ = $V_{MCTA/B}$	—	1.50	—	A
		VDDA/B = 6 V, $V_{OA/B}$ = 4.5 V	—	1.50	—	A
8 V Undervoltage Lockout (Si82FxxxBx) Devices		VDDA/B = 10 V, $V_{OA/B}$ = $V_{MCTA/B}$	—	1.80	—	A
		VDDA/B = 10 V, $V_{OA/B}$ = 7 V	—	2.50	—	A
12 V Undervoltage Lockout (Si82FxxxCx) Devices		VDDA/B = 15 V, $V_{OA/B}$ = $V_{MCTA/B}$	—	1.90	—	A
		VDDA/B = 15 V, $V_{OA/B}$ = 10 V	—	3.50	—	A
15 V Undervoltage Lockout (Si82FxxxEx) Devices		VDDA/B = 18 V, $V_{OA/B}$ = $V_{MCTA/B}$	—	2.10	—	A
		VDDA/B = 18 V, $V_{OA/B}$ = 12 V	—	4.00	—	A
Output Resistance	R_{ONMCA}, R_{ONMCB}		—	0.70	—	Ω
Short Circuit Clamp						
Clamping Voltage	V_{SCCA}, V_{SCCB}	VOA/B – VDDA/B or GNDA/B – VOA/B, $I_{OA/B}$ = 70 mA	—	70.0	—	mV
		VOA/B – VDDA/B or GNDA/B – VOA/B, $I_{OA/B}$ = 500 mA, $t_{SCCA/B}$ = 10 µs	—	530	—	mV
Thermal Shutdown						
Trigger Temperature	T_{SD+}	T_J rising	—	163	—	°C
Release Temperature	$T_{SD–}$	T_J falling	—	131	—	°C
Shutdown Clamp Output Voltage	V_{SDCA}, V_{SDCB}	VDDA/B = High-Z, $I_{OA/B}$ = 50 mA	—	1.55	2.00	V

1. Adding the suffix A/B to any symbol, parameter, or test condition variable denotes that the term applies interchangeably to either gate driver A or gate driver B.
2. A typical value referencing the Miller Clamp Threshold Voltage ($V_{MCTA/B}$) indicates that the current does not fall below 85% of the stated output current before the Miller clamp engages.

6.2.4. Timing Characteristics

Table 8. Timing Characteristics[1]

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Minimum Pulse Width						
Si82FxxAx Devices	PW_{MINA}, PW_{MINB}	No load	—	10.0	—	ns
Si82FxxBx Devices			—	30.0	—	ns
Si82FxxEx Devices			—	90.0	—	ns
Propagation Delay						
Positive-Going Control Input[2]						
0 ns Deglitch (Si82FxxAx) Devices	t_{PLHA}, t_{PLHB}	VIA, VIB, PWM rising; no load	20.0	30.0	40.0	ns
30 ns Deglitch (Si82FxxBx) Devices			45.0	52.5	65.0	ns
90 ns Deglitch (Si82FxxEx) Devices			100	115	140	ns
Negative-Going Control Input[2]						
0 ns Deglitch (Si82FxxAx) Devices	t_{PHLA}, t_{PHLB}	VIA, VIB, PWM falling; no load	20.0	30.0	40.0	ns
30 ns Deglitch (Si82FxxBx) Devices			45.0	52.5	65.0	ns
90 ns Deglitch (Si82FxxEx) Devices			100	115	140	ns
Enable Input Delay[3]	t_{EID}	EN rising or DIS falling, no load	20.0	30.0	40.0	ns
Disable Input Delay[3]	t_{DID}	EN falling or DIS rising, no load	20.0	30.0	40.0	ns
Speed Update Delay[4]	t_{SUD}	SPD+, SPD–	—	65.0	—	µs
Pulse Width Distortion	PWD_A, PWD_B	$\lvert t_{PHLA/B} - t_{PHLA/B} \rvert$	—	5.00	10.0	ns

Table 8. Timing Characteristics[1] (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay Skew						
Channel-to-Channel[5]						
0 ns Deglitch (Si82FxxAx) Devices	$t_{PSK(CC)}$	MAX{ $\lvert t_{PLHA}-t_{PLHB}\rvert$, $\lvert t_{PHLA}-t_{PHLB}\rvert$ }	—	—	5.00	ns
30 ns Deglitch (Si82FxxBx) Devices			—	—	8.00	ns
90 ns Deglitch (Si82FxxEx) Devices			—	—	20.0	ns
Part-to-Part[6]						
0 ns Deglitch (Si82FxxAx) Devices	$t_{PSK(PP)}$	MAX{ $\lvert t_{PLHx}-t_{PLHy}\rvert$, $\lvert t_{PHLx}-t_{PHLy}\rvert$ }	—	—	5.00	ns
30 ns Deglitch (Si82FxxBx) Devices			—	—	8.00	ns
90 ns Deglitch (Si82FxxEx) Devices			—	—	20.0	ns
Output Rise Time[2]						
4 V UVLO (Si82FxxxGx) Devices	t_{RA}, t_{RB}	Speed 7, VDDA/B = 6 V, C_L = 2.2 nF	—	16.0	—	ns
8 V UVLO (Si82FxxxBx) Devices		Speed 7, VDDA/B = 10 V, C_L = 2.2 nF	—	16.0	—	ns
12 V UVLO (Si82FxxxCx) Devices		Speed 7, VDDA/B= 15 V, C_L = 2.2 nF	—	17.0	—	ns
15 V UVLO (Si82FxxxEx) Devices		Speed 7, VDDA/B= 18 V, C_L = 2.2 nF	—	17.0	—	ns
Output Fall Time[2]						
4 V UVLO (Si82FxxxGx) Devices	t_{FA}, t_{FB}	Speed 7, VDDA/B= 6 V, C_L = 2.2 nF	—	22.0	—	ns
8 V UVLO (Si82FxxxBx) Devices		Speed 7, VDDA/B= 10 V, C_L = 2.2 nF	—	19.0	—	ns
12 V UVLO (Si82FxxxCx) Devices		Speed 7, VDDA/B= 15 V, C_L = 2.2 nF	—	18.0	—	ns
15 V UVLO (Si82FxxxEx) Devices		Speed 7, VDDA/B= 18 V, C_L = 2.2 nF	—	20.0	—	ns
Dead Time Delay[7]	t_{DT}	R_{DT} = 10 kΩ	10.0	20.0	30.0	ns
		R_{DT} = 60 kΩ	—	110	—	ns
		R_{DT} = 110 kΩ	170	200	240	ns
Startup Time[8]	t_{ST}		—	125	—	µs
VDDI Logic Input Power Cycle Time[8]	t_{PCL}		—	60.0	—	µs
VDDI Logic Input Shutdown Time[8]	t_{SDL}		—	90.0	—	µs

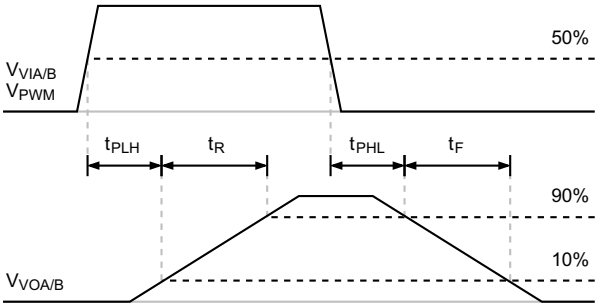
Table 8. Timing Characteristics[1] (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDDA/B = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDDA/B = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

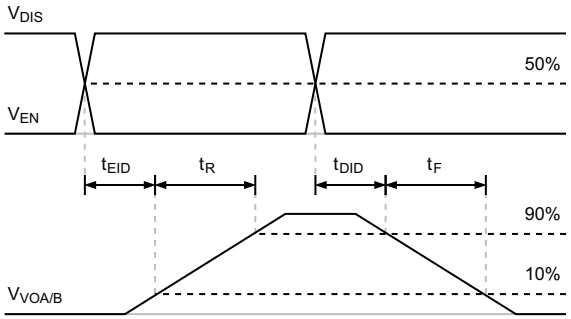
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDDA/B Gate Driver Power Cycle Time[8]	t_{PCGA}, t_{PCGB}		—	125	—	µs
VDDA/B Gate Driver Shutdown Time[8]	t_{SDGA}, t_{SDGB}		—	7.00	—	µs
Common Mode Transient Immunity	CMTI		200	—	—	kV/µs

1. Adding the suffix A/B to any symbol, parameter, or test condition variable denotes that the term applies interchangeably to either gate driver A or gate driver B.
2. See Figure 23, "Control Input Timing Measurements," on page 35 for details.
3. See Figure 24, "Enable or Disable Input Timing Measurements," on page 35 for details.
4. t_{SUD} is measured from the edge of a square wave applied to the input (SPD+ or SPD-) to next change in output (VOA/B) voltage slope. See Figure 25, "Speed Update Delay Timing Measurement," on page 35 for details.
5. $t_{PSK(CC)}$ is the largest absolute value difference in propagation delays between the two channels of a single unit operating at the same supply voltages, load, and ambient temperature. See Figure 26, "Propagation Delay Parameters," on page 35 for details.
6. $t_{PSK(PP)}$ is the largest absolute value difference in propagation delays measured between different channels on different units operating at the same supply voltages, load, and ambient temperature.
7. The dead time pin (DT) can be pulled to VDDI to disable dead time control. Using less than 10 kΩ dead time resistor is not recommended. See Figure 27, "Dead Time Timing Measurement," on page 36 for more information.
8. Startup, power cycle, and shutdown timing are detailed in "4.2. Power Sequence and Timing Behavior" on page 11.



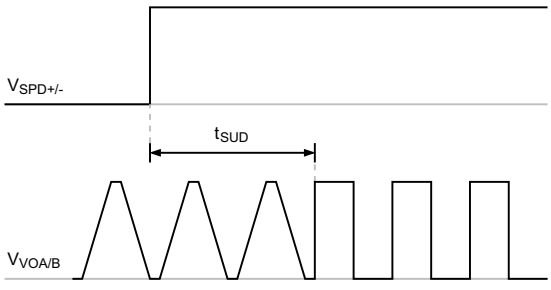
EN = Logic high
DIS = Logic low

Figure 23. Control Input Timing Measurements



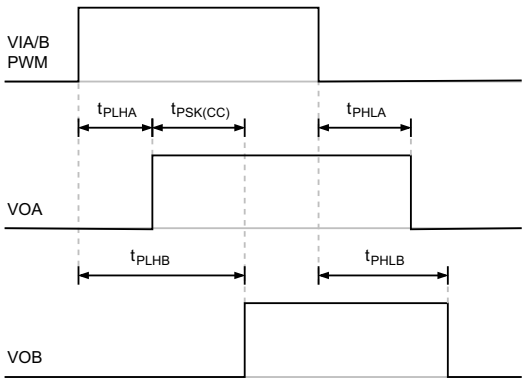
VIA/B or PWM = Logic High

Figure 24. Enable or Disable Input Timing Measurements



VIA/B or PWM = Square wave
EN = Logic high
DIS = Logic low

Figure 25. Speed Update Delay Timing Measurement



EN = Logic high
DIS = Logic low

Figure 26. Propagation Delay Parameters

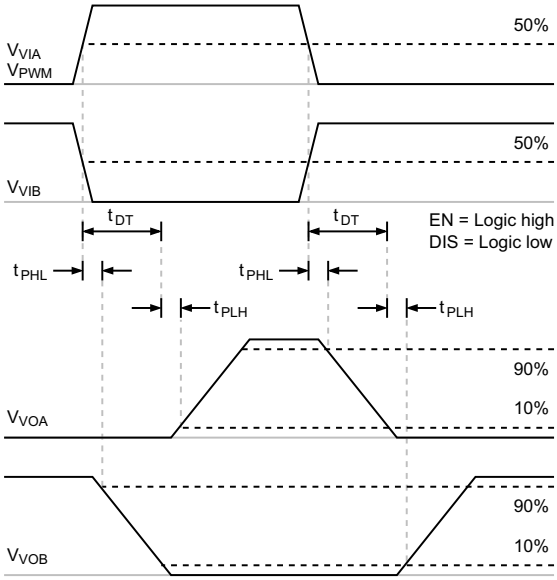


Figure 27. Dead Time Timing Measurement

6.3. Typical Performance Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to the data tables in "6.2. Electrical Characteristics" on page 26 for actual specification limits.

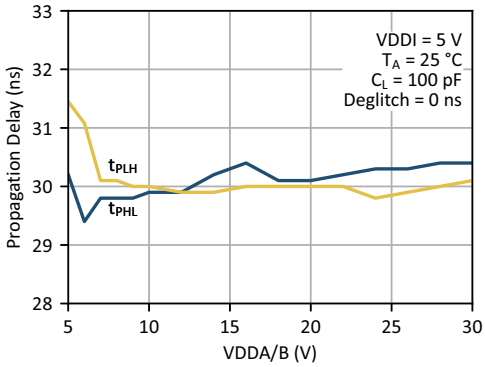


Figure 28. Propagation Delay vs. Gate Driver Supply Voltage

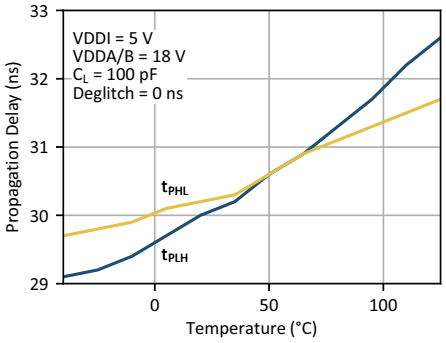


Figure 29. Propagation Delay vs. Ambient Temperature

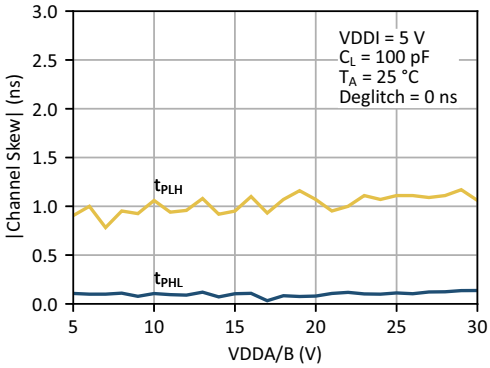


Figure 30. Channel-to-Channel Skew vs. Gate Driver Supply Voltage

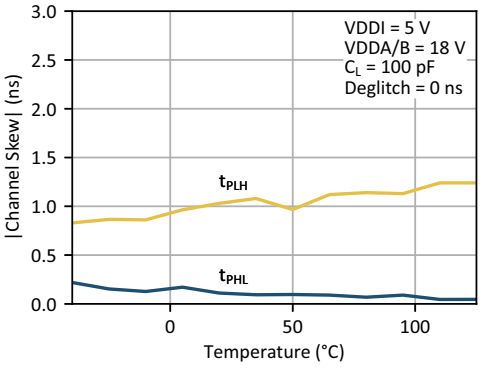


Figure 31. Channel-to-Channel Skew vs. Ambient Temperature

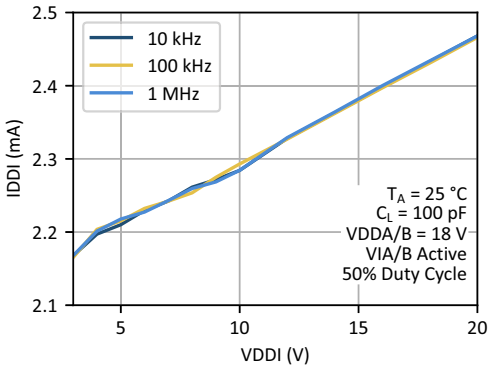


Figure 32. Logic Input Active Supply Current vs. Logic Input Supply Voltage

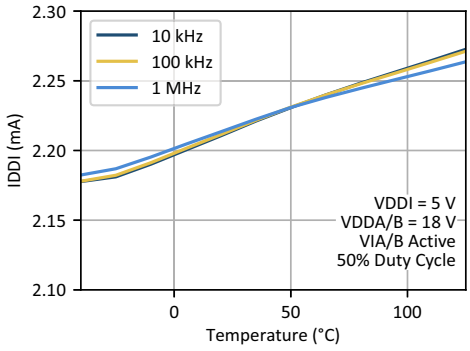


Figure 33. Logic Input Active Supply Current vs. Ambient Temperature

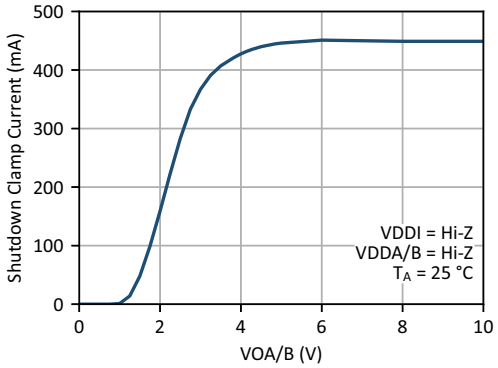


Figure 34. Shutdown Clamp Current vs. Shutdown Clamp Voltage

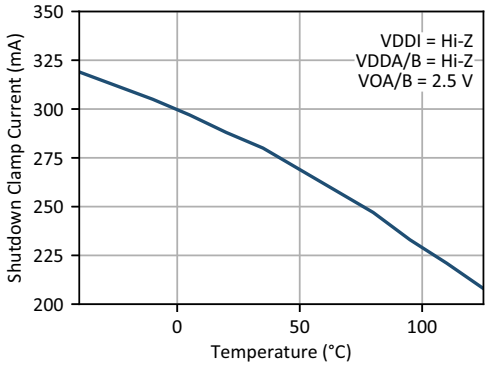


Figure 35. Shutdown Clamp Current vs. Ambient Temperature

6.3.1. 4 V UVLO (Si82FxxxGx) Devices

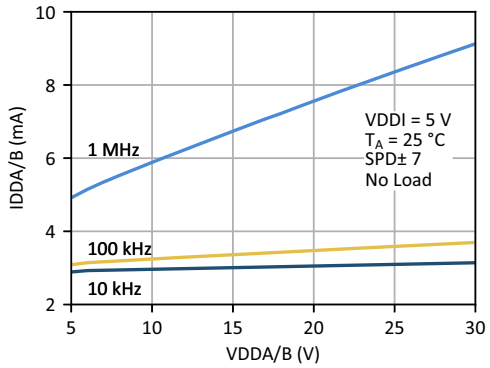


Figure 36. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage

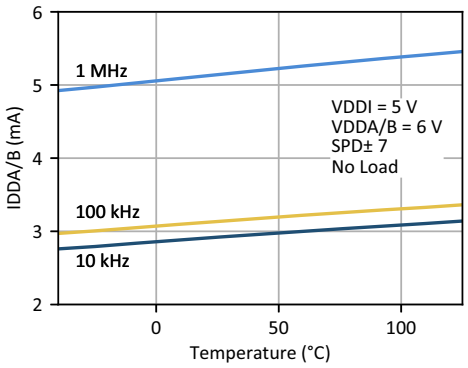


Figure 37. Gate Driver Active Supply Current vs. Ambient Temperature

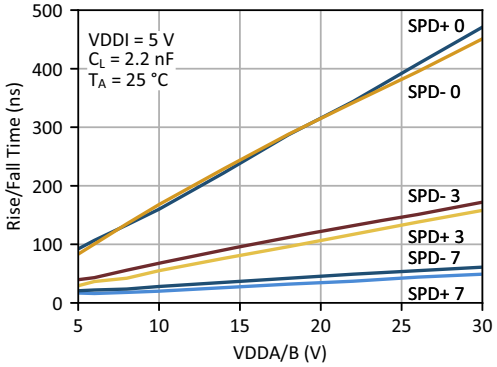


Figure 38. Output Rise/Fall Time vs. Gate Driver Supply Voltage

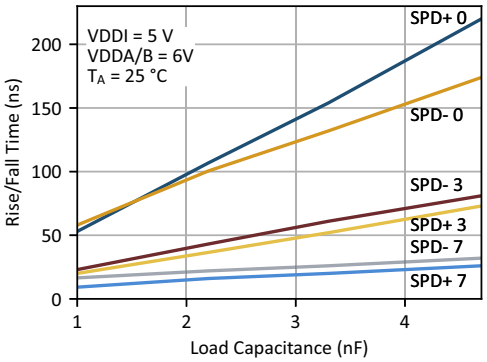


Figure 39. Output Rise/Fall Time vs. Output Load

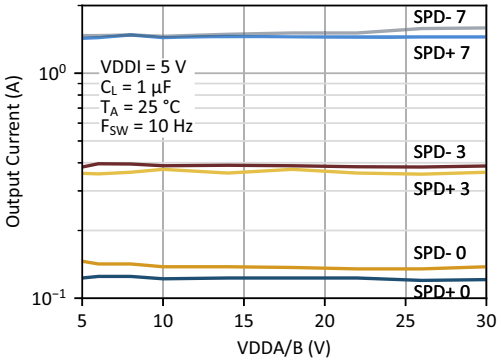


Figure 40. Output Current vs. Gate Driver Supply Voltage

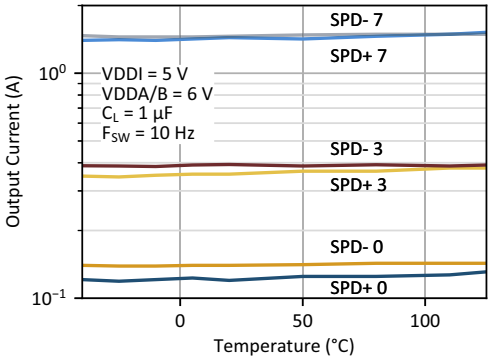


Figure 41. Output Current vs. Ambient Temperature

6.3.2. 8 V UVLO (Si82FxxxBx) Devices

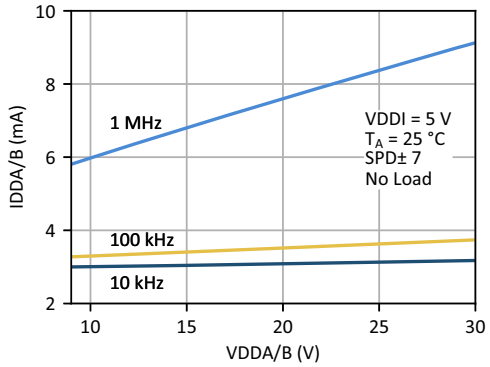


Figure 42. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage

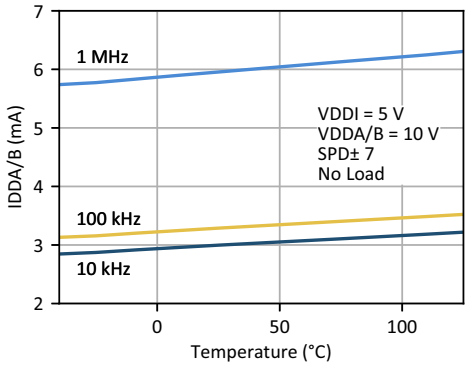


Figure 43. Gate Driver Active Supply Current vs. Ambient Temperature

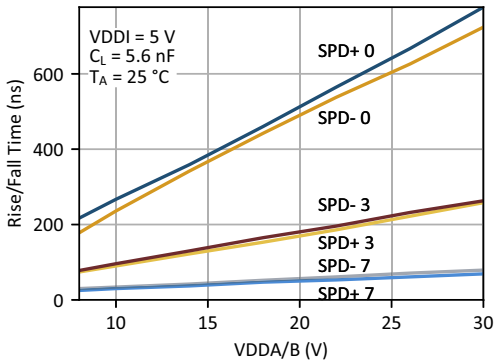


Figure 44. Output Rise/Fall Time vs. Gate Driver Supply Voltage

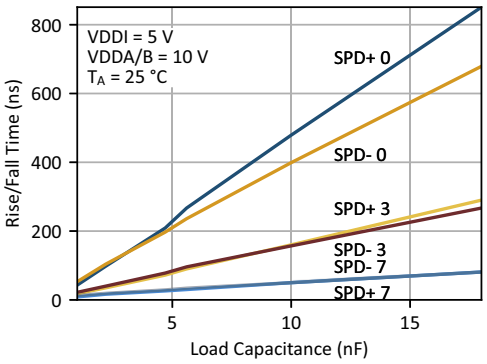


Figure 45. Output Rise/Fall Time vs. Output Load

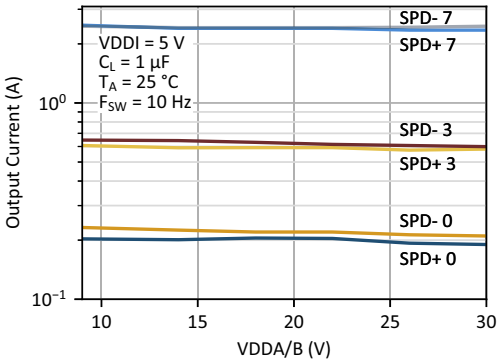


Figure 46. Output Current vs. Gate Driver Supply Voltage

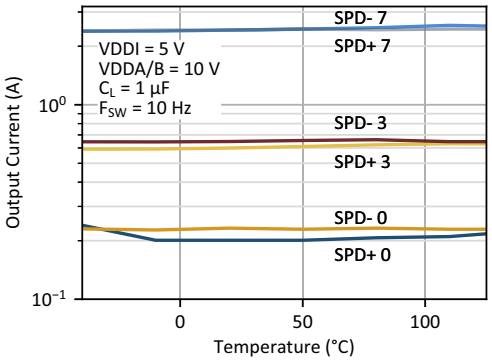


Figure 47. Output Current vs. Ambient Temperature

6.3.3. 12 V UVLO (Si82FxxxCx) Devices

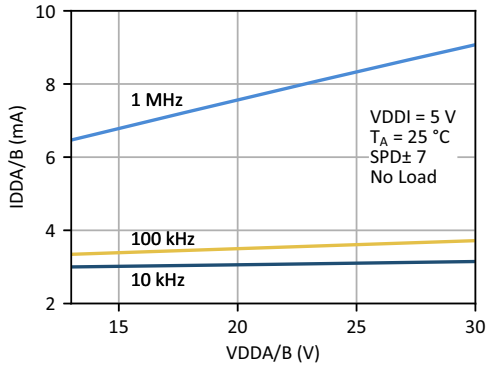


Figure 48. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage

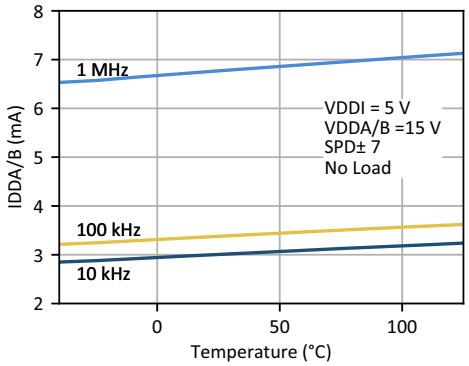


Figure 49. Gate Driver Active Supply Current vs. Ambient Temperature

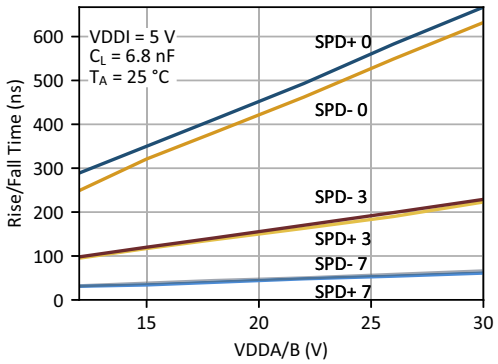


Figure 50. Output Rise/Fall Time vs. Gate Driver Supply Voltage

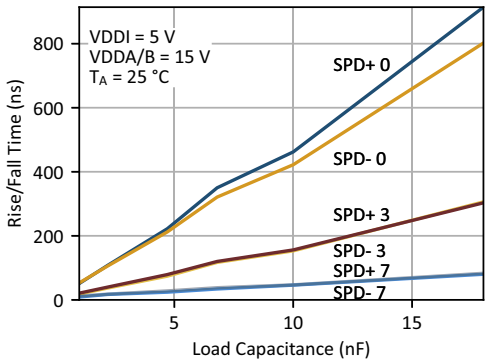


Figure 51. Output Rise/Fall Time vs. Output Load

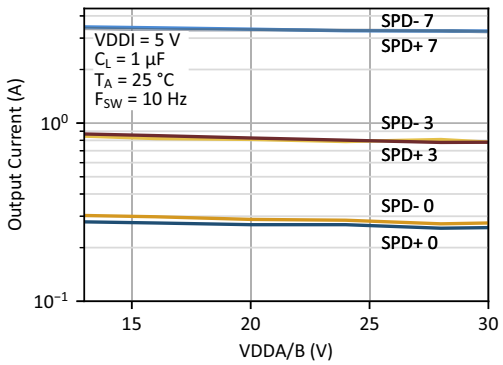


Figure 52. Output Current vs. Gate Driver Supply Voltage

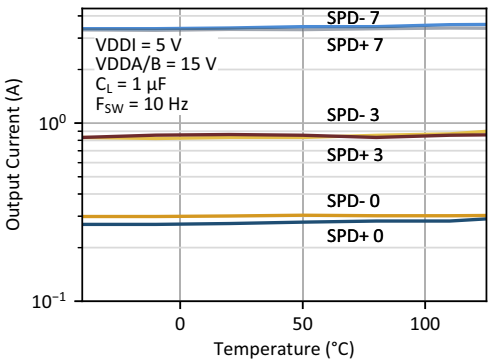


Figure 53. Output Current vs. Ambient Temperature

6.3.4. 15 V UVLO (Si82FxxxEx) Devices

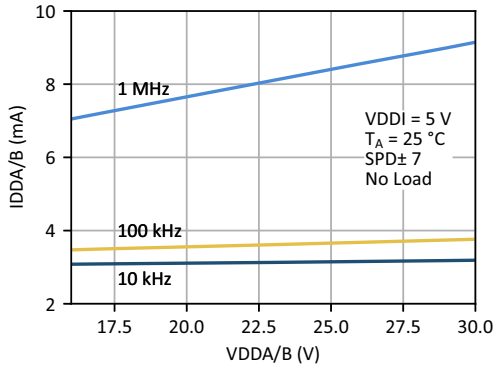


Figure 54. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage

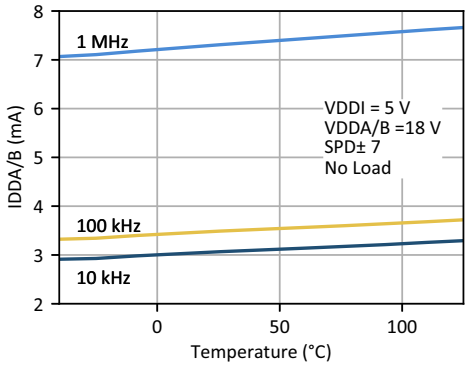


Figure 55. Gate Driver Active Supply Current vs. Ambient Temperature

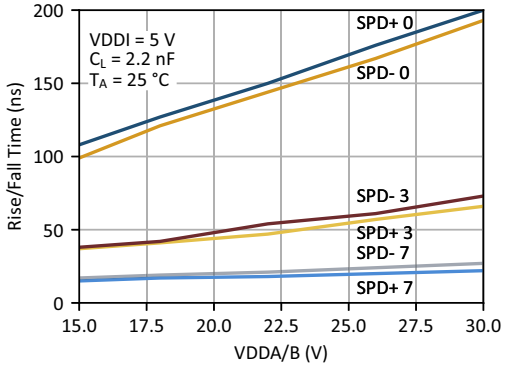


Figure 56. Output Rise/Fall Time vs. Gate Driver Supply Voltage

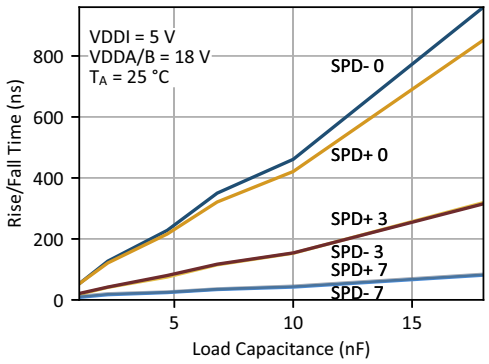


Figure 57. Output Rise/Fall Time vs. Output Load

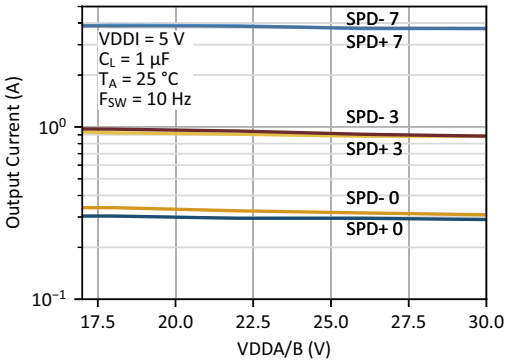


Figure 58. Output Current vs. Gate Driver Supply Voltage

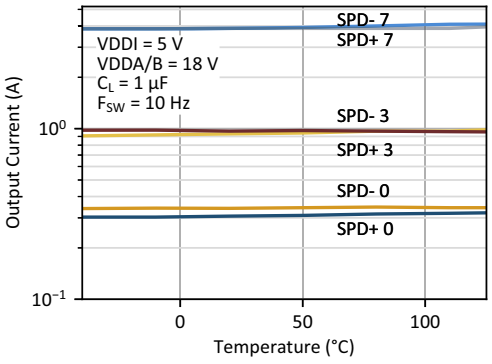


Figure 59. Output Current vs. Ambient Temperature

6.4. Thermal Characteristics

Table 9. Thermal Characteristics

Parameter	Symbol	Test Condition	NB SOIC-16	WB SOIC-14	Unit
Thermal Resistance					
Junction-to-Ambient	θ_{JA}	4-layer, 2s2p JEDEC test board	63	59	°C/W
Characterization Parameter					
Junction-to-Top	Ψ_{JT}	4-layer, 2s2p JEDEC test board	7.5	14	°C/W
Junction-to-Board	Ψ_{JB}	4-layer, 2s2p JEDEC test board	31	34	°C/W

6.5. Safety Certifications and Specifications

Table 10. Regulatory Information[1]

CSA
The Si82Fx is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 250 V_{RMS} working voltage and two means of patient protection (MOPP).
VDE
The Si82Fx is certified under VDE. For more details, see File 5028467.
60747-17: Up to 2121 V_{PEAK} for reinforced insulation working voltage.
UL
The Si82Fx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 6.0 kV_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si82Fx is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see "10. Ordering Guide" on page 55.

Table 11. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			NB SOIC-16	WB SOIC-14	
Nominal External Air Gap (Clearance)	CLR		3.90	8.00	mm
Nominal External Tracking (Creepage)	CRP		3.90	8.00	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.036	0.036	mm
Tracking Resistance	CTI or PTI	IEC60112	600	600	V_{RMS}
Erosion Depth	ED		0.031	0.019	mm
Resistance (Input-Output)[1]	R_{IO}	Test voltage = 500 V, 25 °C	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	1.10	1.00	pF
Input Capacitance[2]	C_I	f = 100 kHz	2.00	2.00	pF

1. To determine resistance and capacitance, the device is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal, and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 12. IEC-60664-1 Ratings

Parameter	Test Conditions	Specification	
		NB SOIC-16	WB SOIC-14
Material group		I	I
Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV
	Rated mains voltage ≤ 300 V_{RMS}	I-III	I-IV
	Rated mains voltage ≤ 600 V_{RMS}	I-II	I-IV
	Rated mains voltage ≤ 1000 V_{RMS}	I	I-III

Table 13. IEC60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			NB SOIC-16	WB SOIC-14	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	445	1500	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	630	2121	V_{PEAK}
Apparent charge	Q_{PD}	Method b: At routine test (100% production) and preconditioning (type test); V_{INI} = 1.2 x V_{IOTM}, t_{INI} = 1 s; $V_{PD(M)}$ = 1.875 x V_{IORM}, t_M = 1 s (method b1) or $V_{PD(M)}$ = V_{INI}, t_M = t_{INI} (method b2)	≤ 5	≤ 5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	5302	8484	V_{PEAK}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile (qualification)	10400	10400	V_{PEAK}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile (qualification)	5000	8000	V_{PEAK}
Isolation resistance	R_{IO_S}	T_{AMB} = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 14. UL1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			NB SOIC-16	WB SOIC-14	
Maximum withstanding isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)	3750	6000	V_{RMS}

Table 15. IEC Safety Limiting Values

Parameter	Symbol	Test Condition	Max[1]		Unit
			NB SOIC-16	WB SOIC-14	
Safety Temperature	T_S		150	150	°C
Safety Input, Output, or Supply Current	I_S	Refer to $Ø_{JA}$ in "6.4. Thermal Characteristics" on page 43; VDDI = 5 V, VDDA/B = 30 V, T_J = 150 °C, T_A = 25 °C	66	70	mA
Safety Input, Output, or Total Power	P_S		1.98	2.11	W

1. Maximum value allowed in the event of a failure; also see the temperature derating curves below.

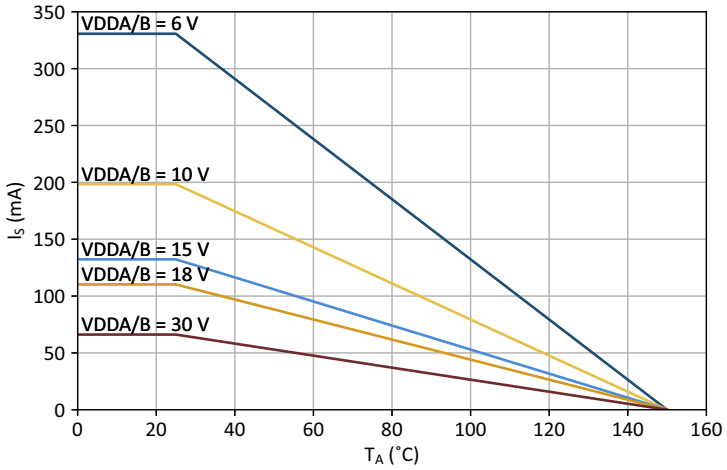


Figure 60. NB SOIC-16 Safety Current vs. Ambient Temperature Derating Curve

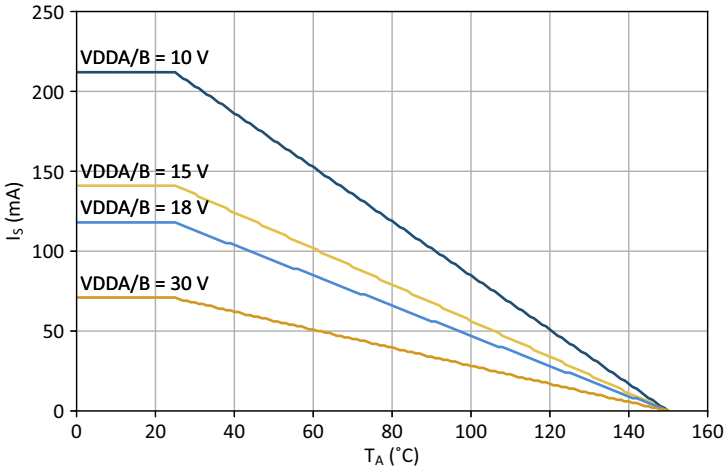


Figure 61. WB SOIC-14 Safety Current vs. Ambient Temperature Derating Curve

7. Package Drawings

7.1. NB SOIC-16 Package Drawing

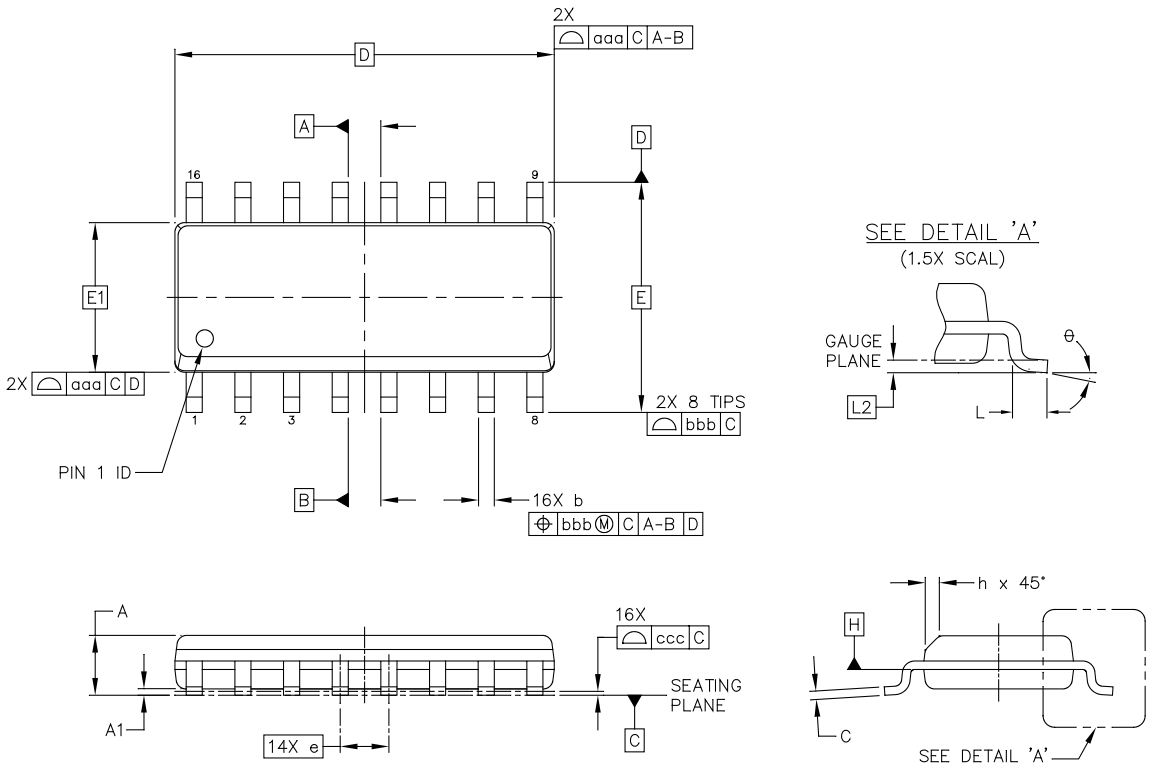


Figure 62. NB SOIC-16 Package Drawing

Table 16. NB SOIC-16 Package Drawing Dimensions[1,2,3,4]

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°

Table 16. NB SOIC-16 Package Drawing Dimensions[1,2,3,4] (Continued)

Dimension	Min	Max
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.2. WB SOIC-14 Package Drawing

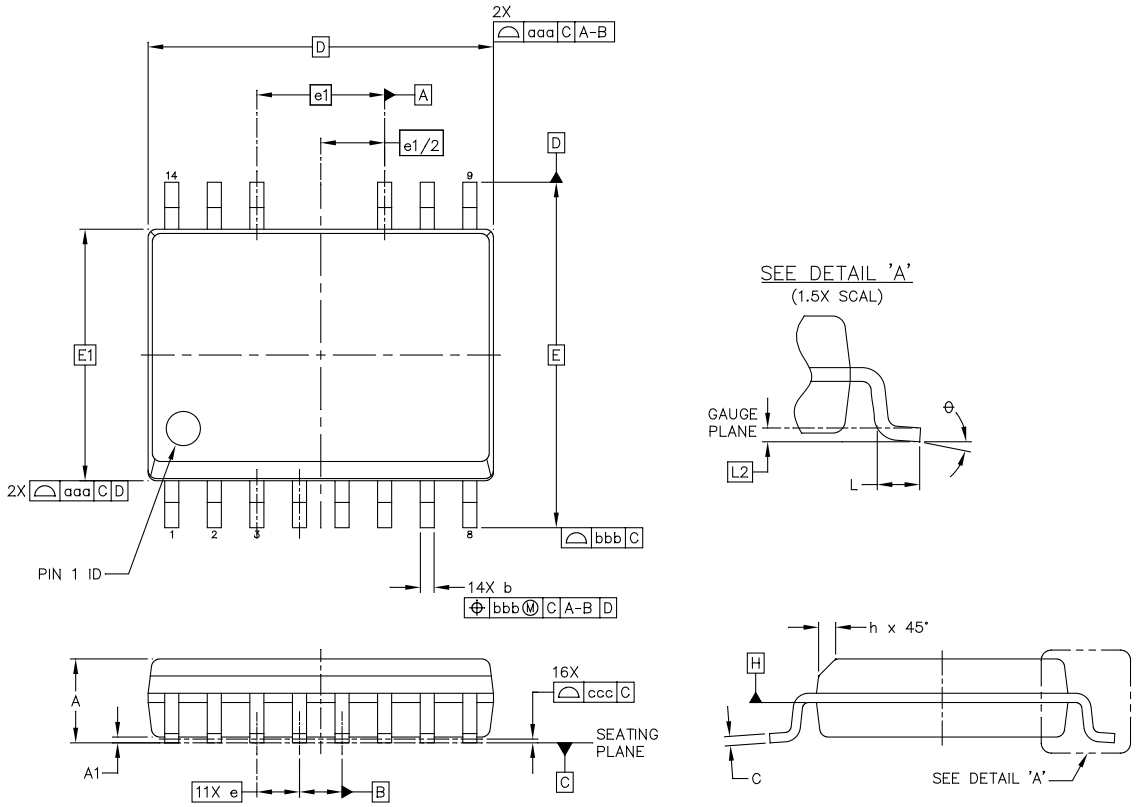


Figure 63. WB SOIC-14 Package Drawing

Table 17. WB SOIC-14 Package Drawing Dimensions[1,2,3]

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
b	0.35	0.49
c	0.23	0.32
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
e1	3.81 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.75
θ	0°	8°

Table 17. WB SOIC-14 Package Drawing Dimensions[1,2,3] (Continued)

Dimension	Min	Max
aaa	0.10	
bbb	0.25	
ccc	0.10	
ddd	0.25	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per the JEDEC J-STD-020C specification for small body, lead-free components.

8. Land Patterns

8.1. NB SOIC-16 Land Pattern

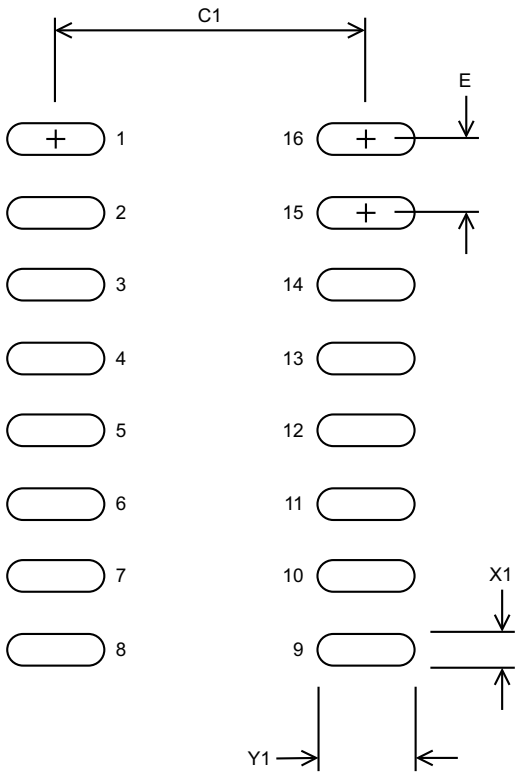


Figure 64. NB SOIC-16 Land Pattern

Table 18. NB SOIC-16 PCB Land Pattern Dimension[1,2]

Dimension	Feature	mm
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8.2. WB SOIC-14 Land Pattern

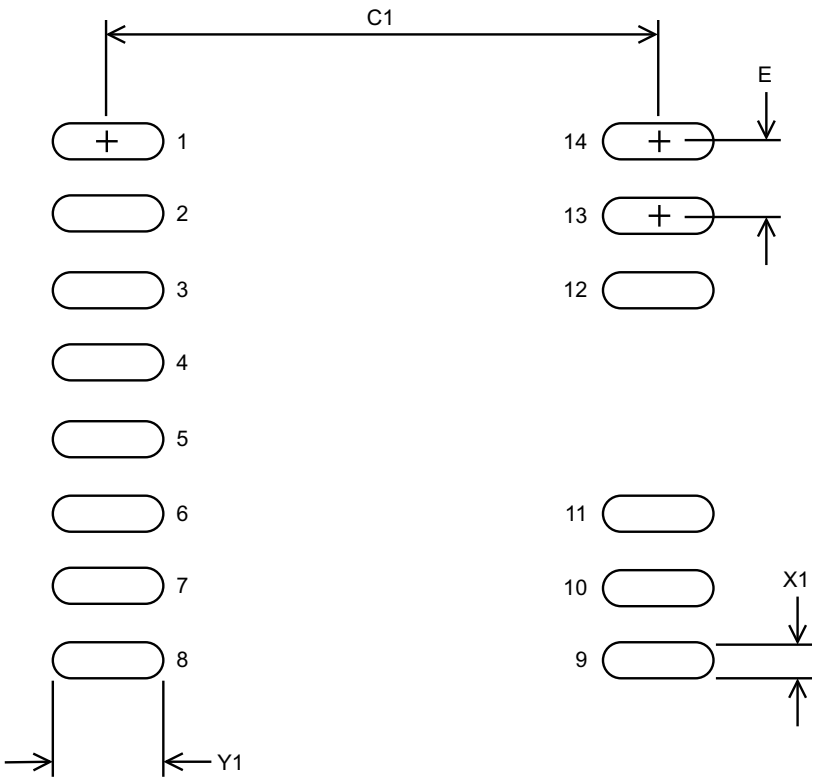


Figure 65. WB SOIC-14 PCB Land Pattern

Table 19. WB SOIC-14 PCB Land Pattern Dimensions[1,2]

Dimension	Feature	mm
C1	Pad Column Spacing	9.80
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.60

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Top Markings

9.1. NB SOIC-16 Top Marking

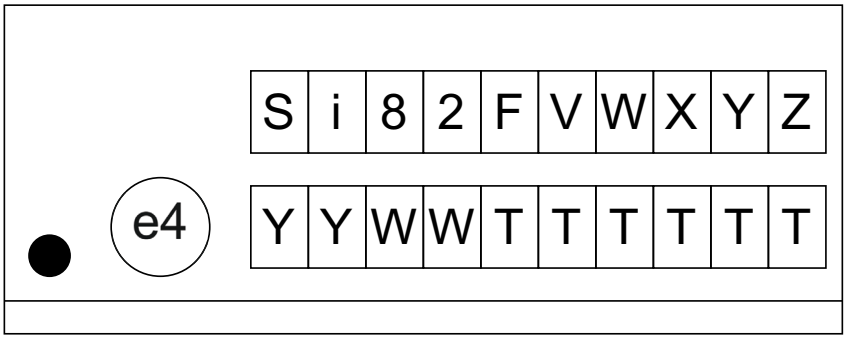


Figure 66. 16-Pin Narrow-Body SOIC Top Marking

Table 20. 16-Pin Narrow-Body SOIC Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See "10. Ordering Guide" on page 55 for more information)	Si82F = Two-channel Performance IsoDriver product series V = Input Pinout 2 = VIA, VIB, DT and DIS inputs (Universal configuration) 3 = VIA, VIB, DT and EN inputs (Universal configuration) 8 = PWM, DT, and DIS inputs (High-Side/Low-Side configuration) 9 = PWM, DT, and EN inputs (High-Side/Low-Side configuration) W = Output Pinout 9 = Combined Source/Sink Driver Output X = Input Configuration A = No deglitch filter B = 30 ns deglitch filter E = 90 ns deglitch filter Y = Output Configuration G = 4 V UVLO B = 8 V UVLO C = 12 V UVLO E = 15 V UVLO Z = Isolation Rating C = 3.75 kV_{RMS}
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg. Trace Code	Manufacturing Traceability Code The Manufacturing Traceability Code represented by "TTTTTT" contains, as its first character, a letter in the range A through M to indicate Industrial-Grade, or a letter in the range N through Z to indicate Automotive-Grade.
	e4 circle is 1.3 mm diameter	The "e4" symbol indicates Pb-free lead finish.

9.2. WB SOIC-14 Top Marking

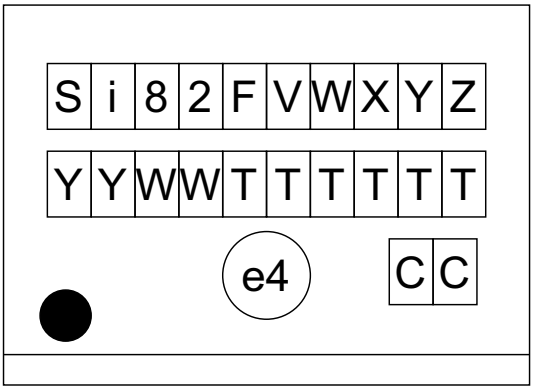


Figure 67. 14-Pin Wide Body SOIC Top Marking

Table 21. 14-Pin Wide Body SOIC Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See "10. Ordering Guide" on page 55 for more information)	Si82F = Two-channel Performance IsoDriver product series V = Input Pinout 2 = VIA, VIB, DT and DIS inputs (Universal configuration) 3 = VIA, VIB, DT and EN inputs (Universal configuration) 8 = PWM, DT, and DIS inputs (High-Side/Low-Side configuration) 9 = PWM, DT, and EN inputs (High-Side/Low-Side configuration) W = Output Pinout 9 = Combined Source/Sink Driver Output X = Input Configuration A = No deglitch filter B = 30 ns deglitch filter E = 90 ns deglitch filter Y = Output Configuration B = 8 V UVLO C = 12 V UVLO E = 15 V UVLO Z = Isolation Rating E = 6.0 kV_{RMS}
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg. Trace Code	Manufacturing Traceability Code The Manufacturing Traceability Code represented by "TTTTTT" contains, as its first character, a letter in the range A through M to indicate Industrial-Grade, or a letter in the range N through Z to indicate Automotive-Grade.
Line 3 Marking:	e4 circle is 1.7 mm diameter	The "e4" symbol indicates Pb-free lead finish.
	CC = Country of Origin ISO Code Abbreviation	TW = Taiwan TH = Thailand

10. Ordering Guide

Table 22. Si82Fx Ordering Guide[1,2,3,4,5,6]

Ordering Part Number (OPN)	Automotive OPN	Inputs	Configuration	Enable/ Disable	Deglitch Filter	Undervoltage Lockout (UVLO)	Isolation Rating	Package Type
NB SOIC-16 Package Options								
Si82F29AGC-IS1	Si82F29AGC-AS1	VIA, VIB	Universal	Disable	NA	4 V	3.75 kV_{RMS}	NB SOIC-16
Si82F29ABC-IS1	Si82F29ABC-AS1	VIA, VIB	Universal	Disable	NA	8 V	3.75 kV_{RMS}	NB SOIC-16
Si82F29ACC-IS1	Si82F29ACC-AS1	VIA, VIB	Universal	Disable	NA	12 V	3.75 kV_{RMS}	NB SOIC-16
Si82F29AEC-IS1	Si82F29AEC-AS1	VIA, VIB	Universal	Disable	NA	15 V	3.75 kV_{RMS}	NB SOIC-16
Si82F39AGC-IS1	Si82F39AGC-AS1	VIA, VIB	Universal	Enable	NA	4 V	3.75 kV_{RMS}	NB SOIC-16
Si82F39ABC-IS1	Si82F39ABC-AS1	VIA, VIB	Universal	Enable	NA	8 V	3.75 kV_{RMS}	NB SOIC-16
Si82F39ACC-IS1	Si82F39ACC-AS1	VIA, VIB	Universal	Enable	NA	12 V	3.75 kV_{RMS}	NB SOIC-16
Si82F39AEC-IS1	Si82F39AEC-AS1	VIA, VIB	Universal	Enable	NA	15 V	3.75 kV_{RMS}	NB SOIC-16
Si82F39BGC-IS1	Si82F39BGC-AS1	VIA, VIB	Universal	Enable	30 ns	4 V	3.75 kV_{RMS}	NB SOIC-16
Si82F39BBC-IS1	Si82F39BBC-AS1	VIA, VIB	Universal	Enable	30 ns	8 V	3.75 kV_{RMS}	NB SOIC-16
Si82F39BCC-IS1	Si82F39BCC-AS1	VIA, VIB	Universal	Enable	30 ns	12 V	3.75 kV_{RMS}	NB SOIC-16
Si82F39BEC-IS1	Si82F39BEC-AS1	VIA, VIB	Universal	Enable	30 ns	15 V	3.75 kV_{RMS}	NB SOIC-16
Si82F39ECC-IS1	Si82F39ECC-AS1	VIA, VIB	Universal	Enable	90 ns	12 V	3.75 kV_{RMS}	NB SOIC-16
Si82F39EEC-IS1	Si82F39EEC-AS1	VIA, VIB	Universal	Enable	90 ns	15 V	3.75 kV_{RMS}	NB SOIC-16
Si82F89AGC-IS1	Si82F89AGC-AS1	PWM	High-Side/Low-Side	Disable	NA	4 V	3.75 kV_{RMS}	NB SOIC-16
Si82F89ABC-IS1	Si82F89ABC-AS1	PWM	High-Side/Low-Side	Disable	NA	8 V	3.75 kV_{RMS}	NB SOIC-16
Si82F89ACC-IS1	Si82F89ACC-AS1	PWM	High-Side/Low-Side	Disable	NA	12 V	3.75 kV_{RMS}	NB SOIC-16
Si82F89AEC-IS1	Si82F89AEC-AS1	PWM	High-Side/Low-Side	Disable	NA	15 V	3.75 kV_{RMS}	NB SOIC-16
Si82F99AGC-IS1	Si82F99AGC-AS1	PWM	High-Side/Low-Side	Enable	NA	4 V	3.75 kV_{RMS}	NB SOIC-16
Si82F99ABC-IS1	Si82F99ABC-AS1	PWM	High-Side/Low-Side	Enable	NA	8 V	3.75 kV_{RMS}	NB SOIC-16
Si82F99ACC-IS1	Si82F99ACC-AS1	PWM	High-Side/Low-Side	Enable	NA	12 V	3.75 kV_{RMS}	NB SOIC-16
Si82F99AEC-IS1	Si82F99AEC-AS1	PWM	High-Side/Low-Side	Enable	NA	15 V	3.75 kV_{RMS}	NB SOIC-16
Si82F99BGC-IS1	Si82F99BGC-AS1	PWM	High-Side/Low-Side	Enable	30 ns	4 V	3.75 kV_{RMS}	NB SOIC-16
Si82F99BBC-IS1	Si82F99BBC-AS1	PWM	High-Side/Low-Side	Enable	30 ns	8 V	3.75 kV_{RMS}	NB SOIC-16
Si82F99BCC-IS1	Si82F99BCC-AS1	PWM	High-Side/Low-Side	Enable	30 ns	12 V	3.75 kV_{RMS}	NB SOIC-16
Si82F99BEC-IS1	Si82F99BEC-AS1	PWM	High-Side/Low-Side	Enable	30 ns	15 V	3.75 kV_{RMS}	NB SOIC-16
Si82F99ECC-IS1	Si82F99ECC-AS1	PWM	High-Side/Low-Side	Enable	90 ns	12 V	3.75 kV_{RMS}	NB SOIC-16
Si82F99EEC-IS1	Si82F99EEC-AS1	PWM	High-Side/Low-Side	Enable	90 ns	15 V	3.75 kV_{RMS}	NB SOIC-16

Table 22. Si82Fx Ordering Guide[1,2,3,4,5,6]

Ordering Part Number (OPN)	Automotive OPN	Inputs	Configuration	Enable/ Disable	Deglitch Filter	Undervoltage Lockout (UVLO)	Isolation Rating	Package Type
WB SOIC-14 Package Options								
Si82F29ABE-IS3	Si82F29ABE-AS3	VIA, VIB	Universal	Disable	NA	8 V	6 kV_{RMS}	WB SOIC-14
Si82F29ACE-IS3	Si82F29ACE-AS3	VIA, VIB	Universal	Disable	NA	12 V	6 kV_{RMS}	WB SOIC-14
Si82F29AEE-IS3	Si82F29AEE-AS3	VIA, VIB	Universal	Disable	NA	15 V	6 kV_{RMS}	WB SOIC-14
Si82F39ABE-IS3	Si82F39ABE-AS3	VIA, VIB	Universal	Enable	NA	8 V	6 kV_{RMS}	WB SOIC-14
Si82F39ACE-IS3	Si82F39ACE-AS3	VIA, VIB	Universal	Enable	NA	12 V	6 kV_{RMS}	WB SOIC-14
Si82F39AEE-IS3	Si82F39AEE-AS3	VIA, VIB	Universal	Enable	NA	15 V	6 kV_{RMS}	WB SOIC-14
Si82F39BBE-IS3	Si82F39BBE-AS3	VIA, VIB	Universal	Enable	30 ns	8 V	6 kV_{RMS}	WB SOIC-14
Si82F39BCE-IS3	Si82F39BCE-AS3	VIA, VIB	Universal	Enable	30 ns	12 V	6 kV_{RMS}	WB SOIC-14
Si82F39BEE-IS3	Si82F39BEE-AS3	VIA, VIB	Universal	Enable	30 ns	15 V	6 kV_{RMS}	WB SOIC-14
Si82F39ECE-IS3	Si82F39ECE-AS3	VIA, VIB	Universal	Enable	90 ns	12 V	6 kV_{RMS}	WB SOIC-14
Si82F39EEE-IS3	Si82F39EEE-AS3	VIA, VIB	Universal	Enable	90 ns	15 V	6 kV_{RMS}	WB SOIC-14
Si82F89ABE-IS3	Si82F89ABE-AS3	PWM	High-Side/Low-Side	Disable	NA	8 V	6 kV_{RMS}	WB SOIC-14
Si82F89ACE-IS3	Si82F89ACE-AS3	PWM	High-Side/Low-Side	Disable	NA	12 V	6 kV_{RMS}	WB SOIC-14
Si82F89AEE-IS3	Si82F89AEE-AS3	PWM	High-Side/Low-Side	Disable	NA	15 V	6 kV_{RMS}	WB SOIC-14
Si82F99ABE-IS3	Si82F99ABE-AS3	PWM	High-Side/Low-Side	Enable	NA	8 V	6 kV_{RMS}	WB SOIC-14
Si82F99ACE-IS3	Si82F99ACE-AS3	PWM	High-Side/Low-Side	Enable	NA	12 V	6 kV_{RMS}	WB SOIC-14
Si82F99AEE-IS3	Si82F99AEE-AS3	PWM	High-Side/Low-Side	Enable	NA	15 V	6 kV_{RMS}	WB SOIC-14
Si82F99BBE-IS3	Si82F99BBE-AS3	PWM	High-Side/Low-Side	Enable	30 ns	8 V	6 kV_{RMS}	WB SOIC-14
Si82F99BCE-IS3	Si82F99BCE-AS3	PWM	High-Side/Low-Side	Enable	30 ns	12 V	6 kV_{RMS}	WB SOIC-14
Si82F99BEE-IS3	Si82F99BEE-AS3	PWM	High-Side/Low-Side	Enable	30 ns	15 V	6 kV_{RMS}	WB SOIC-14
Si82F99ECE-IS3	Si82F99ECE-AS3	PWM	High-Side/Low-Side	Enable	90 ns	12 V	6 kV_{RMS}	WB SOIC-14
Si82F99EEE-IS3	Si82F99EEE-AS3	PWM	High-Side/Low-Side	Enable	90 ns	15 V	6 kV_{RMS}	WB SOIC-14

1. “Si” and “SI” are used interchangeably.
2. An "R" at the end of the Ordering Part Number indicates tape and reel packaging option.
3. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
4. All High-Side/Low-Side drivers have built-in overlap protection. Universal drivers have built-in overlap protection, but the feature can be disabled by connecting the DT input pin to VDDI. See “4.5. Dead Time Control and Overlap Protection” on page 13.
5. Automotive-Grade devices (with an “-A” suffix) are identical in construction materials and electrical parameters to their Industrial Grade (with an “-I” suffix) version counterpart. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In Top Markings, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range A through M to indicate Industrial-Grade, or N through Z to indicate Automotive-Grade.

11. Revision History

Revision	Date	Description	Notes
A	May, 2024	Initial release.	CN0121999

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Skyworks:

SI82F39EEC-IS1R SI82F39ACE-IS3R SI82F89AGC-IS1R SI82F99ECE-IS3 SI82F99BCE-IS3R SI82F29AEE-IS3 SI82F29ABC-IS1 SI82F89ACC-IS1R SI82F89ABE-IS3 SI82F39BCC-IS1R SI82F99BEC-IS1 SI82F99ACE-IS3R SI82F39ECC-IS1R SI82F29AEC-IS1R SI82F99ECE-IS3R SI82F39AEE-IS3 SI82F99ECC-IS1R SI82F99AGC-IS1 SI82F99ACC-IS1 SI82F29ACE-IS3 SI82F89ACE-IS3 SI82F39BCE-IS3 SI82F99AEC-IS1 SI82F39ACC-IS1 SI82F99BBC-IS1 SI82F29AEE-IS3R SI82F99EEE-IS3R SI82F39BGC-IS1 SI82F39ACC-IS1R SI82F39ABC-IS1 SI82F39BBC-IS1R SI82F99BEE-IS3R SI82F39BBE-IS3R SI82F39BEC-IS1 SI82F89AEE-IS3R SI82F99BGC-IS1 SI82F39BBE-IS3 SI82F99BGC-IS1R SI82F39AEE-IS3R SI82F89AEE-IS3 SI82F39AEC-IS1 SI82F99BCC-IS1R SI82F29AGC-IS1R SI82F39ABC-IS1R SI82F99ABE-IS3 SI82F39BEC-IS1R SI82F99ABC-IS1R SI82F39BGC-IS1R SI82F89ABC-IS1 SI82F39BEE-IS3R SI82F99EEC-IS1 SI82F39BBC-IS1 SI82F99BBE-IS3R SI82F39EEE-IS3 SI82F89ABE-IS3R SI82F29ACE-IS3R SI82F99ABE-IS3R SI82F89AEC-IS1R SI82F99EEC-IS1R SI82F89ABC-IS1R SI82F39ECE-IS3R SI82F29ACC-IS1 SI82F29ACC-IS1R SI82F39ACE-IS3 SI82F39ABE-IS3 SI82F99ABC-IS1 SI82F99BEC-IS1R SI82F99EEE-IS3 SI82F39EEE-IS3R SI82F99AEC-IS1R SI82F99AEE-IS3 SI82F29ABE-IS3R SI82F29AEC-IS1 SI82F39AGC-IS1R SI82F29AGC-IS1 SI82F99BCC-IS1 SI82F99BCE-IS3 SI82F39BEE-IS3 SI82F99AEE-IS3R SI82F89ACC-IS1 SI82F99AGC-IS1R SI82F29ABC-IS1R SI82F39ECC-IS1 SI82F99ACC-IS1R SI82F39AEC-IS1R SI82F99BBE-IS3 SI82F89ACE-IS3R SI82F39BCE-IS3R SI82F99BEE-IS3 SI82F39BCC-IS1 SI82F89AEC-IS1 SI82F39ECE-IS3 SI82F99BBC-IS1R SI82F99ECC-IS1 SI82F39EEC-IS1 SI82F99ACE-IS3 SI82F89AGC-IS1 SI82F29ABE-IS3 SI82F39AGC-IS1 SI82F39ABE-IS3R