

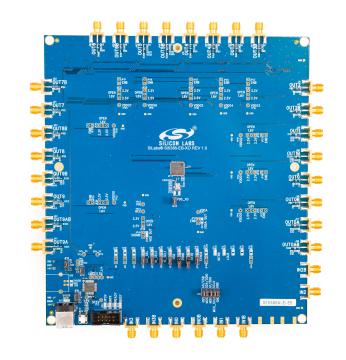
# Si5386 Evaluation Board User's Guide

The Si5386A-E-EB is used for evaluating the Ultra Low Jitter, Any-Frequency, 12-output JESD204B Clock Generator. The Si5386 employs fourth-generation DSPLL technology to enable clock generation for LTE/ JESD204B applications which require the highest level of jitter performance. The Si5386A-E-EB has four independent input clocks and a total of 12 outputs. The Si5386A-E-EB can be easily controlled and configured using Silicon Labs' Clock Builder Pro<sup>®</sup> (CBPro) software tool.

The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "Si5386A-E-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

#### EVB FEATURES

- Powered from USB port or external power supply
- Onboard 54 MHz XO provides holdover mode of operation on the Si5386
- CBPro GUI programmable VDDO supplies allow each of the ten primary outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5386
- SMA connectors for input clocks and output clocks



## 1. Si5386 Functional Block Diagram

Below is a functional block diagram of the Si5386A-E-EB. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See 2. Quick Start and Jumper Defaults or 6.1 Installing ClockBuilder Pro Desktop Software for more information.

Note: All Si5386 schematics, BOMs, User's Guides, and software can be found online at the following link: http://www.silabs.com/si538x-4x-evb

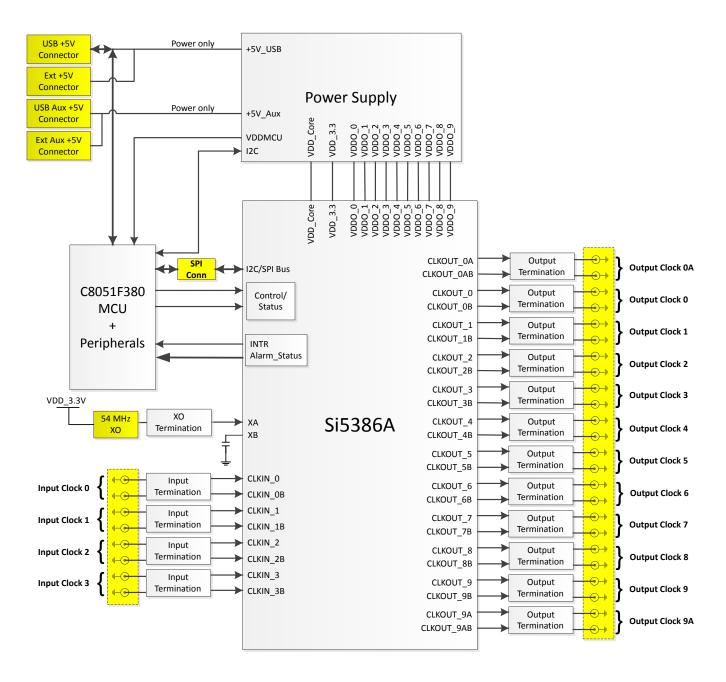


Figure 1.1. Functional Block Diagram of Si5386A-E-EB

# 2. Quick Start and Jumper Defaults

Perform the following steps to quick-start the ClockBuilder<sup>®</sup> Pro software.

- 1. Download and install the ClockBuilder Pro desktop software.
- 2. Connect a USB cable from the Si5386A-E-EB to the PC where the software was installed.
- 3. Confirm jumpers are installed as shown in the table below.
- 4. Launch the ClockBuilder Pro Software.
- 5. You can use ClockBuilder Pro to create, download, and verify a frequency plan on the Si5386A-E-EB.
- 6. Download the Si5386 data sheet for more information or go to Clock Development Tools and search for the latest Si5386 data sheet.

The following table lists the Si5386A-E- EVB jumper defaults.

Table 2.1. Si5386A-E-EVB Jumper Defaults\*

| Location | Туре  | I = Installed | Location | Туре    | I = Installed   |
|----------|-------|---------------|----------|---------|-----------------|
|          |       | O= Open       |          |         | O= Open         |
| JP1      | 2 pin | 0             | JP23     | 2 pin   | 0               |
| JP2      | 2 pin | 0             | JP24     | 3 pin   | all open        |
| JP3      | 2 pin | 0             | JP25     | 2 pin   | 0               |
| JP4      | 2 pin | I             | JP26     | 3 pin   | all open        |
| JP5      | 2 pin | I             | JP27     | 2 pin   | 0               |
| JP6      | 2 pin | I             | JP28     | 3 pin   | all open        |
| JP7      | 2 pin | I             | JP29     | 2 pin   | 0               |
| JP8      | 2 pin | 0             | JP30     | 3 pin   | all open        |
| JP9      | 2 pin | 0             | JP31     | 2 pin   | 0               |
| JP10     | 2 pin | I             | JP32     | 3 pin   | all open        |
| JP13     | 2 pin | 0             | JP33     | 2 pin   | 0               |
| JP14     | 2 pin | I             | JP34     | 3 pin   | all open        |
| JP15     | 3 pin | 1 to 2        | JP35     | 2 pin   | 0               |
| JP16     | 3 pin | 1 to 2        | JP36     | 3 pin   | all open        |
| JP17     | 2 pin | 0             | JP39     | 2 pin   | 0               |
| JP18     | 3 pin | all open      | JP40     | 2 pin   | 0               |
| JP19     | 2 pin | 0             | JP41     | 2 pin   | 0               |
| JP20     | 3 pin | all open      | JP43     | 2 pin   | I               |
| JP21     | 2 pin | 0             |          |         |                 |
| JP22     | 3 pin | all open      | J36      | 5x2 Hdr | All 5 installed |

# 3. Status LEDs

| Location | Silkscreen | Color | Status Function Indication |
|----------|------------|-------|----------------------------|
| D11      | INTRB      | Blue  | DUT Interrupt Active       |
| D12      | LOLB       | Blue  | DUT Loss of Lock Indicator |
| D21      | READY      | Green | MCU Ready                  |
| D22      | 3P3V       | Blue  | DUT +3.3 V is present      |
| D24      | BUSY       | Green | MCU Busy                   |
| D25      | INTR       | Red   | MCU Interrupt active       |
| D26      | VDD DUT    | Blue  | DUT VDD voltage present    |
| D27      | 5VUSBMAIN  | Blue  | Main USB +5 V present      |

#### Table 3.1. Si5386A-E-EVB Status LEDs

D27, D22, and D26 are illuminated when USB +5 V, Si5386 +3.3 V, and Si5386 Output +5 V supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity. D11 and D12 are status indicators from the DUT.

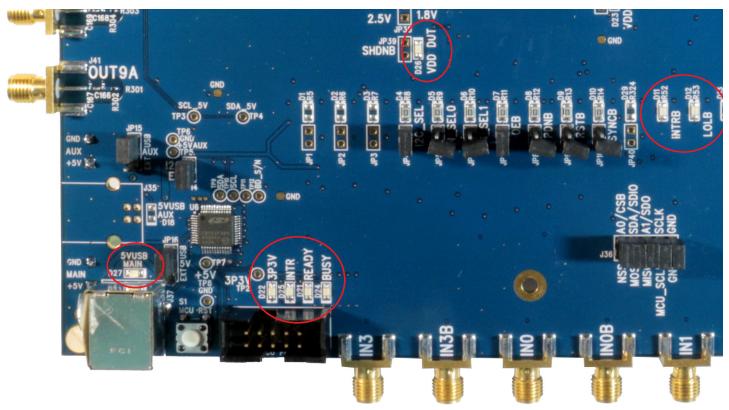


Figure 3.1. Status LEDs

## 4. External Reference Input (XA/XB)

An external XO is used to produce an ultra-low jitter reference clock for the DSPLL and to provide a stable reference for the free-run and holdover modes. The XO footprint on the Si5386A-E-EVB can accommodate both 3.2mm x 5 mm and 2.5 mm x 3.2 mm package sizes. The XO frequency must be 54 MHz (recommended) or 48.0231 MHz for Si5386A devices.

When JP43 is shorted the XO shares the VDD\_3.3V DUT power supply sourced from an on-board ultra low noise LDO. When JP43 is left open an external supply must be used to power the XO. See section 9 for Si5386A-E-EVB schematic details.

Note: The remaining components marked "NI" are not installed.

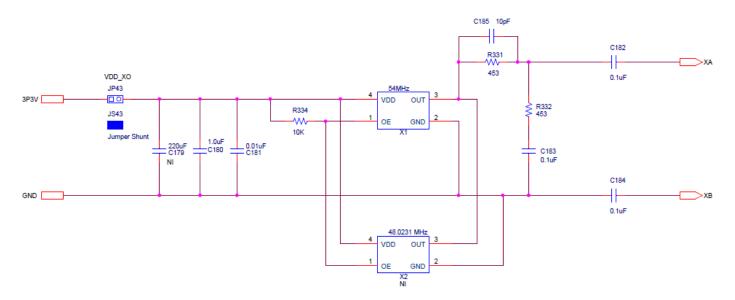


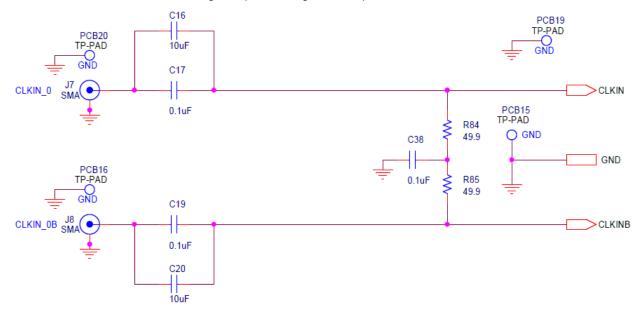
Figure 4.1. External Reference Input Circuit

Si5386 Evaluation Board User's Guide • Clock Input and Output Circuits

# 5. Clock Input and Output Circuits

#### 5.1 Clock Input Circuits (INx/INxB and FB\_IN/FB\_INB)

The Si5386A-E-EB has eight SMA connectors (IN0/IN0B–IN2/IN2B and IN3(FB\_IN)/IN3B(FB\_INB)) for receiving external clock signals. All input clocks are terminated as shown in the figure below. Note input clocks are ac coupled and 50  $\Omega$  terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5386 data sheet.





#### 5.2 Clock Output Circuits (OUTx/OUTxB)

Each of the twenty-four output drivers (12 differential pairs) is ac coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5386A-E-EB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5386A-E-EB, and provide locations on the PCB for optional dc/ac terminations by the end user.

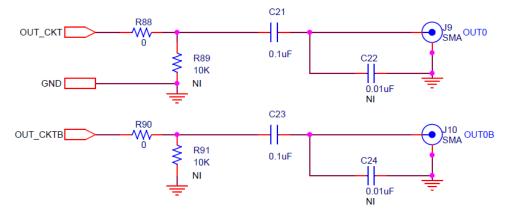


Figure 5.2. Output Clock Termination Circuit

# 6. Using the Si5386 EVB and Installing ClockBuilder Pro Desktop Software

#### 6.1 Installing ClockBuilder Pro Desktop Software

To install the CBPro software on any Windows 7 (or above) PC:

Go to Clock Software Development Tools and download the ClockBuilder Pro software.

Installation instructions, release notes, and a user's guide for ClockBuilder Pro can be found at the download link shown above. Follow the instructions as indicated.

#### 6.2 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software in installed, connect to the EVB with a USB cable as shown below.

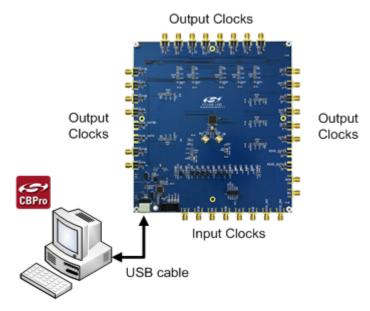


Figure 6.1. EVB Connection Diagram



#### 6.3 Additional Power Supplies

The Si5386A-E-EB comes preconfigured with jumpers installed on JP15 and JP16 (pins 1-2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain +5 V power to all EVB power solely through the J37 USB connector. This setup is the default EVB configuration and is sufficient to configure the device and run multiple clock outputs simultaneously.

In some cases when enabling all outputs or at high output frequencies, the EVB requires more power than a single USB connection can provide. This may result in intermittent device behavior or unexplained increases in jitter/phase-noise. This condition may be checked using the EVB GUI, which is described further below. Selecting the "**All Voltages**" tab of the GUI and clicking on the "**Read All**" button produces a display similar to this one:

| info | DUT SPI     | DUT Settir | ngs Editor            | DUT Register Editor | Phase INC/DEC  | Regulators | All Voltages | GPIO : | Status Re |
|------|-------------|------------|-----------------------|---------------------|----------------|------------|--------------|--------|-----------|
| Vol  | tage @ Regu | lator Pins |                       |                     | Voltage @ Regu | lator      |              |        |           |
|      | V           | DD_PIN     | 2.046 V               | Read                | VI             | DD_REG     | 1.785 V      | Read   | ]         |
|      | VC          | DA_PIN     | 3.282 V               | Read                | VD             | DA_REG     | 3.282 V      | Read   | ]         |
|      | VDD         | OO0_PIN    | 3.927 V               | Read                | VDD            | O0_REG     | 2.482 V      | Read   | ]         |
|      | VDD         | O1_PIN     | 3.179 V               | Read                | VDD            | O1_REG     | 2.501 V      | Read   | ]         |
|      | VDD         | 002_PIN    | 0.000 V               | Read                | VDD            | O2_REG     | 0.000 V 🗌    | Read   |           |
|      | VDD         | O3_PIN     | 3.205 V               | Read                | VDD            | O3_REG     | 2.485 V      | Read   |           |
|      | VDD         | 004_PIN    | 0.000 V               | Read                | VDD            | O4_REG     | 0.000 V 🗌    | Read   | ]         |
|      | VDD         | O5_PIN     | 2.964 V               | Read                | VDD            | O5_REG     | 2.488 V      | Read   |           |
|      | VDD         | DO6_PIN    | 12.000 m              | / Read              | VDD            | O6_REG     | 0.000 V 🗌    | Read   |           |
|      | VDD         | 007_PIN    | 2.948 V               | Read                | VDD            | O7_REG     | 2.481 V 🗌    | Read   |           |
|      | VDE         | 008_PIN    | 12.000 m <sup>1</sup> | / Read              | VDD            | O8_REG     | 2.000 mV 🗌   | Read   |           |
|      | VDE         | 009_PIN    | 2.966 V               | Read                | VDD            | O9_REG     | 2.490 V      | Read   | )         |
| Mis  | c Rails     |            |                       |                     |                |            |              |        |           |
|      |             | RAIL_5V    | 4.735 🗸               | Read                | >              |            |              |        |           |
|      | RA          | IL_3P3V    | 3.306 V               | Read                |                |            |              |        |           |

Figure 6.2. EVB GUI - Power Supply Check

Verify that the "**RAIL\_5V**" measurement shows the EVB voltage > 4.6 V. An EVB voltage lower than this level may cause the issues described above.

In this case, J33 can be used to provide power to the output drivers separately from the main Si5386 device supplies. To make this change, move jumper JP15 to connect pins 2-3 "EXT". Connect J33 to an external 5 V, 0.5A or higher, power source. Make sure that the polarity of the +5 V and GND connections are correct. Verify that the RAIL\_5V voltage is 4.7 V or higher. The EVB should be powered by the USB connector when turning this auxiliary 5 V supply on or off.

See the figure below for the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

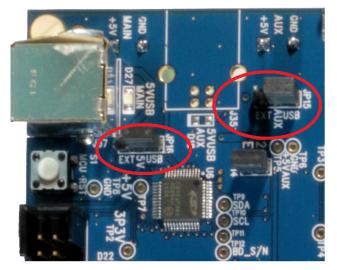


Figure 6.3. JP15-JP16 Standard Jumper Shunt Installation

#### 6.4 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro.

The ClockBuilder Pro installer will install two main applications.

#### Application 1:

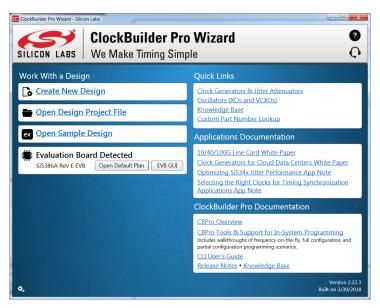


Figure 6.4. ClockBuilder Pro Wizard

Use the CBPro Wizard to do the following:

- · Create a new design.
- · Review or edit an existing design.
- · Export: Create in-system programming files.

#### **Application 2:**

| Si5386A Rev E EVB - ClockBuilder Pro   |                                       |
|--|---------------------------------------|
| File Help  |                                       |
| Info DUT SPI DUT Settings Editor DUT Register Editor Phase INC/DEC Regulators All Voltages GPIO Status | Registers  - Control Registers        |
| Voltage Current Power  | Soft Reset and Calibration            |
| VDD 1.80V 0 0. 1.786 V 262 mA 468 mW Read  | SOFT_RST_ALL                          |
| VDDA 3.30V On 3.281 V 3 mA 10 mW Read  | SOFT_RST                              |
| VDDO0 2.50V 💽 On 2.484 V 48 mA 119 mW Read   | Hard Reset, Sync, &                   |
| VDD01 2.50V 🔽 On 2.504 V 23 mA 58 mW Read  | Power Down                            |
| VDDO2 1.80V V Off OV OmA OmW Read  | HARD_RST                              |
| VDDO3 2.50V 🔽 On 2.485 V 24 mA 60 mW Read  | SYNC                                  |
| VDD04 1.80V 🔮 Off 0 V 0 mA 0 mW Read   | PDN: 0                                |
| VDDO5 2.50V 💽 On 2.485 V 16 mA 40 mW Read  |                                       |
| VDD06 1.80V 💽 Off 0.009 V 0 mA 0 mW Read   |                                       |
| VDD07 2.50V V 00 2.481 V 16 mA 40 mW Read  |                                       |
| VDD08 1.80V 💽 Off 0.009 V 0 mA 0 mW Read   |                                       |
| VDD09 2.50V 💽 On 2.492 V 16 mA 40 mW Read  |                                       |
| All Output 🔽 Select Voltage 💌 Total 408 mA 0.835 W Read All  |                                       |
| Supplies Power On Power Off Compare Design Estimates to Measurements                                   |                                       |
|  |                                       |
|  |                                       |
|  |                                       |
|  |                                       |
| Filtered Auto Scroll: On Insert Marker Clear Copy to Clipboard Pause                                   |                                       |
| Timestamp Source Message   |                                       |
| 16:07:43.846 DUT finished Read_Bytes(TOOL_VERSION) => 0x000000   | A<br>V                                |
| EVB Firmware 1.6   Device: Si5386   DUT Mode: SPI 4-Wire; FW Low-Level Commands                        | ClockBuilder Pro v2.22.3 [2018-03-30] |

Figure 6.5. EVB GUI

Use the EVB GUI to do the following:

- Download configuration to EVB's DUT (Si5386).
- · Control the EVB's regulators.
- Monitor voltage, current, power on the EVB.

#### 6.5 Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5386A-E-EB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-created Default Configuration
- Workflow Scenario #2: Modifying the Default Silicon Labs-created Device Configuration
- Workflow Scenario #3: Testing a User-created Device Configuration

Each is described in more detail in the following sections.

#### 6.6 Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

Verify that the PC and EVB are connected, then launch ClockBuilder Pro by clicking on this icon on your PC's desktop:



Figure 6.6. ClockBuilder Pro Icon

CBPro automatically detects the EVB and device type. When the EVB has been detected, click on the "Open Default Plan" button.

| ClockBuilder Pro Wizard - Silic | on Labs  |  |  |  |
|---------------------------------|--|--|--|--|
| SILICON LABS                    | <b>ClockBuilder Pro</b><br>We Make Timing Simp |  |  |  |
| Work With a Desig               | ŋn   |  |  |  |
| Create New Design               |  |  |  |  |
| 🖶 <u>Open Design</u>            | Project File                                   |  |  |  |
| ex Open Sample                  | <u>e Design</u>                                |  |  |  |
| Si5386A Rev E EVE               |  |  |  |  |

Figure 6.7. CBPro—Open Default Plan Button

Once you open the default plan, a popup will appear.

| Clock | xBuilder Pro v2.22.3  |
|-------|---|
| 0     | Write Design to EVB?<br>The EVB may be out-of-sync with your design. Would you like to write<br>your design to the EVB? |
|       | Yes No  |

Figure 6.8. CBPro—Write Design Dialog

Select "Yes" to write the default plan to the Si5386 device mounted on your EVB. This ensures the device on the EVB is configured with the latest parameters from Silicon Labs.

| 🔝 Si5386A Design Write       | Ca two |  |
|------------------------------|--------|--|
| Writing Si5386A Design to EV | В      |  |
| Address 0x025D               |        |  |
|                              |        |  |
|                              |        |  |

Figure 6.9. CBPro—Write Progress Window

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown in the figure below.

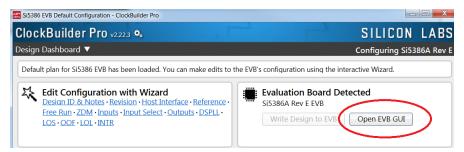


Figure 6.10. CBPro-Open EVB GUI Button

The EVB GUI window will appear on the desktop. Note all power supplies on the "**Regulators**" tab will be set to the values defined in the device's default CBPro project, as shown in the figure below.

| ile   H |          |                     |                 |     |                 |                |              |              |                 |
|---------|----------|---------------------|-----------------|-----|-----------------|----------------|--------------|--------------|-----------------|
| info    | DUT SPI  | DUT Settings Editor | DUT Register Ed | tor | Phase INC/DEC   | Regulators     | All Voltages | GPIO         | Status Register |
|         |          |                     | Volta           | ige | Current         | Power          |              |              |                 |
|         | VD       | D 1.80V             | On 1.78         | 5 V | 262 mA          | 468 mW         | Read         |              |                 |
|         | VDD      | A 3.30V             | On 3.28         | ı v | 3 mA            | 10 mW          | Read         |              |                 |
|         | VDDO     | 0 2.50V 🔽           | On 2.48         | 4 V | 48 mA           | 119 mW         | Read         |              |                 |
|         | VDDO     | 1 2.50V 🔽           | On 2.504        | 4 V | 23 mA           | 58 mW          | Read         |              |                 |
|         | VDDO     | 2 1.80V             | Off             | v   | 0 mA            | 0 mW           | Read         |              |                 |
|         | VDDO     | 3 2.50V 🔽           | On 2.48         | 5 V | 24 mA           | 60 mW          | Read         |              |                 |
|         | VDDO     | 4 1.80V             | Off             | v   | 0 mA            | 0 mW           | Read         |              |                 |
|         | VDDO     | 5 2.50V 🔽           | On 2.48         | 5 V | 16 mA           | 40 mW          | Read         |              |                 |
|         | VDDO     | 6 1.80V 🔽           | Off 0.00        | 9 V | 0 mA            | 0 mW           | Read         |              |                 |
|         | VDDO     | 7 2.50V 🔽           | On 2.48         | ı v | 16 mA           | 40 mW          | Read         |              |                 |
|         | VDDO     | 8 1.80V 🔽           | Off 0.00        | γ   | 0 mA            | 0 mW           | Read         |              |                 |
|         | VDDO     | 9 2.50V 🔽           | On 2.49         | 2 V | 16 mA           | 40 mW          | Read         |              |                 |
|         |          |                     |                 | tal | 408 mA          | 0.835 W        | Read All     | $\mathbf{D}$ |                 |
|         | Output   | - Select Voltage    |                 | -   |                 | 0.055 11       | $\sim$       |              |                 |
|         | Supplies | Power On P          | ower Off        | Со  | mpare Design Es | stimates to Me | asurements   |              |                 |

Figure 6.11. EVB GUI—Regulators

#### 6.6.1 Verify Free-Run Mode Operation

Assuming no external clocks have yet been connected to the INPUT CLOCK differential SMA connectors, labeled "INx/INxB" and located around the perimeter of the EVB, the DUT should now be operating in free-run mode and locked to the onboard XO.

You can run a quick check to determine if the device is powered up, generating output clocks, and consuming power by clicking on the "**Read All**" button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

**Note:** Turning  $V_{DD}$  or  $V_{DDA}$  "Off" will power-down and reset the DUT. Once both of these supplies are turned "On" again, you must reload the desired frequency plan back into the device memory by selecting the "**Write Design to EVB**" button on the CBPro home screen:

| Si5386 EVB Default Configuration - ClockBuilder Pro   |  |
|---|--|
| ClockBuilder Pro v2.22.3 🎭  | SILICON LABS   |
| Design Dashboard 🔻  | Configuring Si5386A Rev E  |
| You have made edits to the EVB design. You can also save your new of Design to Project File" link.  | onfiguration to a project file for future use by clicking the "Save                |
| Edit Configuration with Wizard<br>Design ID & Notes · Revision · Host Interface · Reference ·<br>Free Run · ZDM · Inputs · Input Select · Outputs · DSPLL ·<br>LOS · OOF · LOL · INTR | Evaluation Board Detected<br>Si5386A Rev E EVB<br>Write Design to EVB Open EVB GUI |

Figure 6.12. CBPro—Write Design Button

Failure to do the step above will cause the device to read in the preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks, running in free-run mode from the XO, using external instrumentation connected to the output clock SMA connectors, labeled OUTx/OUTs. To verify plan inputs, go to the appropriate configuration page or click on "Frequency Plan Valid" to see the design report.

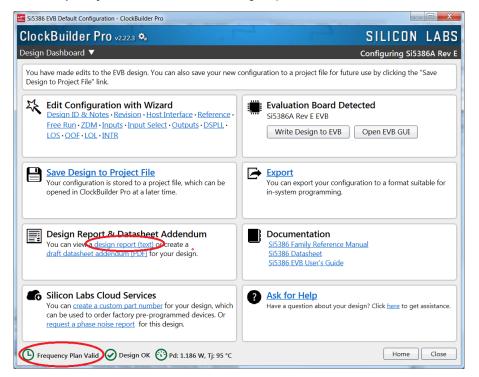


Figure 6.13. CBPro—Design Report Button and Link

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

| 🔀 Si5386A Design Re                     | port   | _ 🗆 🗙    |
|---|--|----------|
| Design Report                           |  |          |
| Overview                                |  | <b>A</b> |
| Part:                                   | S15386A Rev E  |          |
| Design ID:<br>Created By:<br>Timestamp: | <pre><none> ClockBuilder Pro v2.22.3 [2018-03-30] 2018-04-03 16:15:20 GMT-05:00</none></pre>   |          |
| Design Rule C                           |  |          |
| Errors:<br>- No errors                  |  |          |
| Warnings:<br>- No warnings              |  |          |
| Design                                  |  |          |
| Host Interfac                           |  |          |
| SPI Mode:                               | Supply: VDD (Core)<br>4-Wire<br>s Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins) |          |
| Reference:                              | - Oscillator)  |          |
| Inputs:                                 |  |          |
|   | 2 MHz [ 30 + 18/25 MHz ]   |          |
| Stan<br>IN2: Unus                       |  |          |
| IN3: Unus                               | ed   |          |
| Outputs:<br>0010A: 2.94                 | 912 GHz [ 2 + 2966/3125 GHz ]  |          |
| Enab<br>OUTO: Unus                      | led, High-Speed Diff 2.5 V<br>ed   |          |
|   | 04 MHz [ 983 + 1/25 MHz ]<br>led, LVDS 2.5 V   |          |
| OTTT2 • TID115                          |  | Ψ.       |
| Copy to Clipboard                       | d Save Report Ask for Help   | Close    |

Figure 6.14. CBPro—Design Report

#### 6.6.2 Verify Locked Mode Operation

Now, assuming that you connect the input clocks to the EVB as shown in the Design Report above, the DUT on your EVB will be running in "locked" mode.

#### 6.7 Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the configuration using the CBPro Wizard, click on the appropriate category. The category may also be selected from a dropdown list by clicking on the "**Design Dashboard**" button above this section.

| Si5386 EVB Default Configuration - ClockBuilder Pro  |  |
|--|--|
| ClockBuilder Pro v2.22.3 🍫   | SILICON LABS   |
| Design Dashboard   | Configuring Si5386A Rev E  |
| You have made edits to the EVB design. You can also save your new or Design to Project File" link.   | configuration to a project file for future use by clicking the "Save                                 |
| Edit Configuration with Wizard<br>Design ID & Notes - Revision - Host Interface - Reference -<br>Free Run - ZDM - Inputs - Input Select - Outputs - DSPLL -<br>LOS - OOF - LOL - INTR                        | Evaluation Board Detected         Si5386A Rev E EVB         Write Design to EVB         Open EVB GUI |
| Save Design to Project File<br>Your configuration is stored to a project file, which can be<br>opened in ClockBuilder Pro at a later time.   | You can export your configuration to a format suitable for in-system programming.                    |
| Design Report & Datasheet Addendum<br>You can view a design report (text) or create a<br>draft datasheet addendum (PDF) for your design.   | Documentation<br>SI5386 Family Reference Manual<br>SI5386 Datasheet<br>SI5386 EVB User's Guide       |
| <b>Silicon Labs Cloud Services</b><br>You can create a custom part number for your design, which<br>can be used to order factory pre-programmed devices. Or<br>request a phase noise report for this design. | Ask for Help<br>Have a question about your design? Click <u>here</u> to get assistance.              |
| Design OK OPd: 1.186 W, Tj: 95 °C  | Home Close   |

Figure 6.15. CBPro—Edit Settings Links and Pulldown

You will now be taken to the Wizard's step-by-step menu pages to allow you to change any of the default plan's operating configurations.

| Si5386 EVB Default | Configuration - ClockBuilder Pro   |                            |           |  |  |  |  |  |
|--------------------|--|----------------------------|-----------|--|--|--|--|--|
| ClockBuild         | er Pro v2.22.3 🎭   | SILICON                    | LABS      |  |  |  |  |  |
| Step 1 of 14 - De  | sign ID & Notes 🔻  | Configuring Si53           | 86A Rev E |  |  |  |  |  |
| Design ID          | sgisters, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/r  | evision identifier         |           |  |  |  |  |  |
| Design ID:         | (optional; max 8 characters) The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN.  |                            |           |  |  |  |  |  |
| Padding Mode:      | NULL Padded<br>If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pad<br>character).   | ded with 0x00 bytes (aka I | NULL      |  |  |  |  |  |
|                    | Space Padded<br>If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padded with 0x20 bytes (space<br>character).                        |                            |           |  |  |  |  |  |
|                    | want here. The text is stored in your project file and included in design reports and custom p<br>ord wrapped in reports, you can use newlines to start a new paragraph. | art number datasheet add   | endums.   |  |  |  |  |  |
|                    |  |                            |           |  |  |  |  |  |
|                    |  |                            |           |  |  |  |  |  |
|                    |  |                            |           |  |  |  |  |  |
|                    |  |                            |           |  |  |  |  |  |
| Frequency Pla      | n Valid 🕑 Design OK 🔅 Pd: 1.186 W, Tj: 95 °C Write to EVB < Back   | Next > Finish              | Cancel    |  |  |  |  |  |

Figure 6.16. CBPro—Design ID and Notes Edit Page

As you edit the settings, you may notice the "Frequency Plan Valid" link in the lower left corner updating. You can click on this link to bring up the design report to confirm that the information is correct. When you are finished editing each page, you may click on the "> Next" or "< Back" buttons to move from page to page. When you are done making all your desired changes, you can click on "Write to EVB" to reconfigure your device. The Design Write status window will appear each time you write to the EVB.

| Si5386A Design Write          | Ca funnt | _ <b></b> |
|-------------------------------|----------|-----------|
| Writing Si5386A Design to EVB |          |           |
| Address 0x025D                |          |           |
|                               |          |           |
|                               |          |           |

Figure 6.17. CBPro—Design Write Progress Window

When you have verified your design settings, you may save the design project. Click on the "**Finish**" button to return to the home page and then click on the "**Save Design to Project File**" link. You can use the windows file browser to reach the correct location and enter a filename for this new project.

#### 6.8 Workflow Scenario #3: Testing a User-Created Device Configuration

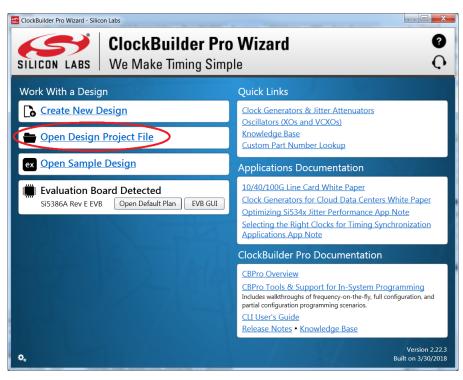


Figure 6.18. CBPro—Open Design Project Link

Using the windows file browser popup, locate your CBPro design file (\*.slabtimeproj or \*.sitproj file).

| Copen CBPro Project File  |                            |                  |                    |   |                                  |   |  |  |
|---|----------------------------|------------------|--------------------|---|----------------------------------|---|--|--|
| Organize 🔻 New f  | folder                     |                  |                    |   | •                                | 0 |  |  |
| ★ Favorites   | Name                       | Date modified    | Туре               | Size  |                                  |   |  |  |
| ■ Desktop<br>Downloads<br>Dropbox (Sil<br>Secent Place <sub>=</sub> | Si5386A-RevE-Project       | 4/3/2018 4:18 PM | Silicon Labs Timin | 12 KB   |                                  |   |  |  |
| Libraries<br>Documents<br>Music<br>Pictures<br>Libraries            |                            |                  |                    |   |                                  |   |  |  |
| 🍇 Computer<br>🏷 Windows (C: 👻                                       |                            |                  |                    |   |                                  |   |  |  |
| File  | name: Si5386A-RevE-Project |                  |                    | <ul> <li>▼ Silico</li> <li><u>O</u>p</li> </ul> | n Labs Timing Proje<br>en 🚽 Cano |   |  |  |

Figure 6.19. CBPro—Windows File Browser

Select "Yes" when the WRITE DESIGN to EVB popup appears:

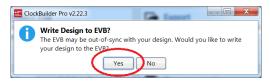


Figure 6.20. CBPro—Write Design Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

#### 6.9 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export" as shown below:

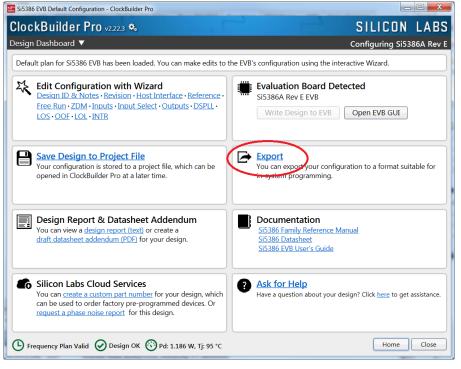


Figure 6.21. CBPro—Export Design Programming File

You can now write your device's complete configuration to file formats suitable for in-system programming.

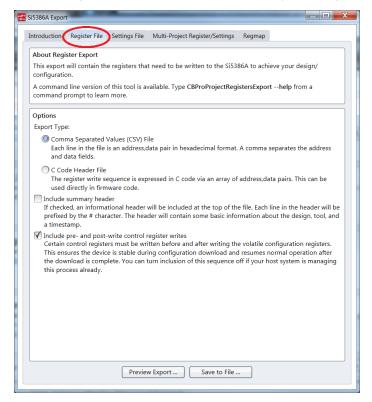


Figure 6.22. CBPro—Export Configuration Window

Si5386 Evaluation Board User's Guide • Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

# 7. Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

The Si5386 device loads the Non-Volatile Memory (OTP) on either a powerup or a hard reset, overwriting any previous volatile register changes. This allows the device to begin functioning as desired on powerup/hard-reset without manual intervention. To restart the device while preserving volatile changes and without loading the OTP, use soft-reset through the registers or EVB-GUI.

**Note:** Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5386 using ClockBuilder Pro on the Si5386 EVB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5386 RAM space and can be done virtually an unlimited number of times. Writing to OTP is limited as described below.

Refer to the Si5386 Family Reference Manual and device datasheet for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

Si5386 Evaluation Board User's Guide • Serial Device Communications (Si5386 <-> MCU)

## 8. Serial Device Communications (Si5386 <-> MCU)

#### 8.1 Onboard SPI Support

The MCU on-board the Si5386A-E-EB communicates with the Si5386 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5386 device is the SPI slave. The Si5386 device can also support a 2-wire I<sup>2</sup>C serial interface, although the Si5386A-E-EB does NOT support the I<sup>2</sup>C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I<sup>2</sup>C.

#### 8.2 External I<sup>2</sup>C Support

I<sup>2</sup>C can be supported if driven from an external I<sup>2</sup>C controller. The serial interface signals between the MCU and Si5386 pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I<sup>2</sup>C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the on-board MCU from the Si5386 device. The shunt at J4 (I2C\_SEL) must also be removed to select I<sup>2</sup>C as Si5386 interface type. An external I<sup>2</sup>C controller connected to the Si5386 side of J36 can then communicate to the Si5386 device. (For more information on I<sup>2</sup>C signal protocol, please refer to the Si5386 data sheet.)

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5386 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J36 and J4,  $I^2C$  operation should use J36 pin 4 (DUT\_SDA\_SDIO) as the  $I^2C$  SDA and J36 pin 8 (DUT\_SCLK) as the  $I^2C$  SCLK. Please note the external  $I^2C$  controller will need to supply its own  $I^2C$  signal pull-up resistors.

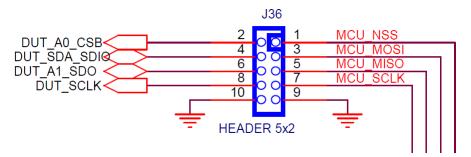


Figure 8.1. Serial Communications Header J36

Si5386 Evaluation Board User's Guide • Si5386A-E-EB Schematic and Bill of Materials (BOM)

## 9. Si5386A-E-EB Schematic and Bill of Materials (BOM)

The Si5386 EVB Schematic and Bill of Materials (BOM) can be found online at: http://www.silabs.com/si538x-4x-evb

Note: Please be aware the Si5386 EVB schematic is in OrCad Capture hierarchical format and not in a typical "flat" schematic format.

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