Si5348 Rev D Data Sheet

Network Synchronizer for SyncE/ 1588 PTP Telecom Boundary (T-BC) and Slave (T-TSC) Clocks

The Si5348 combines the industry's smallest footprint and lowest power network synchronizer clock with unmatched frequency synthesis flexibility and ultra-low jitter. The Si5348 is ideally suited for wireless backhaul, IP radio, small and macro cell wireless communications systems, and data center switches requiring both traditional and packet based network synchronization.

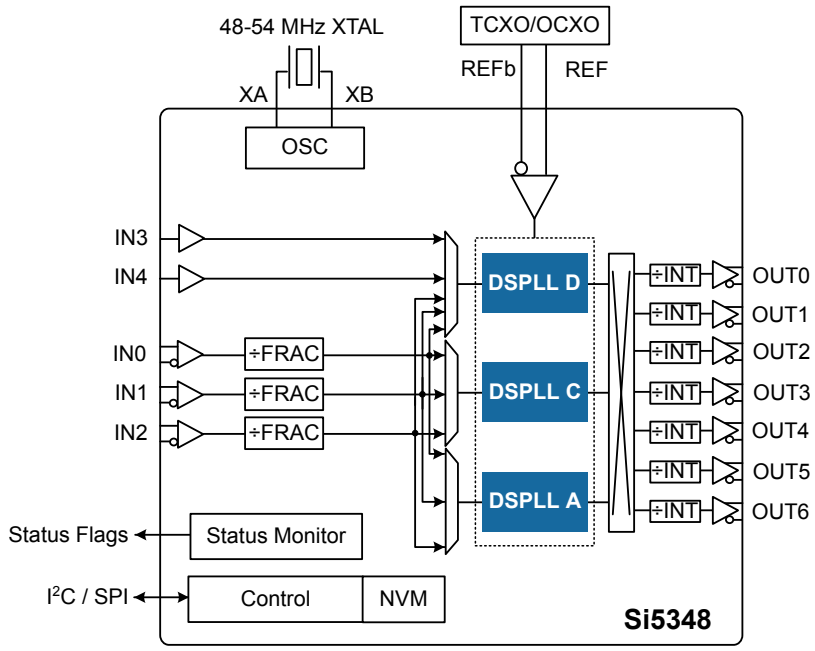
The three independent DSPLLs™ are individually configurable as a SyncE PLL, IEEE 1588 DCO or a general-purpose PLL for processor/FPGA clocking. The Si5348 can also be used in legacy SETS systems needing Stratum 3/3E compliance. The optional digitally controlled oscillator (DCO) mode provides precise timing adjustment to 1 ppt for 1588 (PTP) clock steering applications. The unique design of the Si5348 allows the TCXO/OCXO reference input to determine the device's frequency accuracy and stability. The Si5348 is programmable via a serial interface with in-circuit programmable non-volatile memory so it always powers up into a known configuration. Programming the Si5348 is easy with ClockBuilder Pro™ software. Factory pre-programmed devices are also available.

Applications:

- Synchronous Ethernet (SyncE) ITU-T G.8262 EEC Option 1 & 2
- Telecom Boundary Clock (T-BC) as defined by ITU-T G.8273.2
- IEEE 1588 (PTP) slave clock synchronization
- Stratum 3/3E, G.812, G.813 network synchronization

KEY FEATURES

- Three independent DSPLLs in a single monolithic IC supporting flexible SyncE/ IEEE 1588 and SETS architectures
- Ultra-low jitter of 100 fs
- Input frequency range:
  - External crystal: 48 to 54 MHz
  - REF clock: 5 to 250 MHz
  - Diff clock: 8 kHz to 750 MHz
  - LVCMOS clock: 8 kHz to 250 MHz
- Output frequency range:
  - Differential: 1 PPS to 718.5 MHz
  - LVCMOS: 1 PPS to 250 MHz
- Meets the requirements of:
  - ITU-T G.8262 (SyncE) EEC Options 1 & 2
  - ITU-T G.812 Type III, IV
  - ITU-T G.813 Option 1
  - Telcordia GR-1244, GR-253 (Stratum-3/3E)



1. Feature List

The Si5348 features are listed below:

- Three independent DSPLLs in a single monolithic IC supporting flexible SyncE/IEEE 1588 and SETS architectures
- Ultra-Low Jitter
  - 100 fs typ (12 kHz to 20 MHz)
- Meets the requirements of:
  - ITU-T G.8273.2 T-BC
  - ITU-T G.8262 (SyncE) EEC Options 1 & 2
  - ITU-T G.812 Type III, IV
  - ITU-T G.813 Option 1
  - Telcordia GR-1244, GR-253 (Stratum-3/3E)
- Each DSPLL generates any output frequency from any input frequency
- Input frequency range:
  - External crystal: 48-54 MHz
  - REF clock: 5-250 MHz
  - Diff clock: 8 kHz-750 MHz
  - LVCMOS clock: 8 kHz-250 MHz
- Output frequency range:
  - Differential: 1 PPS to 718.5 MHz
  - LVCMOS: 1 PPS to 250 MHz
- Pin or software controllable DCO on each DSPLL with typical resolution to 1 ppt/step
- TCXO/OCXO reference input determines DSPLL free-run/holdover accuracy and stability
- Programmable jitter attenuation bandwidth per DSPLL: 0.001 Hz to 4 kHz
- Highly configurable output drivers: LVDS, LVPECL, LVCMOS, HCSL, CML
- Core voltage:
  - VDD: 1.8 V ±5%
  - VDDA: 3.3 V ±5%
- Independent output supply pins: 3.3 V, 2.5 V, or 1.8 V
- Built-in power supply filtering
- Status monitoring: LOS, OOF, LOL
- Serial Interface: I^2C or SPI (3-wire or 4-wire)
- ClockBuilder™ Pro software tool simplifies device configuration
- 5 input, 7 output, 64 QFN
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

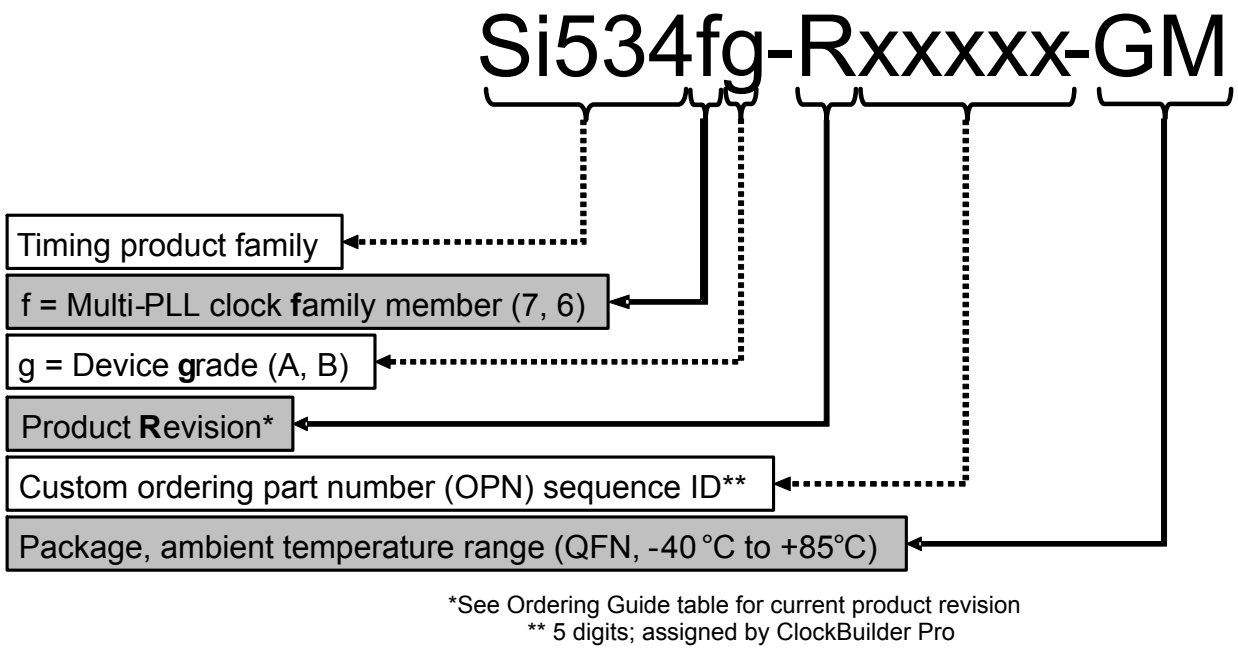
2. Ordering Guide

Table 2.1. Si5348 Ordering Guide

Ordering Part Number	# of DSPLLs	Output Clock Frequency Range	Package	RoHS-6, Pb-Free	Temperature Range
Si5348A-D-GM [1, 2]	3	1 Hz to 718.5 MHz	64-Lead 9x9 QFN	Yes	–40 to 85 °C
Si5348B-D-GM [1, 2]		1 Hz to 350 MHz			
Si5348-D-EVB	—	—	Evaluation Board	—	—
SiOCXO1-EVB	—	12.800 MHz	OCXO Evaluation Board	—	—

Note:

1. Add an R at the end of the device part number to denote tape and reel ordering options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by the ClockBuilder Pro software. Part number format is: Si5348A-Dxxxxx-GM, where “xxxxx” is a unique numerical sequence representing the pre-programmed configuration.



*See Ordering Guide table for current product revision
** 5 digits; assigned by ClockBuilder Pro

Figure 2.1. Ordering Part Number Fields

Table of Contents

3. Functional Description

The Si5348 offers three DSPLLs that have identical performance and flexibility which can be independently configured and controlled through the serial interface. Each of the DSPLLs support locked, free-run, and holdover modes of operation with an optional DCO mode for IEEE 1588 applications. The device requires an external crystal and an external reference (TCXO or OCXO) to operate. The reference input (REF/REFb) determines the frequency accuracy and stability while in free-run and holdover modes. The external crystal completes the internal oscillator circuit (OSC) which is used by the DSPLL for intrinsic jitter performance. There are three main inputs (IN0 - IN2) for synchronizing the DSPLLs. Input selection can be manual or automatically controlled using an internal state machine. Two additional manually selected inputs are available to DSPLL D. Any of the output clocks (OUT0 to OUT6) can be configured to any of the DSPLLs using a flexible crosspoint connection. Output 6 is the only output that can be configured for a 1 Hz output to support 1 PPS.

3.1 Standards Compliance

Each of the DSPLLs meet the requirements of ITU-T G.8262 (SyncE), G.812, G.813, G.8273.2 (T-BC), in addition to Telcordia GR-1244 and GR-253 as shown in the compliance report. The DCO feature enables IEEE1588 (PTP) implementations in addition to hybrid SyncE + IEEE1588 (T-BC).

3.2 Frequency Configuration

The frequency configuration for each of the DSPLLs is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), and integer output division (Rn) allows each of the DSPLLs to lock to any input frequency and generate virtually any output frequency. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

3.3 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter and wander attenuation. Register configurable DSPLL loop bandwidth settings of 1 mHz to 4 kHz are available for selection for each of the DSPLLs. Since the loop bandwidth is controlled digitally, each of the DSPLLs will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

Table 3.1. Loop Bandwidth Requirements for North America

SONET (Telcordia)	SDH (ITU-T)	SyncE (ITU-T)	Loop Bandwidth
GR-253 Stratum 3E	G.812 Type III	—	0.001 Hz
GR-253 Stratum 3	G.812 Type IV	G.8262 EEC Option 2	<0.1 Hz
—	G.813 Option 1	G.8262 EEC Option 1	1 - 10 Hz

3.3.1 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in the range of 100 Hz to 4 kHz are available for selection. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting. The fastlock feature can be enabled or disabled independently for each of the DSPLLs.

3.4 Modes of Operation

Once initialization is complete, each of the DSPLLs operates independently in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown below. The following sections describe each of these modes in greater detail.

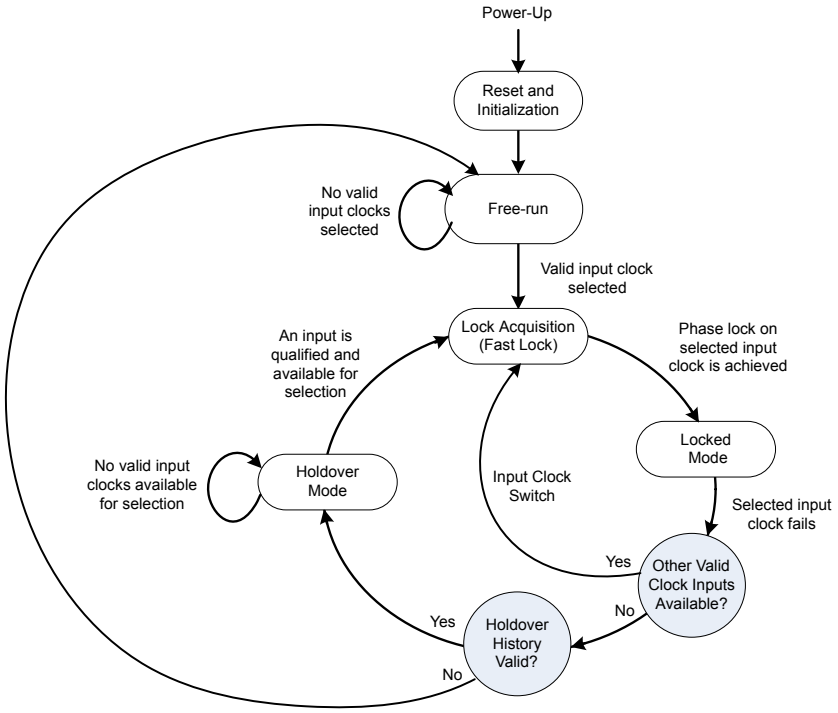


Figure 3.1. Modes of Operation

3.4.1 Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RSTb pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes. A hard reset affects all DSPLLs, while a soft reset can either affect all or each DSPLL individually.

3.4.2 Free-run Mode

Once power is applied to the Si5348 and initialization is complete, all three DSPLLs will automatically enter freerun mode. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the clock source at the reference inputs (REF/REFb). A TCXO or OCXO is recommended for applications that need frequency accuracy and stability to meet the synchronization standards as shown in the following table:

Table 3.2. Free-run Accuracy for North American and European Synchronization Standards

SONET (Telcordia)	SDH (ITU-T)	SyncE (ITU-T)	Free-run Accuracy
GR-253 Stratum 3E	G.812 Type III	—	±4.6 ppm
GR-253 Stratum 3	G.812 Type IV	G.8262 EEC Option 2	
—	G.813 Option 1	G.8262 EEC Option 1	

3.4.3 Lock Acquisition Mode

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process.If the fast lock feature is enabled, a DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

3.4.4 Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point, any XTAL frequency drift will not affect the output frequency. Each DSPLL has its own LOLb pin and status bit to indicate when lock is achieved. Refer to 3.8.6 LOL Detection for more details on the operation of the loss of lock circuit.

3.4.5 Holdover Mode

Any of the DSPLLs will automatically enter Holdover Mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. Each DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

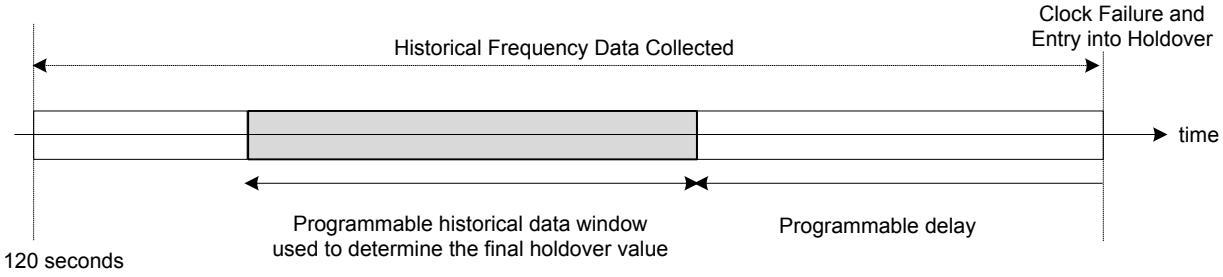


Figure 3.2. Programmable Holdover Window

When entering holdover, a DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the REF/REFb pins. If the clock input becomes valid, a DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequencies to achieve frequency and phase lock with the input clock. This pull-in process is glitchless.

The DSPLL output frequency when exiting holdover can be ramped (recommended). Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The ramp rate can be 0.2 ppm/s, 40,000 ppm/s, or any of about 40 values in between. The DSPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. The same ramp rate settings are used for both exit from holdover and ramped input switching. For more information on ramped input switching see 3.7.6 Ramped Input Switching.

Note: If ramped holdover exit is not selected, the holdover exit is governed either by (1) the DSPLL loop BW or (2) a user-selectable holdover exit BW.

3.5 Digitally-Controlled Oscillator (DCO) Mode

The DSPLLs support a DCO mode where their output frequencies are adjustable in pre-defined steps defined by frequency step words (FSW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increments (FINC) or decrements (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. The DCO mode is available when the DSPLL is operating in locked mode. The DCO mode is mainly used in IEEE1588 (PTP) applications where a clock needs to be generated based on recovered timestamps. In this case timestamps are recovered by the PHY/MAC. A processor containing servo software controls the DCO to close the timing loop between the master and slave nodes. The processor has the option of using the FINC/FDEC pin controls to update the DCO frequency or by controlling it through the serial interface.

3.5.1 Frequency Increment/Decrement Using Pin Controls (FINC, FDEC)

Controlling the output frequency with pin controls is available. This feature involves asserting the FINC or FDEC pins to step (increment or decrement) the DSPLL's output frequency. Both the step size and DCO selection (A, C, D) is made through the serial interface by writing to register bits.

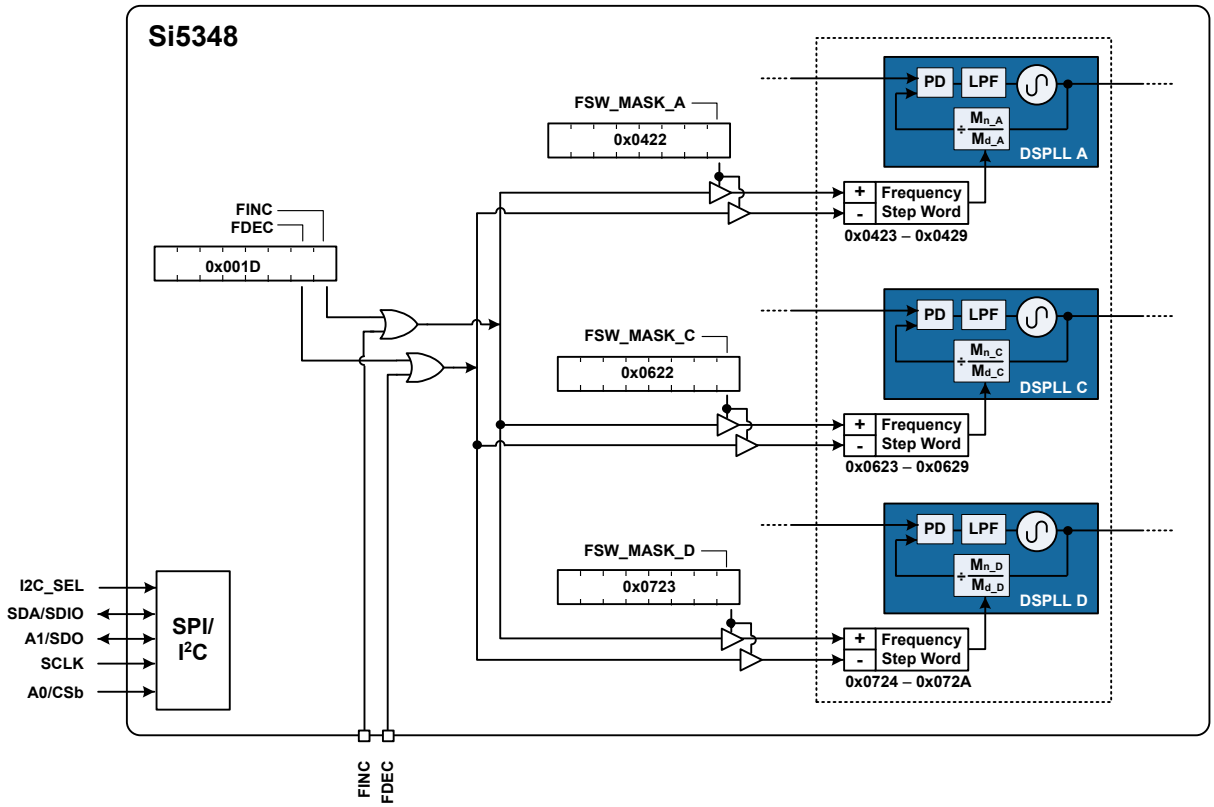


Figure 3.3. Controlling the DCO Mode By Pin Control

3.5.2 Frequency Increment/Decrement Using the Serial Interface

Controlling the DSPLL frequency through the serial interface is available. This feature involves asserting the FINC or FDEC bits to activate the frequency change defined by the frequency step word. A set of mask bits selects the DSPLL(s) that is affect by the frequency change.

3.6 External Reference (XA/XB, REF/REFb)

The external crystal at the XA/XB pins determines jitter performance of the output clocks, and the external reference clock at the REF/REFb pins determines the frequency accuracy, wander and stability during free-run or holdover modes. Jitter from the external clock on the REF/REFb pins will have little effect on the output jitter performance, depending upon the selected bandwidth.

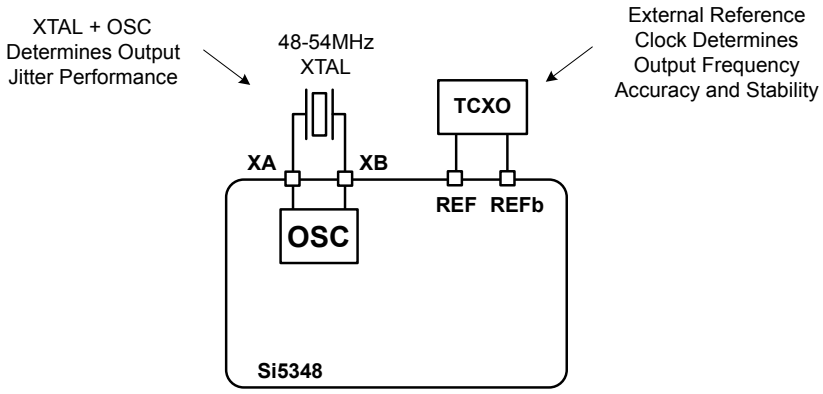


Figure 3.4. External Reference Connections

3.6.1 External Crystal (XA/XB)

The external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLLs. The device includes internal XTAL loading capacitors which eliminate the need for external capacitors and also has the benefit of reduced noise coupling from external sources. A crystal in the range of 48 to 54 MHz is recommended for best jitter performance. Although the device includes built-in XTAL load capacitors (CL) of 8 pF, crystals with load capacitances up to 18 pF can also be accommodated. The Si5348 Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Although ***not*** recommended, the device can also accommodate an external clock at the XA/XB pins instead of a crystal. Selection between the external crystal or clock is controlled by register configuration. The internal crystal loading capacitors (CL) are disabled in this mode. Refer to Table 5.12 Crystal Specifications[1] on page 42 for reference clock requirements when using this mode. The Si5348 Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.

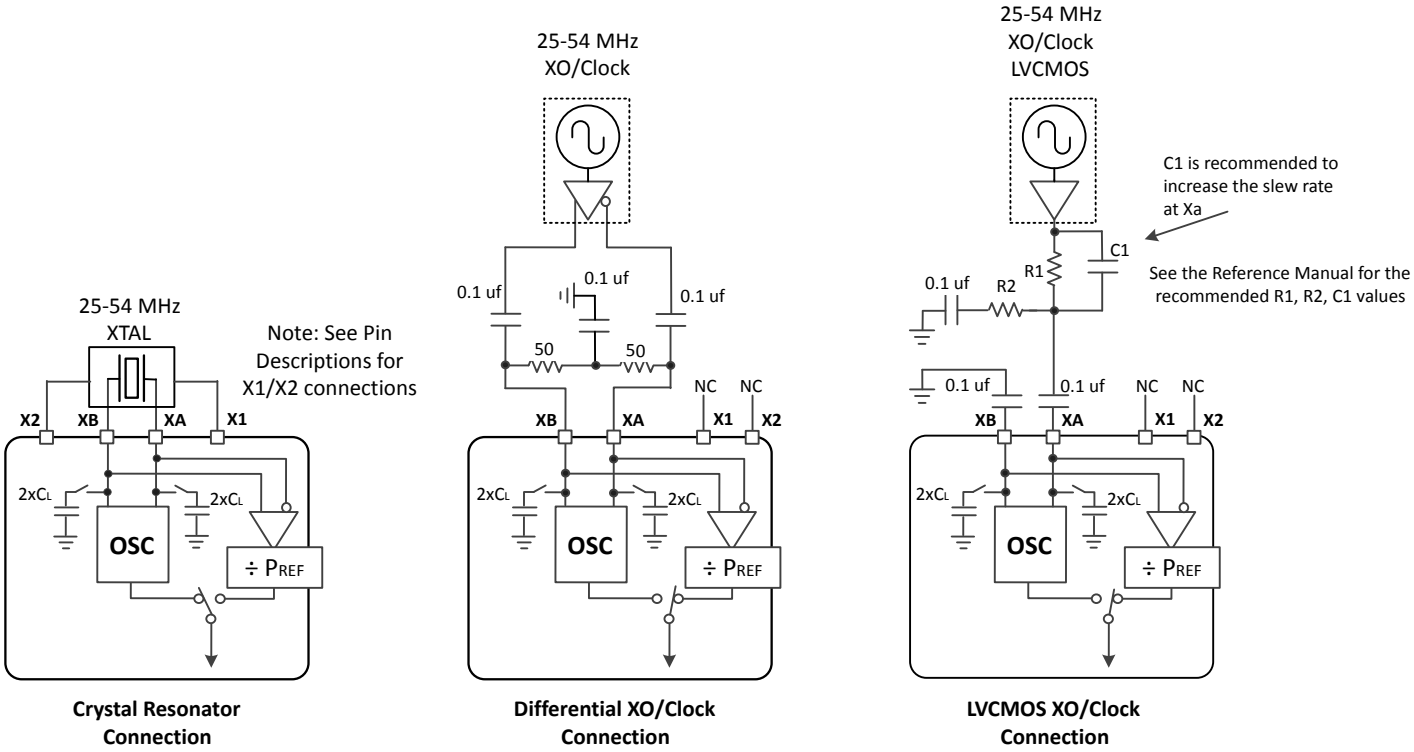
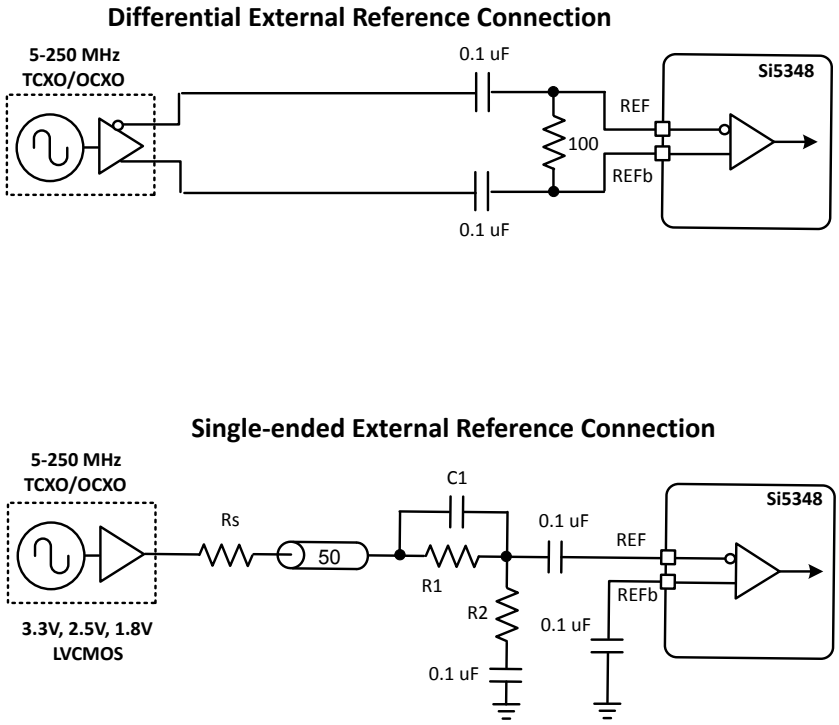


Figure 3.5. Crystal Resonator Connections

Note: See Table 5.3 Input Clock Specifications on page 30 for more information.

3.6.2 External Reference (REF/REFb)

The external reference at the REF/REFb pins is used to determine output frequency accuracy and stability during free-run and holdover modes. This reference is usually from a TCXO or OCXO and can be connected differentially or single-ended as shown in the figure below:



Note: (1) When 3.3V LVCMOS driver is present, C1, R1 and R2 may be needed to keep the signal at INx < 3.6 Vpp_se. See the reference manual for details.

(2) RS matches the CMOS driver to a 50 ohm transmission line (if used)

Figure 3.6. External Reference Connections

Note: See Table 5.3 Input Clock Specifications on page 30 for more information.

3.7 Inputs (IN0, IN1, IN2, IN3, IN4)

There are three inputs, IN0, IN1, and IN2, which can be used to synchronize any of the DSPLLs. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows inputs IN0–IN2 to connect to any of the DSPLLs as shown in the figure below. DSPLL D has two additional inputs, IN3–IN4, which can be manually selected. IN3 and IN4 are CMOS only inputs. If both IN3 and IN4 are used, they must be the same frequency.

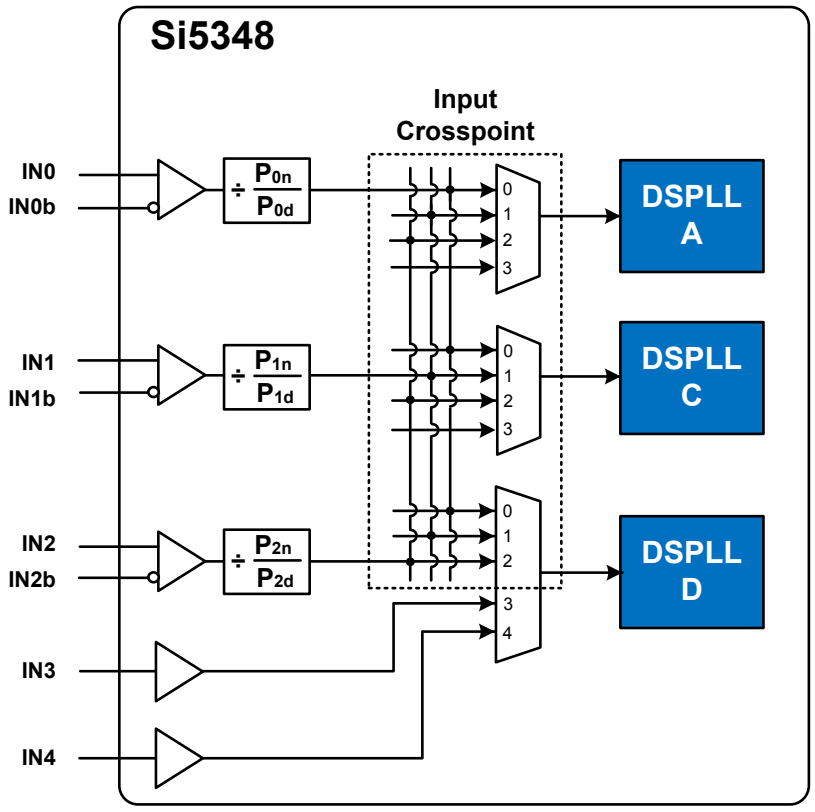


Figure 3.7. DSPLL Input Selection Crosspoint

3.7.1 Input Selection

Input selection for each of the DSPLLs can be made manually through register control or automatically using an internal state machine.

3.7.2 Manual Input Selection

In manual mode the input selection is made by writing to a register. IN0-IN2 and REF is available to DSPLL A and C, IN0-IN4 and REF is available to DSPLL D. If there is no clock signal on the selected input, the DSPLL will automatically enter holdover mode.

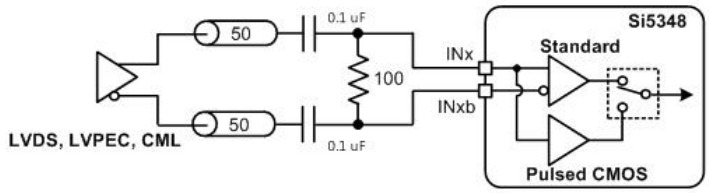
3.7.3 Automatic Input Selection

When configured in this mode, the DSPLLs automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable for each DSPLL and supports revertive or non-revertive selection. All inputs are continuously monitored for loss of signal (LOS) and/or invalid frequency range (OOF). Only inputs that do not assert both the LOS and OOF monitors can be selected for synchronization by the automatic state machine. The DSPLL(s) will enter either holdover or freerun mode if there are no valid inputs available. When both IN3 and IN4 are used, all clock selection must be manual and automatic entry into holdover is not supported, which means that if the Si5348 is locked to either IN3 or IN4 and the input clock fails, the Si5348 will not go into holdover. When only one of IN3 or IN4 is used, automatic clock selection is available and automatic entry into holdover is supported. Hitless switching with IN3-IN4 is not available.

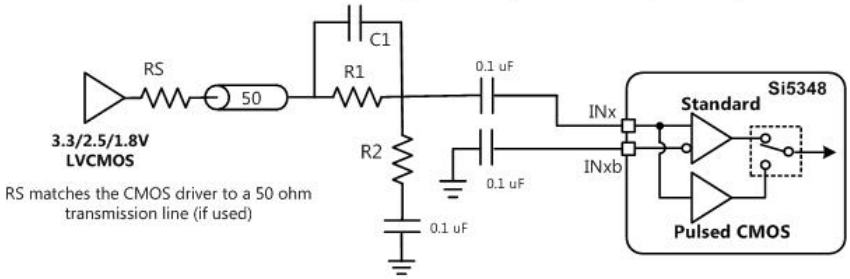
3.7.4 Input Configuration and Terminations

Each of the differential inputs IN0-IN2, and REF are compatible with standard LVDS, LVPECL, HCSL, CML, and single-ended LVCMOS formats, or as a low duty cycle pulsed CMOS format. The standard format inputs have a nominal 50% duty cycle, must be ac-coupled and use the “Standard” Input Buffer selection as these pins are internally dc-biased to approximately 0.83 V. The pulsed CMOS input format allows pulse-based inputs, such as frame-sync and other synchronization signals having a duty cycle much less than 50%. These pulsed CMOS signals are dc-coupled and use the “Pulsed CMOS” Input Buffer selection. In all cases, the inputs should be terminated near the device input pins as shown in the figure below. The resistor divider values given below will work with up to 1 MHz pulsed inputs. In general, following the “Standard AC Coupled Single Ended” arrangement shown below will give superior jitter performance.

Standard AC-coupled Differential (IN0-IN2)

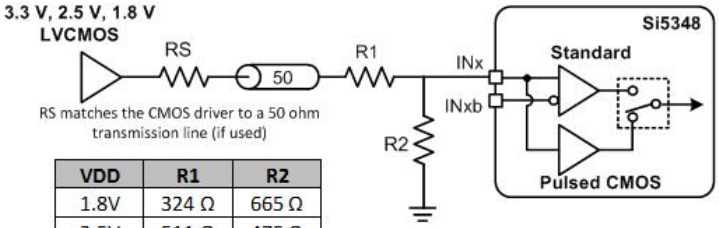


Standard AC-coupled Single-Ended (IN0-IN2)



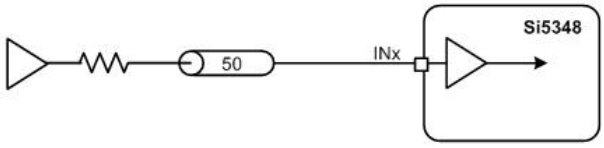
When 3.3V LVCMOS driver is present, use R2 = 845 ohm and R1 = 267 ohm if needed to keep the signal at INx < 3.6 Vpp_se. Including C1 = 6 pf may improve the output jitter due to faster input slew rate at INx. If attenuation is not needed for Inx<3.6Vppse, make R1 = 0 ohm and omit C1, R2 and the capacitor below R2.

Pulsed CMOS DC-coupled Single-Ended only for Frequencies < 1MHz (IN0-IN2)



VDD	R1	R2
1.8V	324 Ω	665 Ω
2.5V	511 Ω	475 Ω
3.3V	634 Ω	365 Ω

IN3, IN4 – DC-coupled LVCMOS



Note: See Datasheet for Input Clock Specifications

Figure 3.8. Termination of Differential and LVCMOS Input Signals

3.7.5 Hitless Input Switching

Hitless switching is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, meaning that they have to be exactly at the same frequency, or at an integer frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during an input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz. Hitless switching can be enabled on a per DSPLL basis. Clock inputs 3 and 4 do not support hitless switching.

3.7.6 Ramped Input Switching

When switching between two plesiochronous input clocks (i.e., the frequencies are "almost the same" but not quite), ramped input switching should be enabled to ensure a smooth transition between the two inputs. Ramped input switching avoids frequency transients and overshoot when switching between frequencies and so is the default switching mode in CBPro. The feature should be turned off when switching between input clocks that are always frequency locked (i.e., are always the same exact frequency). The same ramp rate settings are used for both holdover exit and clock switching. For more information on ramped exit from holdover, see 3.4.5 Holdover Mode.

3.7.7 Glitchless Input Switching

The DSPLLs have the ability of switching between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if it is enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no output runt pulses generated at the output during the transition. All clock inputs, including 3 and 4, support glitchless input switching.

3.7.8 Synchronizing to Gapped Input Clocks

Each of the DSPLLs support locking to an input clock that has missing periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter, so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. This is shown in the figure below:

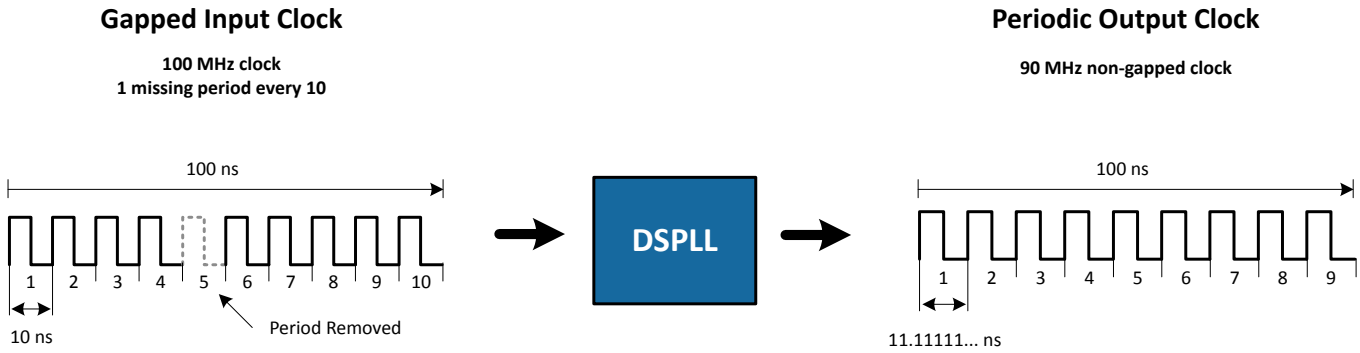


Figure 3.9. Generating an Averaged Clock Output Frequency from a Gapped Clock Input

A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every eight. Locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification in Table 5.8 Performance Characteristics on page 37 when the switch occurs during a gap in either input clock.

3.8 Fault Monitoring

Three input clocks (IN0, IN1, IN2) and the reference input (REF/REFb) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. Each of the DSPLLs also has an LOL indicator, which is asserted when synchronization is lost with their selected input clock. Note that IN3 and IN4 are not monitored.

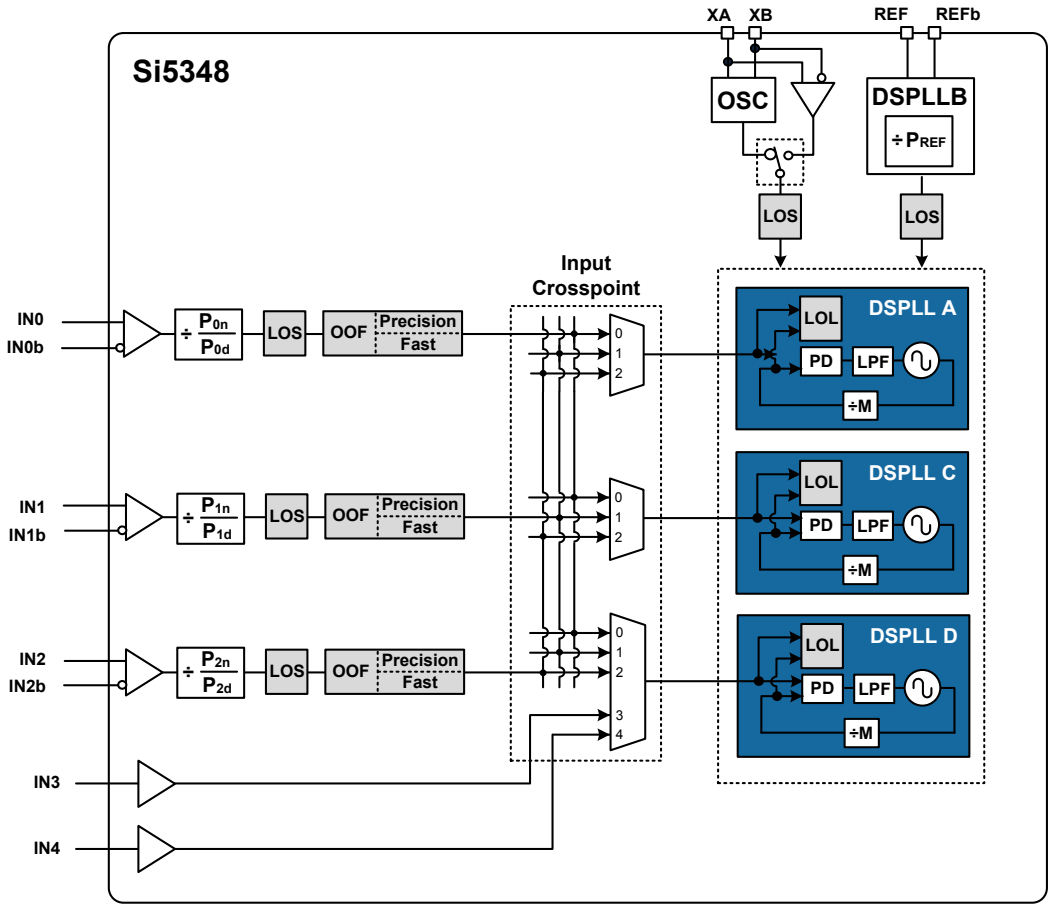


Figure 3.10. Si5348 Fault Monitors

3.8.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register, when set, always stays asserted until cleared. When DSPLLD is configured to use both IN3 and IN4 the LOS outputs are not connected to the holdover entry/exit logic. When configured for one of either IN3 or IN4 (but not both) the LOS for the input clock is connected to the holdover entry/exit logic.

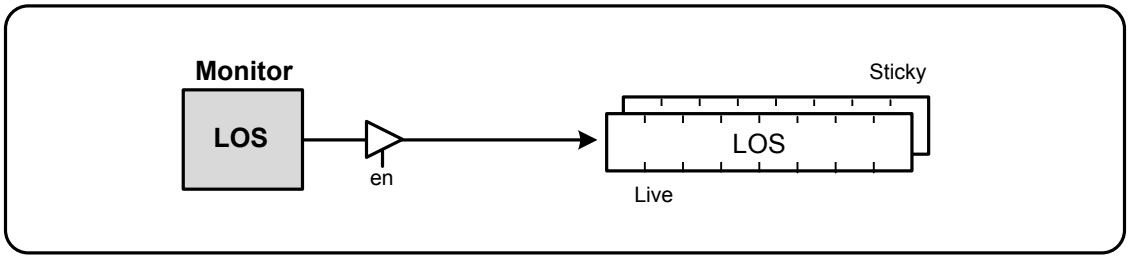


Figure 3.11. LOS Status Indicators

3.8.2 XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

3.8.3 OOF Detection

Input clocks IN0, IN1, IN2 are monitored for frequency accuracy with respect to an OOF reference, which it considers as its “0_ppm” reference. Since a TCXO or OCXO will be connected to the REF input, most applications will declare the REF input to be the OOF reference. The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.

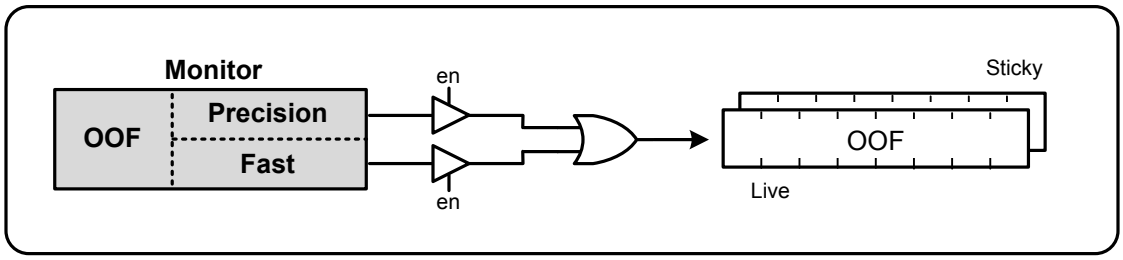


Figure 3.12. OOF Status Indicator

3.8.4 Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1/16 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range, which is register configurable up to ±500 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0 – IN2) as the 0 ppm OOF reference instead of the REF/REFb pins is available. This option is register-configurable. XA/XB can also be used as the 0 ppm reference.

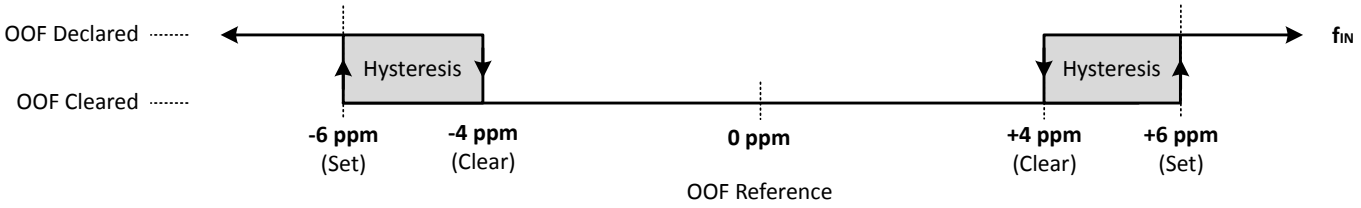


Figure 3.13. Example of Precise OOF Monitor Assertion and De-assertion Triggers

3.8.5 Fast OOF Monitor

Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

3.8.6 LOL Detection

There is an LOL monitor for each of the DSPLLs. The LOL monitor asserts the LOL register bit when a DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition for each of the DSPLLs (LOL_Ab, LOL_Cb, LOL_Db) and also for the reference. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOLb pin reflects the current state of the LOL monitor.

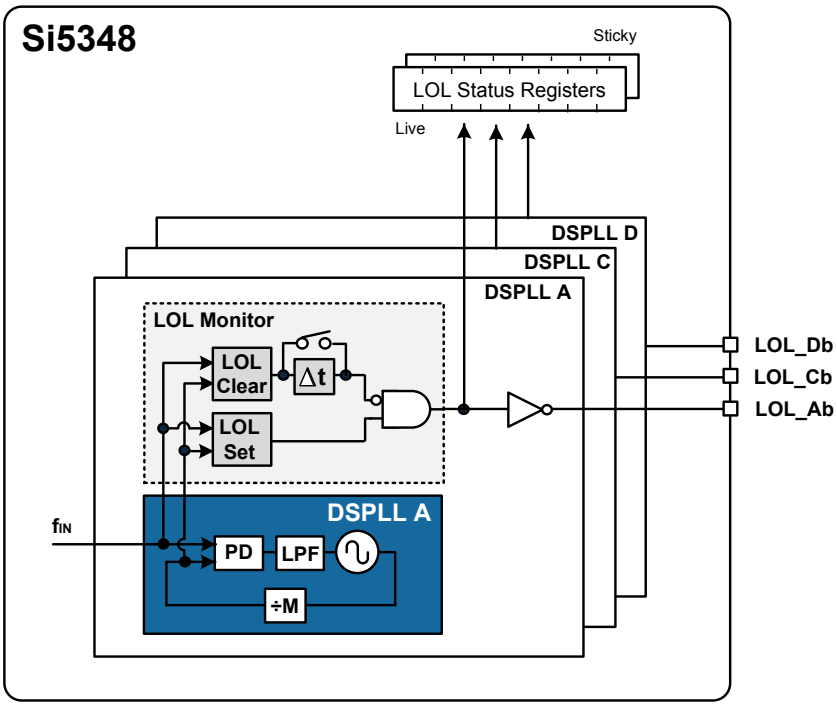


Figure 3.14. LOL Status Indicators

Each of the LOL frequency monitors has adjustable sensitivity, which is register-configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there is more than 1 ppm frequency difference is shown in Figure 3.15 LOL Set and Clear Thresholds on page 18.

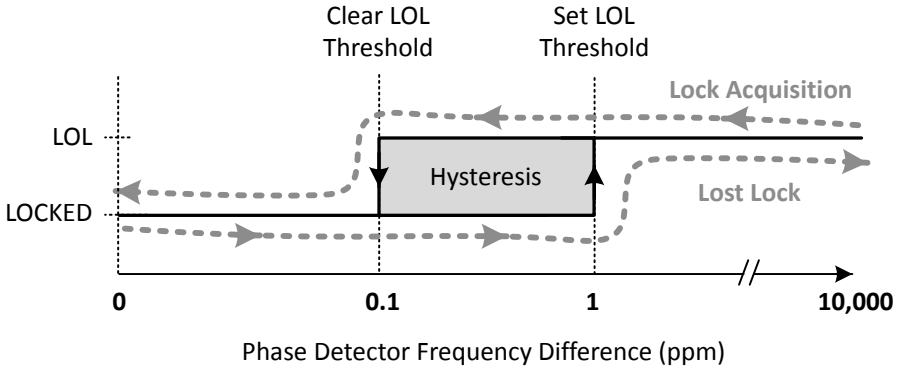


Figure 3.15. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The

configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilderPro utility.

3.8.7 Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the sticky status registers.

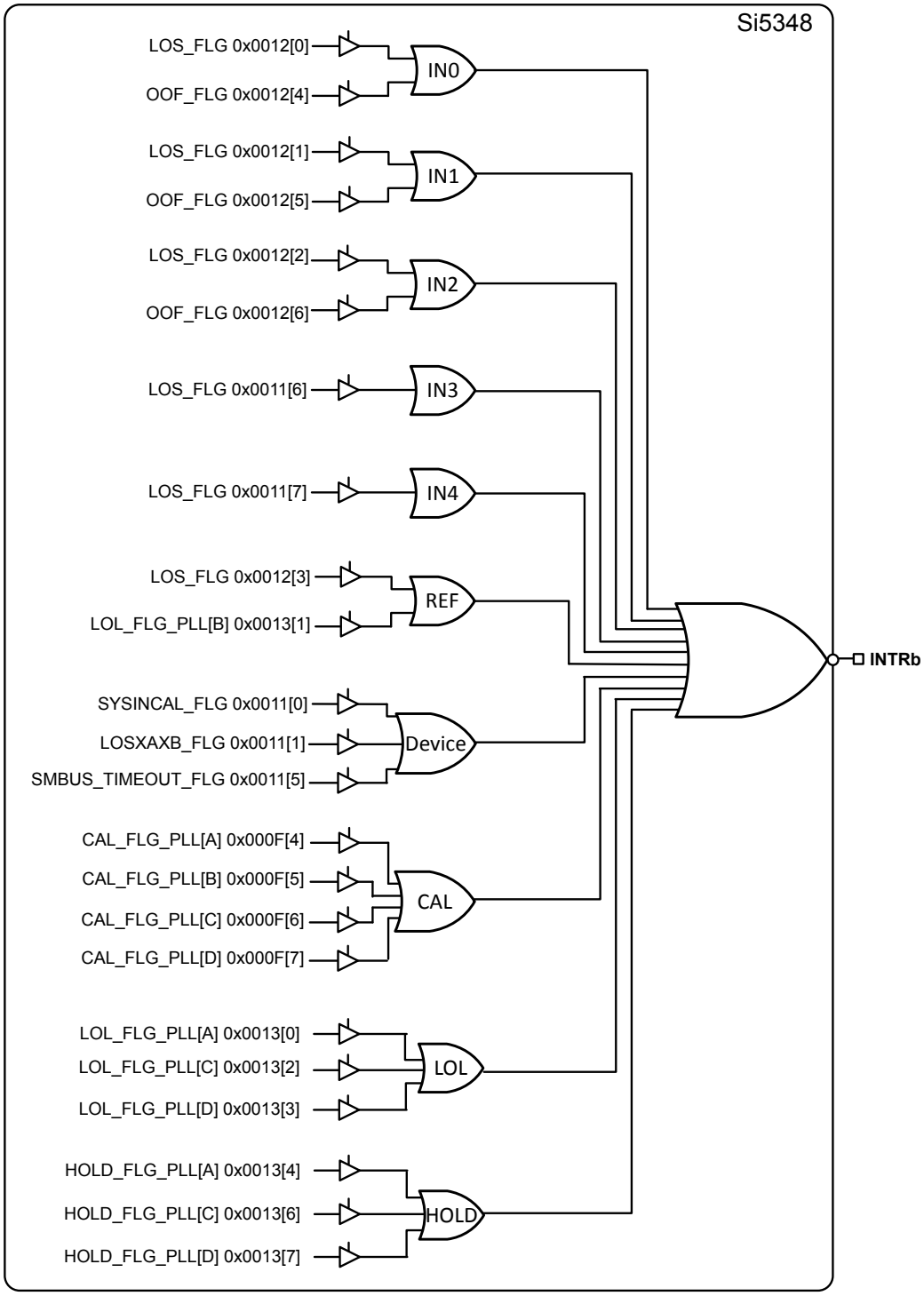


Figure 3.16. Interrupt Triggers and Masks

3.9 Outputs

The Si5348 supports seven differential output drivers. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 14 single-ended outputs, or a combination of differential and single-ended outputs.

3.9.1 Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the DSPLLs as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power-up.

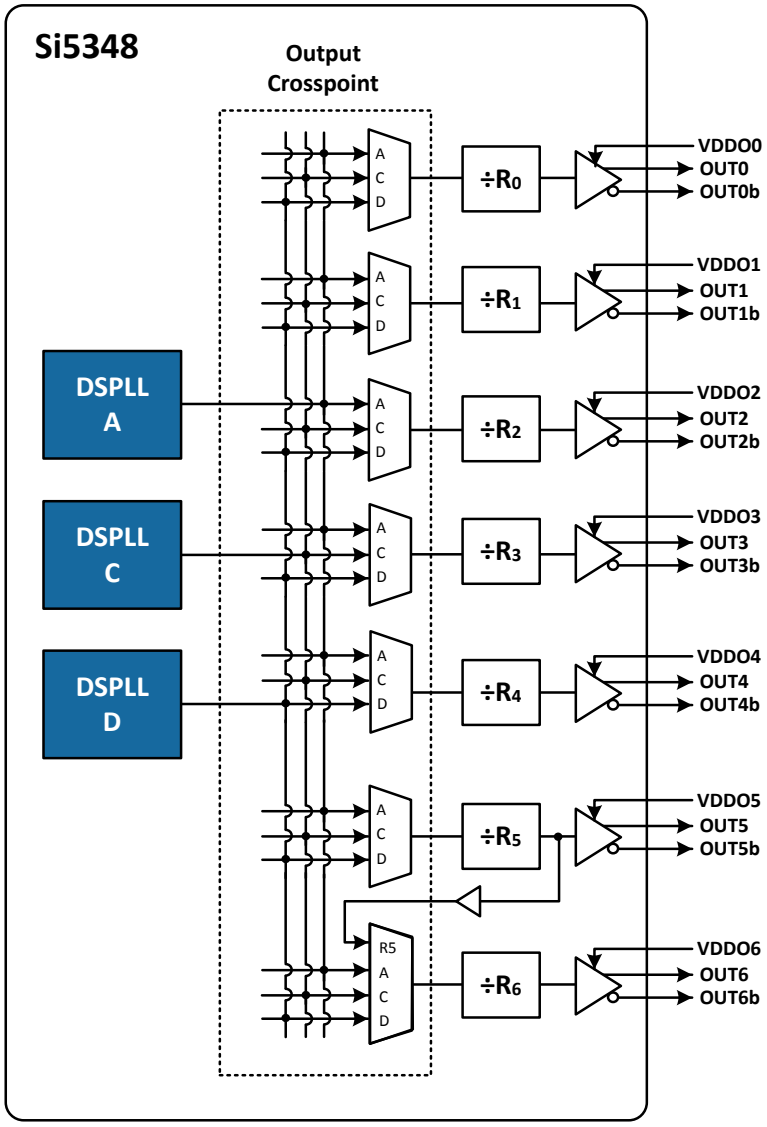


Figure 3.17. DSPLL to Output Driver Crosspoint

3.9.2 Support For 1 Hz Output

Output 6 of the Si5348 can be configured to generate a 1 Hz clock by cascading the R5 and R6 dividers. Output 5 is still usable in this case but is limited to a maximum frequency of 33.5 MHz. ClockBuilder Pro automatically determines the optimum configuration when generating a 1 Hz output (1 PPS).

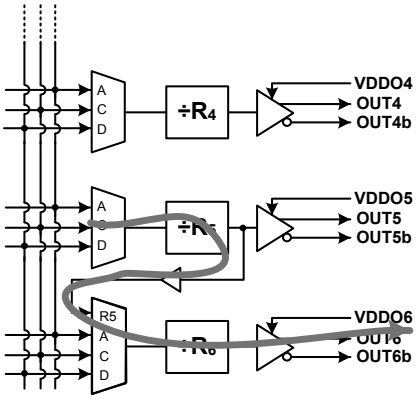


Figure 3.18. Generating a 1 Hz Output using the Si5348

3.9.3 Differential Output Terminations

Note: In this document, the terms LVDS and LVPECL refer to driver formats that are compatible with these signaling standards.

The differential output drivers support both ac-coupled and dc-coupled terminations, as shown in the figure below:

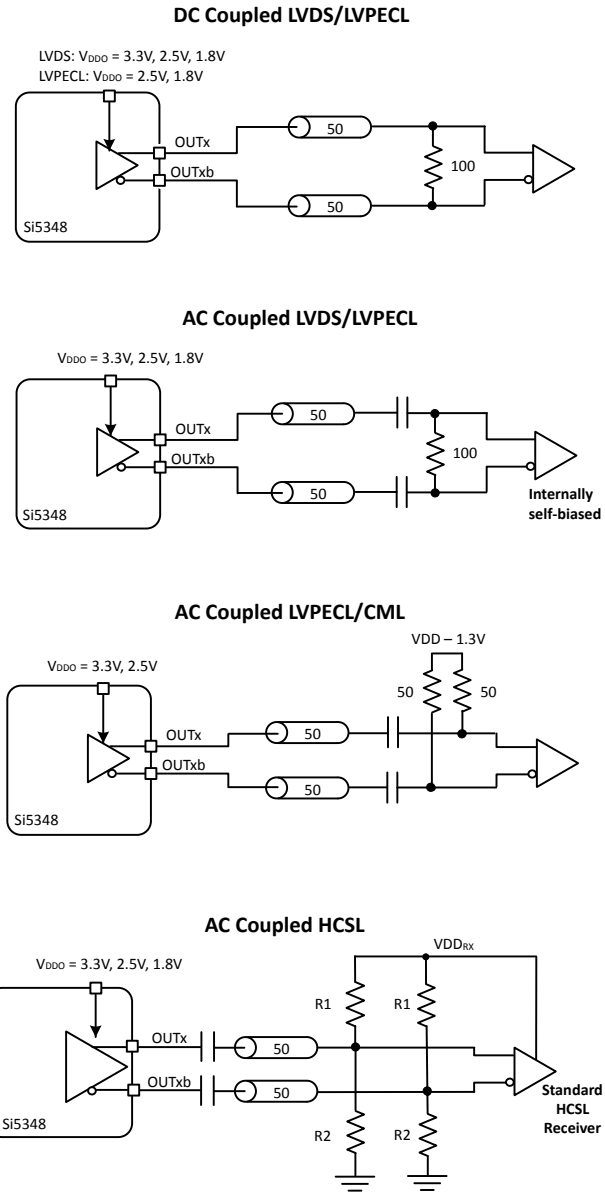


Figure 3.19. Supported Differential Output Terminations

Note: See Si5348 Rev D Reference Manual for resistor values.

3.9.4 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled, as shown in the figure below.

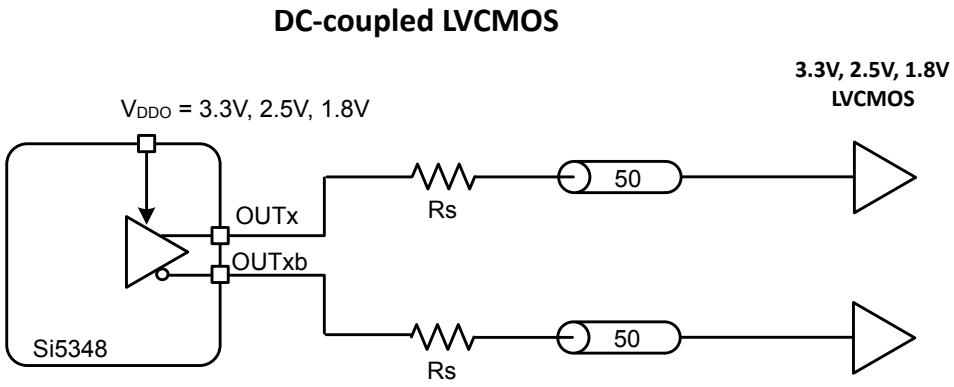


Figure 3.20. LVCMOS Output Terminations

Note: See Si5348 Rev D Reference Manual for resistor values.

3.9.5 Output Signal Format

The differential output amplitude and common mode voltage are both programmable and compatible with a wide variety of signal formats, including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 14 single-ended outputs or a combination of differential and single-ended outputs.

3.9.6 Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (V_{CM}) for the differential modes is programmable and depends on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when dc-coupling the output drivers.

3.9.7 LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO options as shown in the table below. Note that selecting a lower source impedance may result in higher output power consumption.

Table 3.3. Typical Output Impedance (Z_S)

VDDO	CMOS_DRIVE_Selection		
	OUTx_CMOS_DRV=1	OUTx_CMOS_DRV=2	OUTx_CMOS_DRV=3
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

3.9.8 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

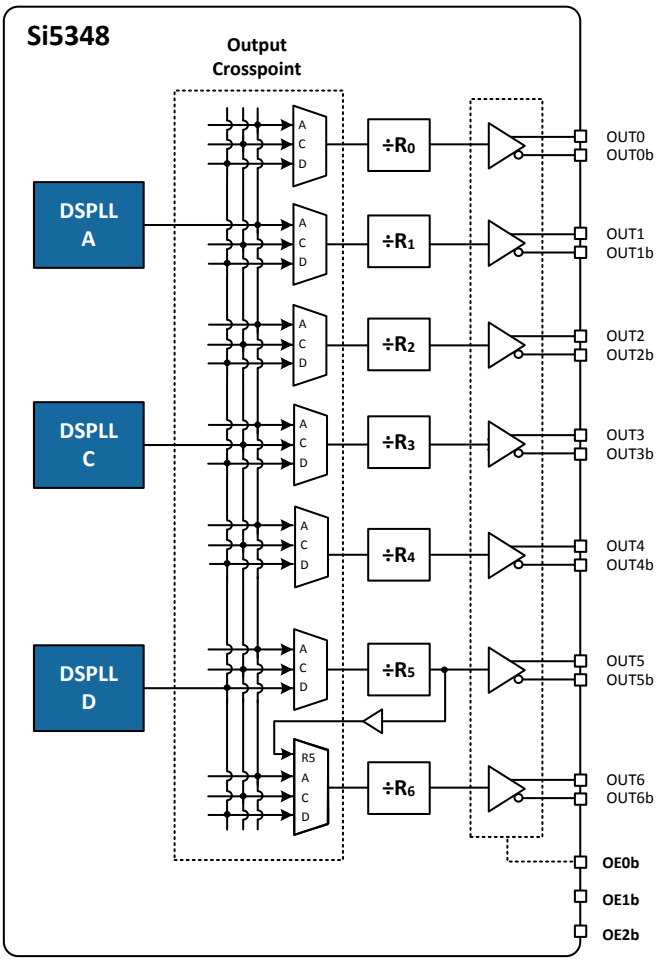
3.9.9 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTxb pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable, which enables complementary clock generation and/or inverted polarity with respect to other output drivers.

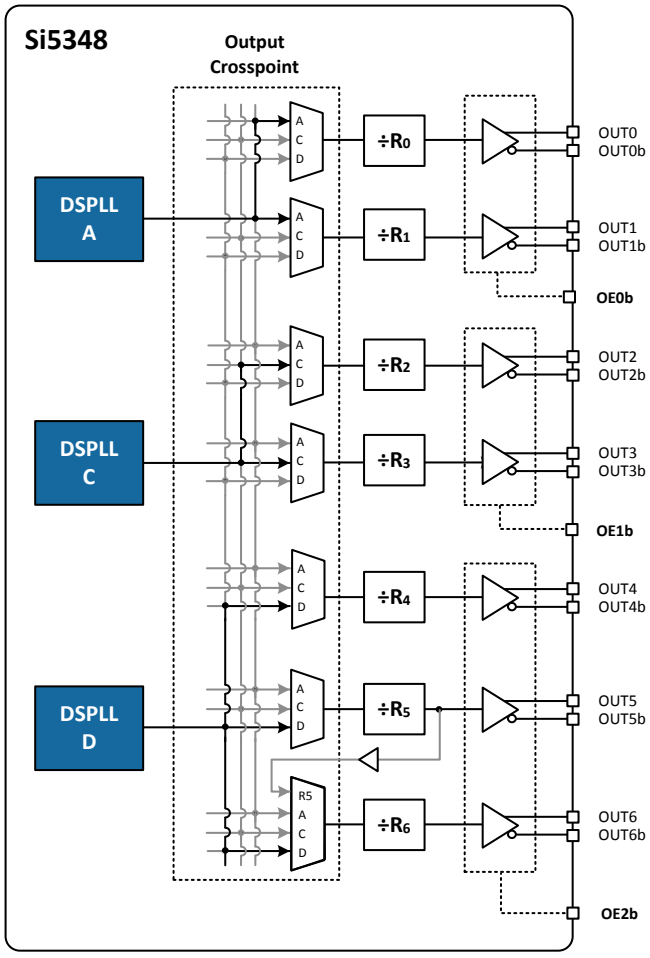
3.9.10 Output Enable/Disable

The Si5348 allows enabling/disabling outputs by pin or register control, or a combination of both. Three output enable pins are available (OE0b, OE1b, OE2b). The output enable pins can be mapped to any of the outputs (OUTx) through register configuration. By default OE0b controls all of the outputs while OE1b and OE2b remain unmapped and has no effect until configured. The figure below shows an example of an output enable mapping scheme that is register configurable and can be stored in NVM as the default at power-up.

Enabling and disabling outputs can also be controlled by register control. This allows disabling one or more output when the OEb pin(s) has them enabled. By default the output enable register settings are configured to allow the OEb pins to have full control.



In its default state the OE0b pin enables/disables all outputs. The OE1b and OE2b pins are not mapped and have no effect on outputs.



An example of a configurable output enable scheme. In this case OE0b controls the outputs associated with DSPLL A, OE1b controls the outputs for DSPLL C, and OE2b controls the outputs for DSPLL D.

Figure 3.21. Example of Configuring Output Enable Pins

3.9.11 Output Disable During LOL

By default a DSPLL that is out of lock will generate either free-running clocks or generate clocks in holdover mode. There is an option to disable the outputs when a DSPLL is LOL. This option can be useful to force a downstream PLL into holdover.

3.9.12 Output Disable During XAXB_LOS

The internal oscillator circuit (OSC) in combination with the external crystal (XTAL) provides a critical function for the operation of the DSPLLs. In the event of a crystal failure the device will assert an XAXB_LOS alarm. By default all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability will be indeterminate during this fault condition.

3.9.13 Output Driver State When Disabled

The disabled state of an output driver is register configurable as disable low or high.

3.9.14 Synchronous/Asynchronous Output Disable

Outputs can be configured to disable synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode, the output clock will disable immediately without waiting for the period to complete.

3.9.15 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the hard reset bit will have the same result.

3.10 Power Management

Unused inputs, output drivers, and DSPLLs can be powered down when unused.

3.11 In-Circuit Programming

The Si5348 is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible.

3.12 Serial Interface

Configuration and operation of the Si5348 is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire mode.

3.13 Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed part will generate clocks at power-up. Custom, factory-pre-programmed devices are available. Use the ClockBuilder Pro custom part number wizard (https://www.skyworksinc.com/en/application-pages/clockbuilder-pro-software) to quickly and easily request and generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Skyworks sales representative. Samples of your pre-programmed device will typically ship in about two weeks.

3.14 Enabling Features and/or Configuration Settings Not Available in ClockBuilder Pro for Factory Pre-programmed Devices

As with essentially all modern software utilities, ClockBuilder Pro is continuously updated and enhanced. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the Si5348 Reference Manual.

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is not yet available in CBPro, you must contact a Skyworks Support for assistance. One example of this type of feature or custom setting is the customizable output amplitude and common voltages for the clock outputs. After careful review of your project file and requirements, the Skyworks applications engineer will email back your CBPro project file with your specific features and register settings enabled using what is referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown in the table below:

Table 3.4. Setting Overrides

Location	Name	Type	Target	Dec Value	Hex Value
0×0435[0]	FORCE_HOLD_PLLA	No NVM	N/A	1	0×1
0×0B48[4:0]	OOF_DIV_CLK_DIS	User	OPN and EVB	31	0×1F

Once you receive the updated design file, simply open it in CBPro. The device will begin operation after startup with the values in the NVM file. The flowchart for this process is shown in the figure below:

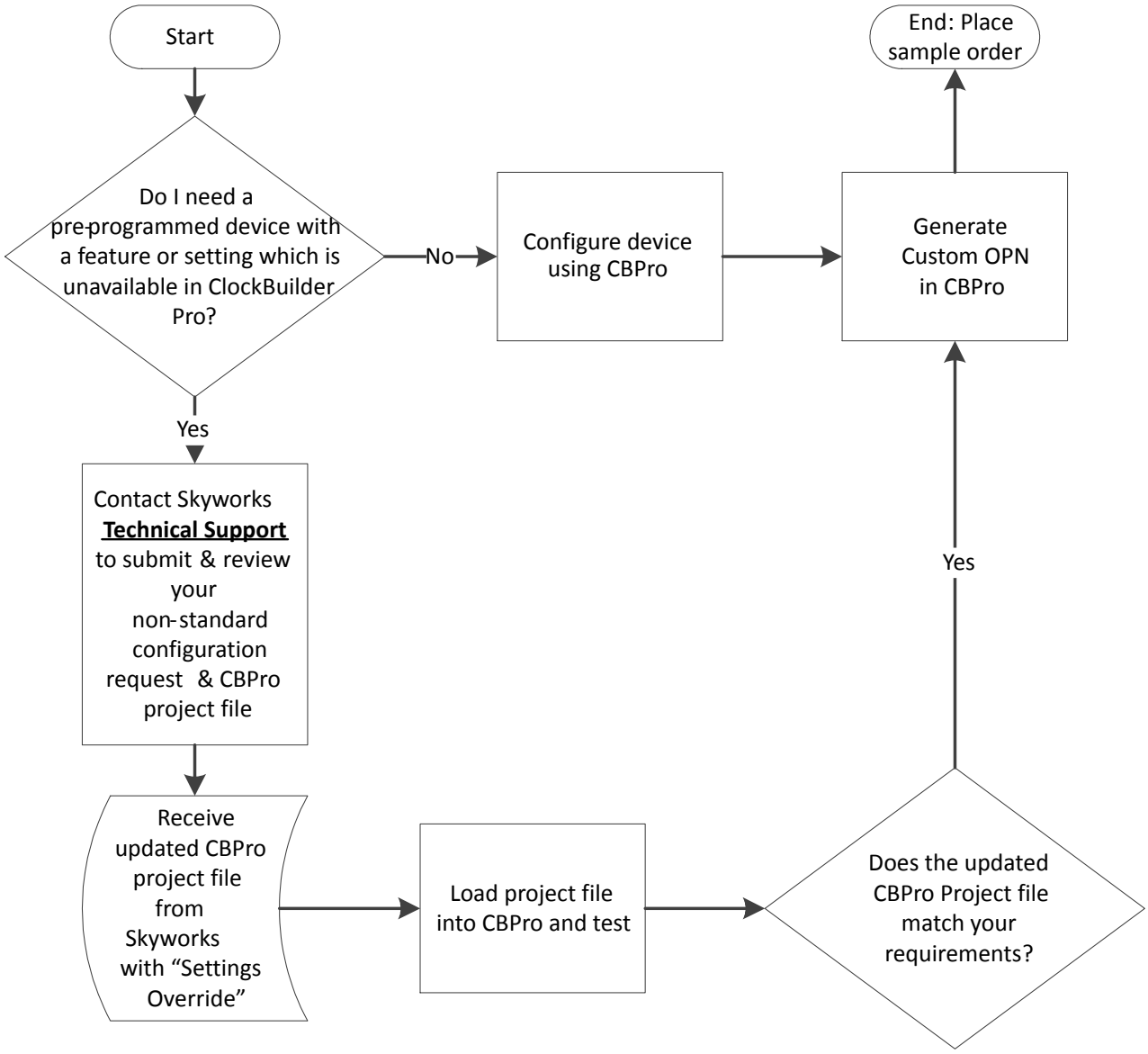


Figure 3.22. Process for Requesting Non-Standard CBPro Features

Note: Contact Skyworks Technical Support at https://www.skyworksinc.com/en/Support.

4. Register Map

Refer to the Si5348 Reference Manual for a complete list of register descriptions and settings.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.37	2.50	2.62	V
		1.71	1.80	1.89	V
Status Pin Supply Voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

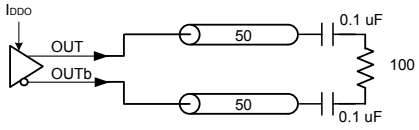
Table 5.2. DC Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current[1]	I_{DD}		—	290	460	mA
	I_{DDA}		—	125	145	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[2] @ 156.25 MHz	—	22	26	mA
		LVDS Output[2] @ 156.25 MHz	—	15	18	mA
		3.3 V LVCMOS[3] output @ 156.25 MHz	—	22	30	mA
		2.5 V LVCMOS[3] output @ 156.25 MHz	—	18	23	mA
		1.8 V LVCMOS[3] output @ 156.25 MHz	—	12	16	mA
Total Power Dissipation[1, 4]	P_d	Si5348	—	1250	1600	mW

Note:

1. Si5348 test configuration: 7 x 2.5 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Differential outputs terminated into an AC coupled 100 Ω load.
3. LVCMOS outputs measured into a 5-inch 50 Ω PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, which is the strongest driver setting. Refer to the Si5348 Reference Manual for more details on register settings.
4. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Differential Output Test Configuration



LVCMOS Output Test Configuration

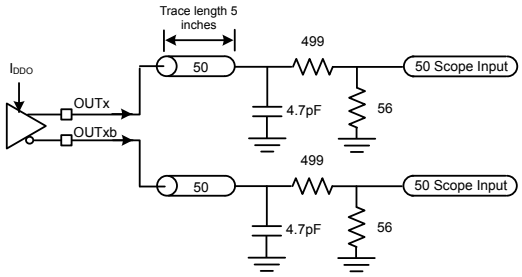


Table 5.3. Input Clock Specifications

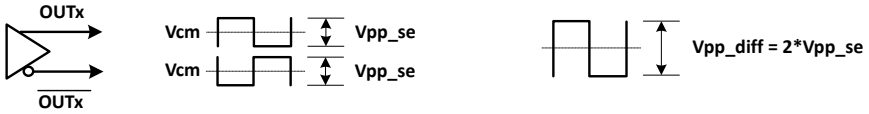
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Input Buffer (IN0, IN1, IN2, REF)						
Input Frequency Range	f_{IN_DIFF}	Differential	0.008	—	750	MHz
		Single-ended/LVCMOS	0.008	—	250	
		REF	5	—	250	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage Swing [1]	V_{IN}	Differential AC-coupled f_{IN}< 250 MHz	100	—	1800	mVpp_se
		Differential AC-coupled 250 MHz < f_{IN}< 750 MHz	225	—	1800	mVpp_se
		Single-ended AC-coupled f_{IN} < 250 MHz	100	—	3600	mVpp_se
Slew Rate[2,3]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Input Capacitance	C_{IN}		—	2.4	—	pF
Input Resistance Differential	R_{IN_DIFF}		—	16	—	kΩ
Input Resistance Single-ended	R_{IN_SE}		—	8	—	kΩ
Pulsed CMOS Input Buffer - DC-coupled (IN0, IN1, IN2)[4]						
Input Frequency	$f_{IN\_PULSED\_CMOS}$		0.008	—	250	MHz
Input Voltage	V_{IL}		–0.2	—	0.4	V
	V_{IH}		0.8	—	—	V
Slew Rate[2,3]	SR		400	—	—	V/µs
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
LVCMOS Input Buffer - AC/DC Coupled (IN3, IN4)						
Input Frequency	f_{IN_CMOS}		0.008	—	2.048	MHz
Input Voltage	V_{IL}		—	—	0.3 x V_{DDIO}[5]	V
	V_{IH}		0.7 x V_{DDIO}[5]	—	—	V
Minimum Pulse Width	PW	Pulse Input	50	—	—	ns
Input Resistance	R_{IN}		—	20	—	kΩ
REFCLK (Applied to XA/XB)						
REFCLK Frequency	f_{IN_REF}	Full operating range. Jitter performance may be reduced.	24.97	—	54.06	MHz
		Range for best jitter.	48	—	54	MHz
		TCXO frequency for SyncE applications. Jitter performance may be reduced.	—	40	—	MHz
Input Single-ended Voltage Swing	V_{IN_SE}		365	—	2000	mVpp_se
Input Differential Voltage Swing	V_{IN_DIFF}		365		2500	mVpp_diff
Slew Rate[2, 3]	SR		400	—	—	V/µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Voltage swing is specified as single-ended mVpp.



2. Recommended for specified jitter performance. Jitter performance can degrade if the minimum slew rate specification is not met (see the Family Reference Manual).
3. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 - 0.2) \times V_{IN\_Vpp\_se}) / SR$.
4. Pulsed CMOS mode is intended primarily for single-ended LVCMOS input clocks < 1 MHz, which must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low frequency video frame sync pulse. Since the input thresholds (V_{IL}, V_{IH}) of this buffer are non-standard (0.4 and 0.8 V, respectively), refer to the input attenuator circuit for DC-coupled Pulsed LVCMOS in the Si5348 Reference Manual. Otherwise, for standard LVCMOS input clocks, use the Standard AC-coupled, Single-ended input mode.
5.

Table 5.4. Control Input Pin Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5348 Control Input Pins (I2C_SEL, A0/CSb, A1/SDO, SDA/SDIO, SCLK, RSTb, OE0b, OE1b, OE2b, FINC)						
Input Voltage	V_{IL}		—	—	0.3 × V_{DDIO}[1]	V
	V_{IH}		0.7 × V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	1.5	—	pF
Input Resistance	R_L		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb, FINC	100	—	—	ns
Update Rate	F_{UR}	FINC	—	—	1	MHz
Si5348 Control Input Pin (FDEC)						
Input Voltage	V_{IL}		—	—	0.3 × V_{DDS}	V
	V_{IH}		0.7 × V_{DDS}	—	—	V
Input Capacitance	C_{IN}		—	1.5	—	pF
Minimum Pulse Width	PW	FDEC	100	—	—	ns
Update Rate	F_{UR}	FDEC	—	—	1	MHz

Note:
1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.

Table 5.5. Differential Clock Output Specifications

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	718.5	MHz
	f_{OUT1Hz}	1 PPS signal only available on Output 6			1		Hz
Duty Cycle	DC	f_{OUT} < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} < 718.5 MHz		45	—	55	%
Output-Output Skew Using Same DSPLL	T_{SKS}	Outputs on same DSPLL (Measured at 712.5 MHz)		—	0	75	ps
OUT-OUTb Skew	T_{SK_OUT}	Measured from the positive to negative output pins		—	0	50	ps
Output Voltage Amplitude[1]	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	350	430	510	mVpp_se
			LVPECL	640	750	900	

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Common Mode Voltage[1]	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.10	1.20	1.30	V
			LVPECL	1.90	2.00	2.10	
		V_{DDO} = 2.5 V	LVPECL, LVDS	1.10	1.20	1.30	V
		V_{DDO} = 1.8 V	sub-LVDS	0.80	0.90	1.00	V
Rise and Fall Times (20% to 80%)	t_R/t_F			—	100	150	ps
Differential Output Impedance	Z_O			—	100	—	Ω
Power Supply Noise Rejection[2]	PSRR	10 kHz sinusoidal noise		—	–101	—	dBc
		100 kHz sinusoidal noise		—	–96	—	dBc
		500 kHz sinusoidal noise		—	–99	—	dBc
		1 MHz sinusoidal noise		—	–97	—	dBc
Output-output Crosstalk[3]	XTALK			—	–72	—	dBc

Note:

1. Output amplitude and common mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. Note that the maximum LVDS single-ended amplitude can be up to 110 mV higher than the TIA/EIA-644 maximum. Refer to the Si5348 Reference Manual for recommended settings. Not all combinations of voltage amplitude and common mode voltages settings are possible.
2. Measured for 156.25 MHz carrier frequency. 100 mVpp of sinewave noise added to VDDO running at 3.3 V and noise spur amplitude measured.
3. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to "AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems" for guidance on minimizing crosstalk. Note that all active outputs must be terminated when measuring crosstalk.

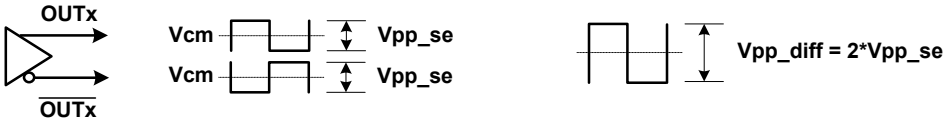


Table 5.6. LVCMOS Clock Output Specifications

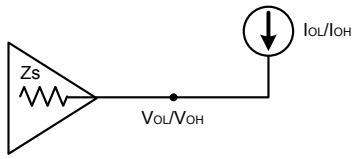
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	250	MHz
	f_{OUT1Hz}	Only Available on Output 6			1		Hz
Duty Cycle	DC	f_{OUT} <100 MHz		48	—	52	%
		100 MHz < f_{OUT} < 250 MHz		45	—	55	
Output Voltage High[1, 2, 3]	V_{OH}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OH} = –10 mA	V_{DDO} × 0.85	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = –12 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = –17 mA		—	—	
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OH} = –6 mA	V_{DDO} × 0.85	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = –8 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = –11 mA		—	—	
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OH} = –4 mA	V_{DDO} × 0.85	—	—	V
		OUTx_CMOS_DRV=3	I_{OH} = –5 mA		—	—	
Output Voltage Low[1, 2, 3]	V_{OL}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OL} = 10 mA	—	—	V_{DDO} × 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 12 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OL} = 6 mA	—	—	V_{DDO} × 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 8 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OL} = 4 mA	—	—	V_{DDO} × 0.15	V
		OUTx_CMOS_DRV=3	I_{OL} = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	V_{DDO} = 3.3 V		—	400	600	ps
		V_{DDO} = 2.5 V		—	450	600	ps
		V_{DDO} = 1.8 V		—	550	750	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

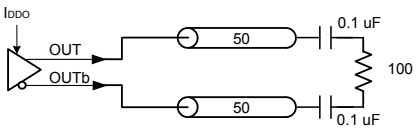
1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5348 Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.

DC Test Configuration



3. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, at 156.25 MHz.

Differential Output Test Configuration



LVCMOS Output Test Configuration

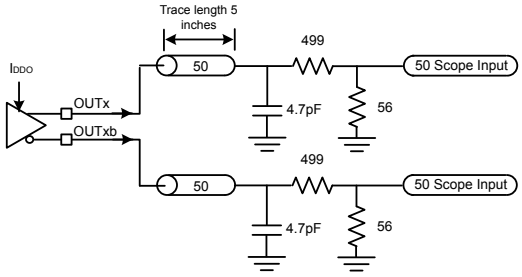


Table 5.7. Output Status Pin Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5348 Status Output Pins (LOL_Cb, LOL_Db, INTRb, LOS1b, LOS2b, SDA/SDIO[2], A1/SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[1] × 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[1] × 0.15	V
Si5348 Status Output Pins (LOL_Ab, LOS0b)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} × 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} × 0.15	V

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. Users normally select this option in the ClockBuilder Pro GUI. Alternatively, refer to the Si5348 Reference Manual for more details on register settings.
2. The V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I^2C mode or is unused with I2C_SEL pulled high. V_{OL} remains valid in all cases.

Table 5.8. Performance Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Loop Bandwidth Programming Range[1]	f_{BW}		0.001	—	4000	Hz
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates free-running clocks	—	30	45	ms
PLL Lock Time[2]	t_{ACQ}	With Fastlock enabled	—	280	300	ms
POR to Serial Interface Ready[3]	t_{RDY}		—	—	15	ms
Jitter Peaking	J_{PK}	Measured with a frequency plan running a 25 MHz input, 25 MHz output, and a loop bandwidth of 4 Hz	—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1&2 Carrier Frequency = 10.3125 GHz Jitter Modulation Frequency = 10 Hz	—	3180	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch	t_{SWITCH}	Manual or automatic switch between two input clocks at same frequency.[5]	—	—	1.2	ns
Pull-in Range	ω_P		—	500	—	ppm
RMS Phase Jitter[4]	J_{GEN}	12 kHz to 20 MHz	—	100	150	fs rms

Note:

1. Actual loop bandwidth might be lower; refer to CBPro for actual value on your frequency plan.
2. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with fastlock bandwidth set to 100 Hz, LOL set/clear thresholds of 3/0.3 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator de-assertion.
3. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.
4. Jitter generation test conditions: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz LVPECL. (Does not include jitter from input reference).
5. For input frequency configurations, which have Fpfd > 1 MHz. Consult your CBPro Design report for the Fpfd frequency of your configuration.
6. Measured from input to one or more outputs with the same input and output frequencies.

Table 5.9. I^2C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
SMBus Timeout	—		25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		100	—	100	—	ns
Data set-up time	$t_{SU:DAT}$		250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r		—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f		—	300	—	300	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

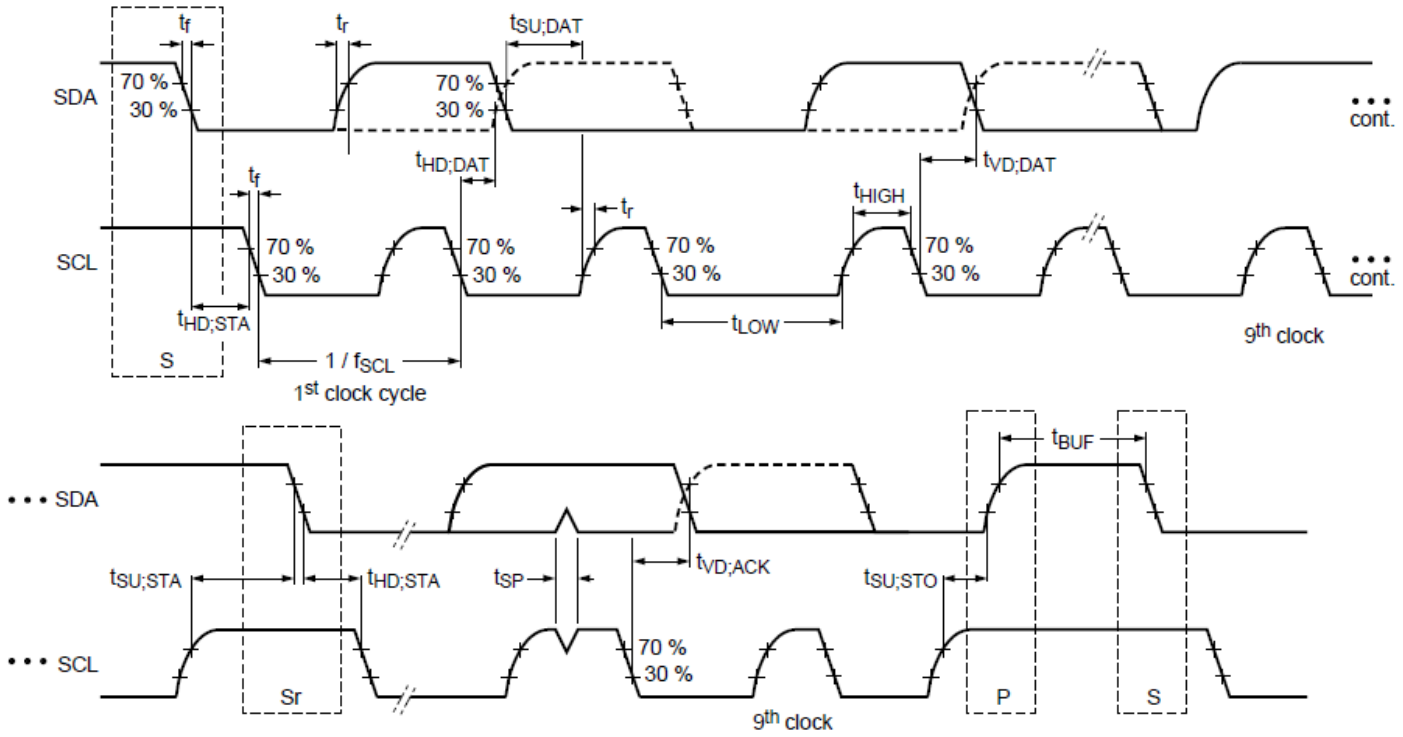


Figure 5.1. I²C Serial Port Timing Standard and Fast Modes

Table 5.10. SPI Timing Specifications (4-Wire)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	—	18	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	—	15	ns
Delay Time, CSb Rise to SDIO Tri-State	T_{D3}	—	—	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	2	—	—	T_C

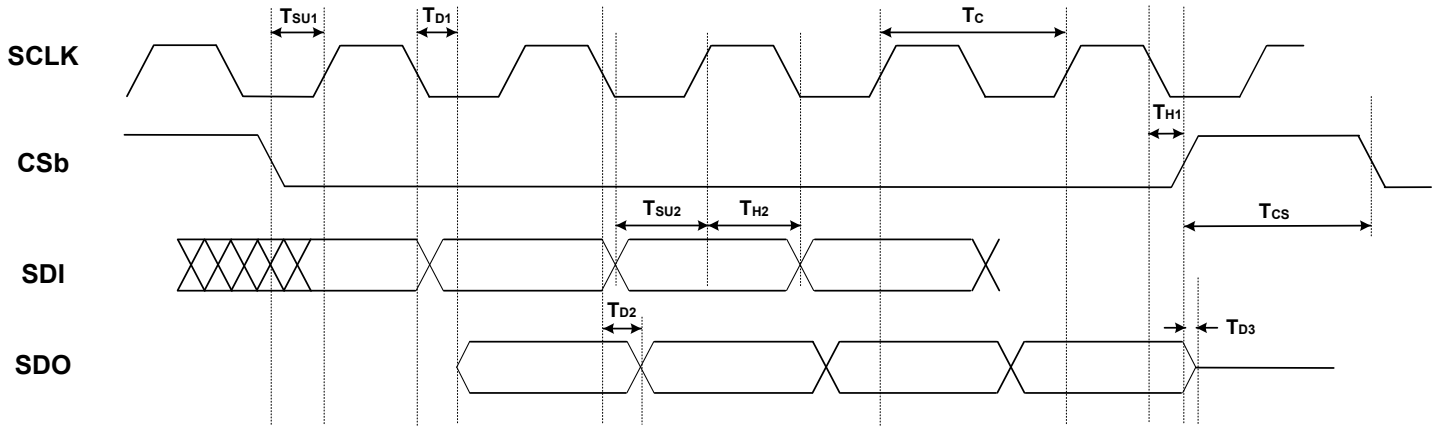


Figure 5.2. 4-Wire SPI Serial Interface Timing

Table 5.11. SPI Timing Specifications (3-Wire)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	—	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	—	15	ns
Delay Time, CSb Rise to SDIO Tri-State	T_{D3}	—	—	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	2	—	—	T_C

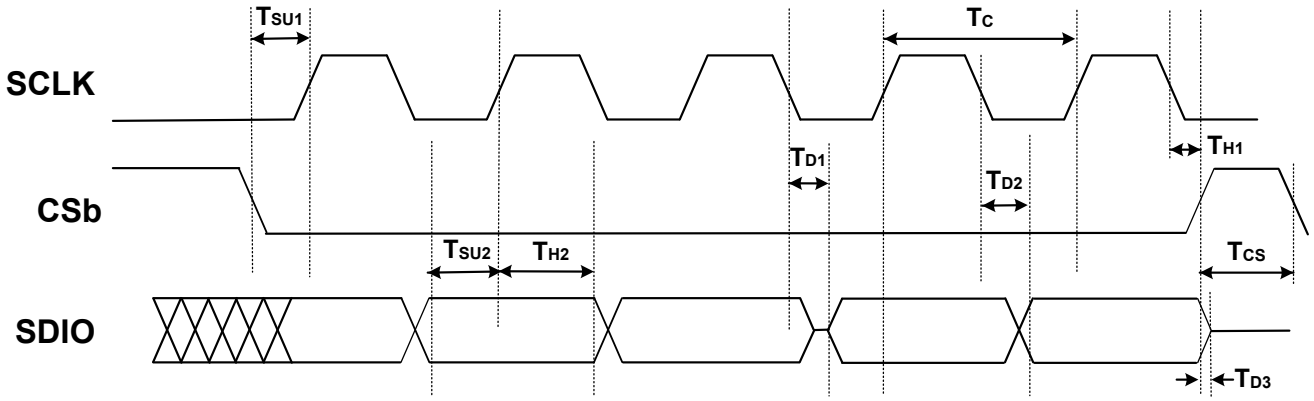


Figure 5.3. 3-Wire SPI Serial Interface Timing

Table 5.12. Crystal Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency Range	f_{XTAL}		48	—	54	MHz
Load Capacitance	C_L		—	8	—	pF
Crystal Drive Level	d_L		—	—	200	µW
Equivalent Series Resistance Shunt Capacitance	r_{ESR} C_O	Refer to the Family Reference Manual to determine ESR and shunt capacitance.				

Note:

1. Refer to the Si534x/8x Recommended Crystal, TCXO and OCXOs Reference Manual for recommended 48 to 54 MHz crystals. The Si5348 is designed to only work with crystals that meet these specifications and not with XOs.

Table 5.13. Thermal Characteristics

Parameter	Symbol	Test Condition[1]	Value	Unit
Si5348-64QFN				
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	Θ_{JC}		9.5	
Thermal Resistance Junction to Board	Θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	

Note:

1. Based on PCB Dimension: 3" x 4.5", PCB Thickness: 1.6 mm, PCB Land/Via: 36, Number of Cu Layers: 4.

Table 5.14. Absolute Maximum Ratings[1, 2, 3, 4,]

Parameter	Symbol	Test Condition	Value	Unit
Storage Temperature Range	T_{STG}		–55 to 150	°C
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDS}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}[5]	IN0 - IN4, REF	–1.0 to V_{DDA} + 0.3	V
	V_{I2}	RSTb, OE0b, OE1b, OE2b, I2C_SEL,FINC, FDEC, A1/SDO, SDA/SDIO, SCLK, A0/CSb,	–0.5 to V_{DDA} + 0.3	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Max Junction Temperature in Operation	T_{JCT}		125	°C
Soldering Temperature (Pb-free profile)[3]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[4]	T_P		20-40	s

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN package is RoHS-6 compliant.
3. For detailed MSL and packaging information, go to https://www.skyworksinc.com/en/Support.
4. The device is compliant with JEDEC J-STD-020.
5. The minimum voltage at these pins can be as low as –1.0 V when an ac input signal of 8 kHz or greater is applied. See Table 5.3 Input Clock Specifications on page 30 spec for Single-Ended AC-Coupled f_{IN} < 250 MHz.

6. Typical Application Schematic

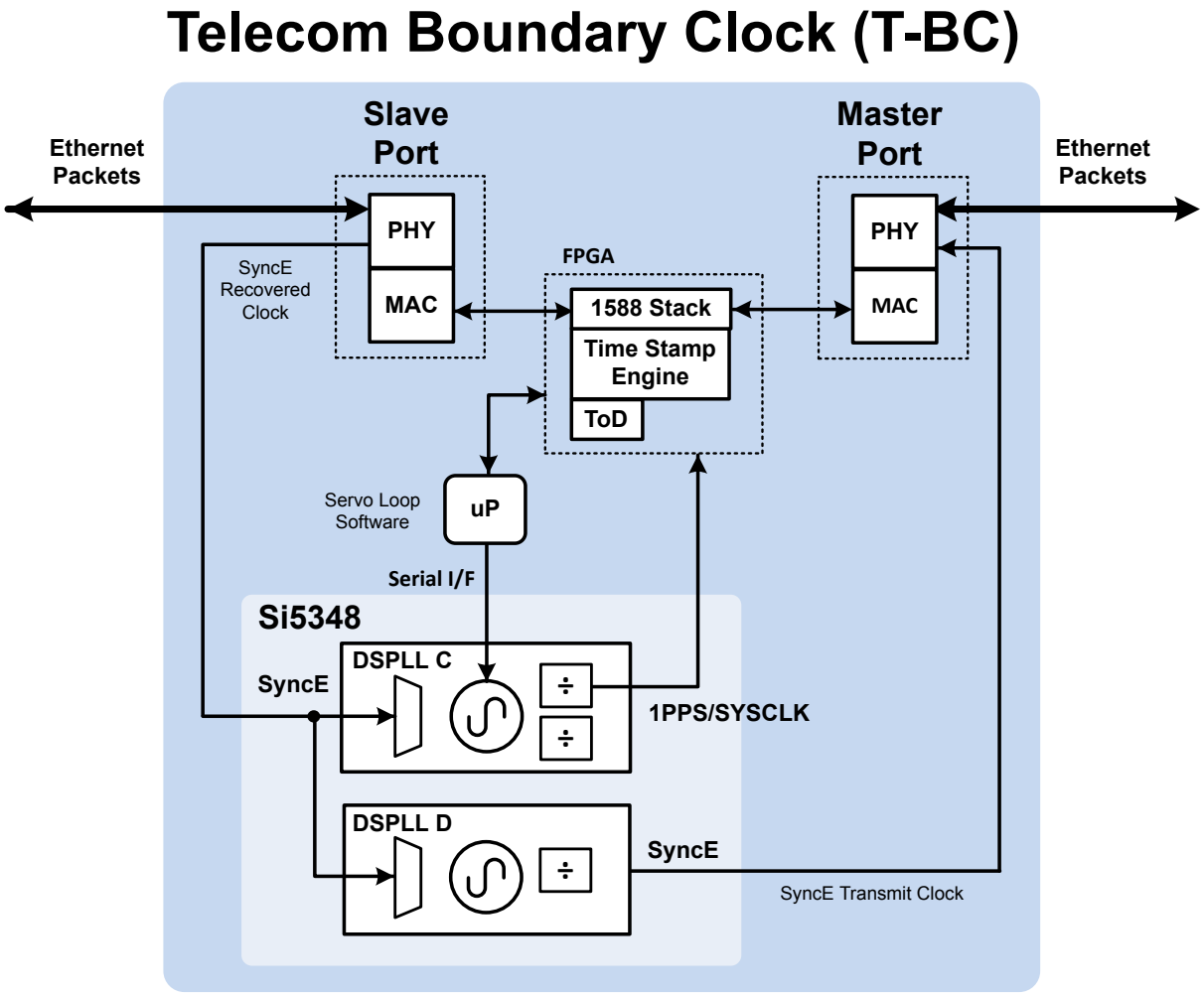


Figure 6.1. Using the Si5348 as a Telecom Boundary Clock

7. Detailed Block Diagram

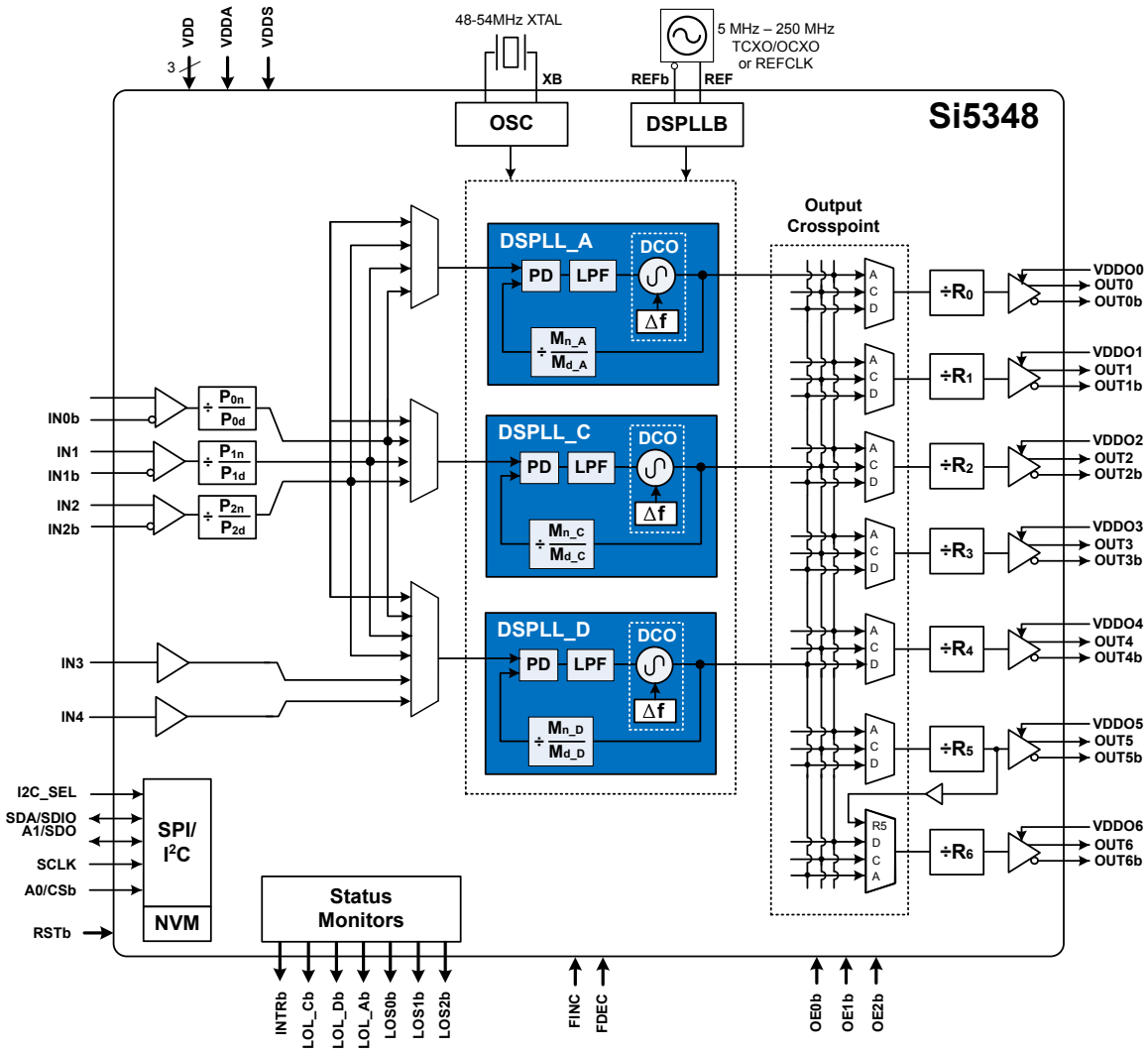


Figure 7.1. Si5348 Detailed Block Diagram

8. Typical Operating Characteristics (Jitter and Phase Noise)

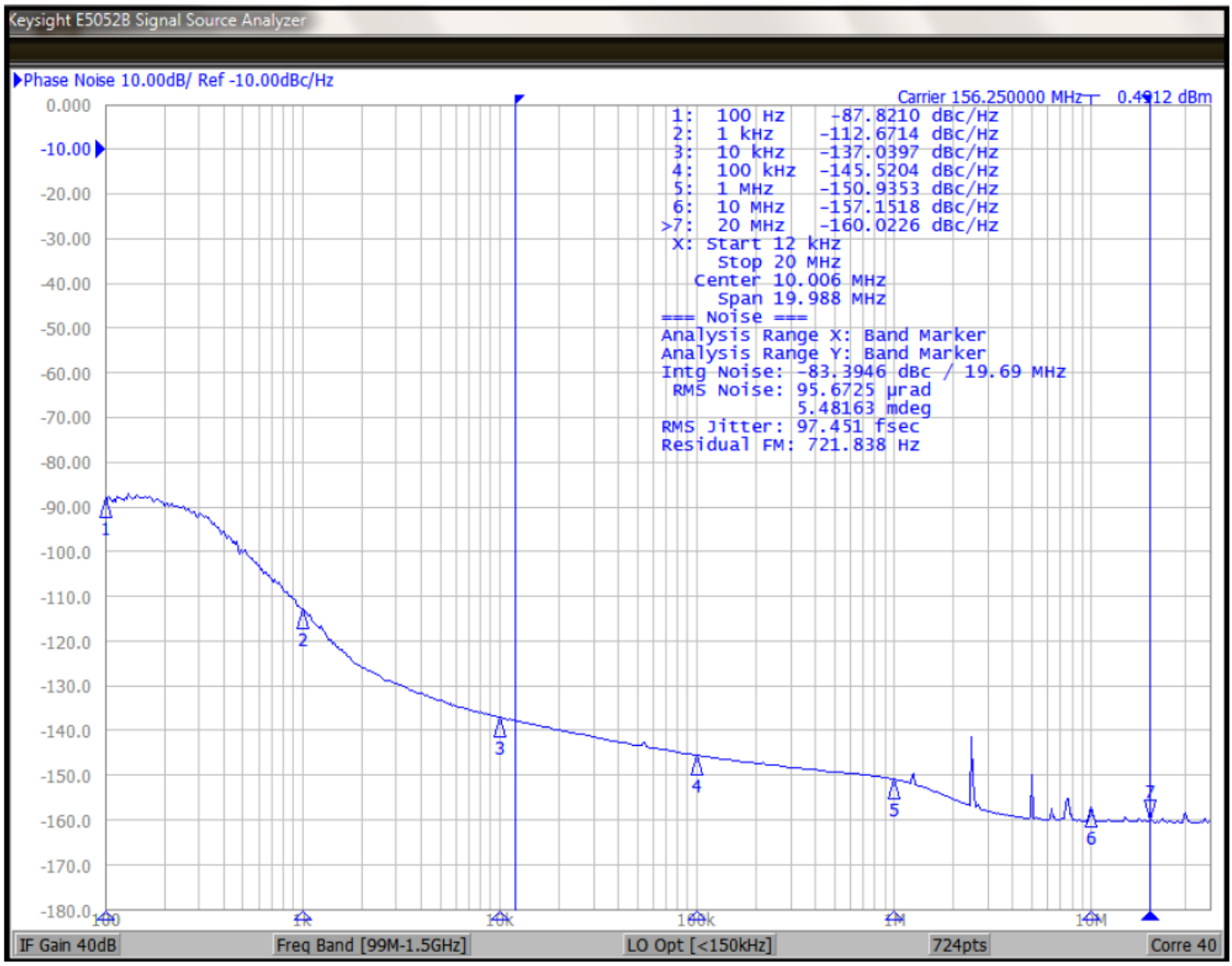


Figure 8.1. Input = 25 MHz; Output = 156.25 MHz, 2.5 V LVDS with Rakon 12.8 MHz Reference

9. Pin Descriptions

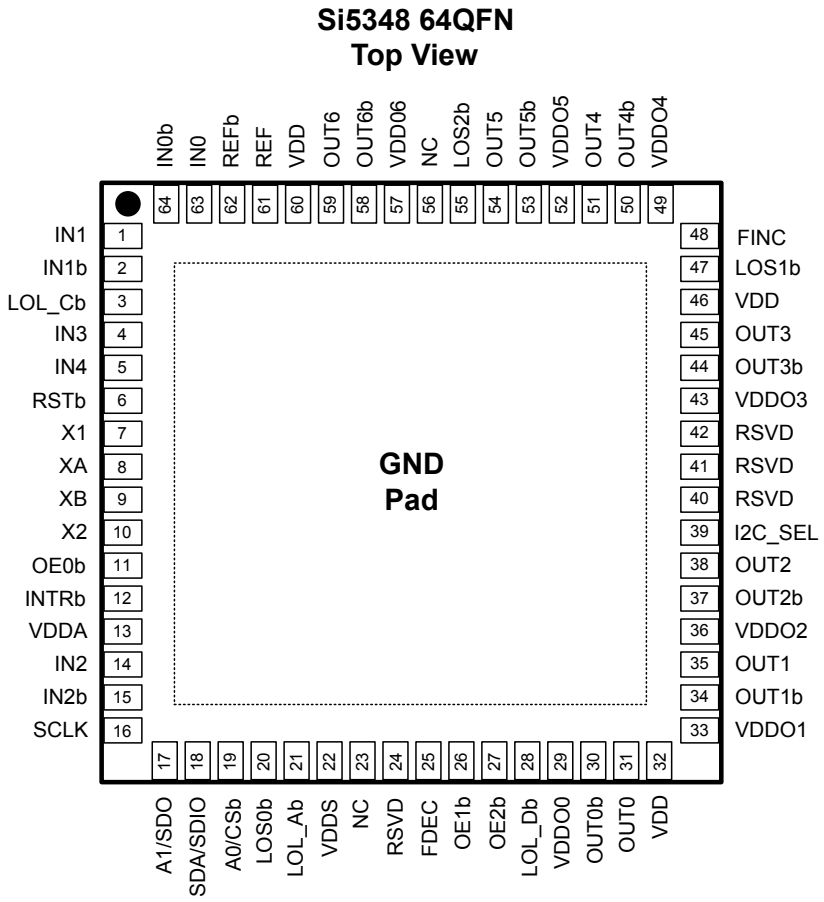


Figure 9.1. Si5348 Pin Descriptions

Table 9.1. Si5348 Pin Descriptions [1]

Pin Name[1]	Pin Number	Pin Type [2]	Function
Inputs			
XA	8	I	**Crystal Input**. Input pin for external crystal (XTAL).
XB	9	I	
X1	7	I	**XTAL Shield**. Connect these pins directly to the XTAL ground pins. The XTAL ground pins should be separated from the PCB ground plane. Refer to the Si5348 Reference Manual for layout guidelines.
X2	10	I	
IN0	63	I	**Clock Inputs**. IN0-IN2 accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to Input Configuration and Terminations input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded through a capacitor when accepting a single-ended clock. IN3 and IN4 only support single ended LVCMOS signals.These pins are high-impedance and must be terminated externally. Unused inputs can be disabled by register configuration and the pins left unconnected.
IN0b	64	I	
IN1	1	I	
IN1b	2	I	
IN2	14	I	
IN2b	15	I	
IN3	4	I	
IN4	5	I	
REF	61	I	**Reference Input**. This input accepts a reference clock from a stable source (eg. TCXO or OCXO) that is used to determine free-run frequency accuracy and stability during free-run or holdover of the DSPLL or DCO. These inputs can accept differential or single-ended connections. Refer to the Si5348 Reference Manual for recommended TCXOs and OCXOs.
REFb	62	I	
Outputs			
OUT0	31	O	**Output Clocks**. These output clocks support a programmable signal amplitude and common mode voltage. Desired output signal format is configurable using register control.Termination recommendations are provided in Figure 3.19 Supported Differential Output Terminations on page 22. Unused outputs should be left unconnected.
OUT0b	30	O	
OUT1	35	O	
OUT1b	34	O	
OUT2	38	O	
OUT2b	37	O	
OUT3	45	O	
OUT3b	44	O	
OUT4	51	O	
OUT4b	50	O	
OUT5	54	O	
OUT5b	53	O	
OUT6	59	O	
OUT6b	58	O	
Serial Interface			
I2C_SEL	39	I	**I2C Select**[3]. This pin selects the serial interface mode as I^2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled up to the voltage selected by the IO_VDD_SEL register bit. This pin is 3.3 V tolerant.

Pin Name[1]	Pin Number	Pin Type [2]	Function
SDA/SDIO	18	I/O	**Serial Data Interface[3]**. This is the bidirectional data pin (SDA) for the I^2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When not in SPI mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode unless the master SPI driver is open drain. This pin is 3.3 V tolerant.
A1/SDO	17	I/O	**Address Select 1/Serial Data Output[3]**. In I^2C mode this pin functions as the A1 address input pin and does not have an internal pull up or pull down resistor. In 4-wire SPI mode, this is the serial data output (SDO) pin. and drives high to the voltage selected by the IO_VDD_SEL pin. This pin is 3.3 V tolerant. This pin must be pulled up externally when unused.
SCLK	16	I	**Serial Clock Input[3]**. This pin functions as the serial clock input for both I^2C and SPI modes. This pin does not have an internal pull-up or pull-down. When in I^2C mode or unused, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode unless the SPI master driver is open drain. This pin is 3.3 V tolerant.
A0/CSb	19	I	**Address Select 0/Chip Select[3]**. This pin functions as the hardware controlled address A0 input pin in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up by a 20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit. This pin is 3.3 V tolerant.
Control/Status			
INTRb	12	O	**Interrupt[3]**. This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use.
RSTb	6	I	**Device Reset[3]**. Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up.
OE0b	11	I	**Output Enable 0-2[3]**. These output enable pins have a programmable register mask which allows them to control any of the output clocks. By default the OE0b pin enables all output clocks and OE1b, OE2b have no control over the output clocks until register configured. These pins are internally pulled low and can be left unconnected when not in use.
OE1b	26	I	
OE2b	27	I	
LOL_Ab	21	O	**Loss of Lock_A/C/D**. These output pins indicate when DSPLL A, C, D is out-of-lock (low) or locked (high). They can be left unconnected when not in use. For LOL_C and LOL_D, see Note 3. For LOL_A, see Note 4.
LOL_Cb	3	O	
LOL_Db	28	O	
LOS0b	20	O	**Loss of Signal for IN0, IN1, IN2**. These pins reflect the loss of signal register status bits for inputs (IN0, IN1, IN2). These pins can be left unconnected when not in use. For LOS_1 and LOS_2, see Note 3. For LOS_0, see Note 4.
LOS1b	47	O	
LOS2b	55	O	
FDEC	25	I	**Frequency Decrement Pin[4]**. This pin is used to step-down the output frequency of a selected DSPLL. The frequency change step size is register configurable. This pin does not have an internal pullup/pulldown and must be externally pulled when unused.

Pin Name[1]	Pin Number	Pin Type [2]	Function
FINC	48	I	**Frequency Increment Pin[3]**. This pin is used to step-up the output frequency of a selected DSPLL. The frequency change step size is register configurable. The DSPLL(s) affected by the frequency change is determined by the M_FSTEP_MSK_PLLx register settings. This pin is pulled low internally and can be left unconnected when not in use.
RSVD	24	-	**Reserved**. These pins are connected to the die. Leave disconnected.
	40	-	
	41	-	
	42	-	
NC	23	-	**No Connect**. These pins are not connected to the die. Leave disconnected.
	56	-	
Power			
VDD	32	P	**Core Supply Voltage**. The device core operates from a 1.8 V supply. See the Si5348 Reference Manual for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
	46		
	60		
VDDA	13	P	**Core Supply Voltage 3.3 V**. This core supply pin requires a 3.3 V power source. See the Si5348 Reference Manual for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
VDDS	22	P	**Status Output Voltage**. The voltage on this pin determines VOL/VOH on the LOL and LOS status output pins. Connect to either 3.3 V or 1.8 V. A 0.1 µF bypass capacitor should be placed very close to this pin.
VDDO0	29	P	**Output Clock Supply Voltage 0-6**. Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 0402 1 µF capacitor should be placed very near each of these pins.
VDDO1	33	P	
VDDO2	36	P	
VDDO3	43	P	
VDDO4	49	P	
VDDO5	52	P	
VDDO6	57	P	
GND PAD	-	P	**Ground Pad**. This pad provides connection to ground and must be connected for proper operation. Use as many vias as practical and keep the via length to an internal ground plan as short as possible.

Note:

1. Refer to the Si5348 Reference Manual for more information on register setting names.
2. I = Input, O = Output, P = Power.
3. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
4. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

10. Package Outline

The figure below illustrates the package details for the Si5348. The table below lists the values for the dimensions shown in the illustration.

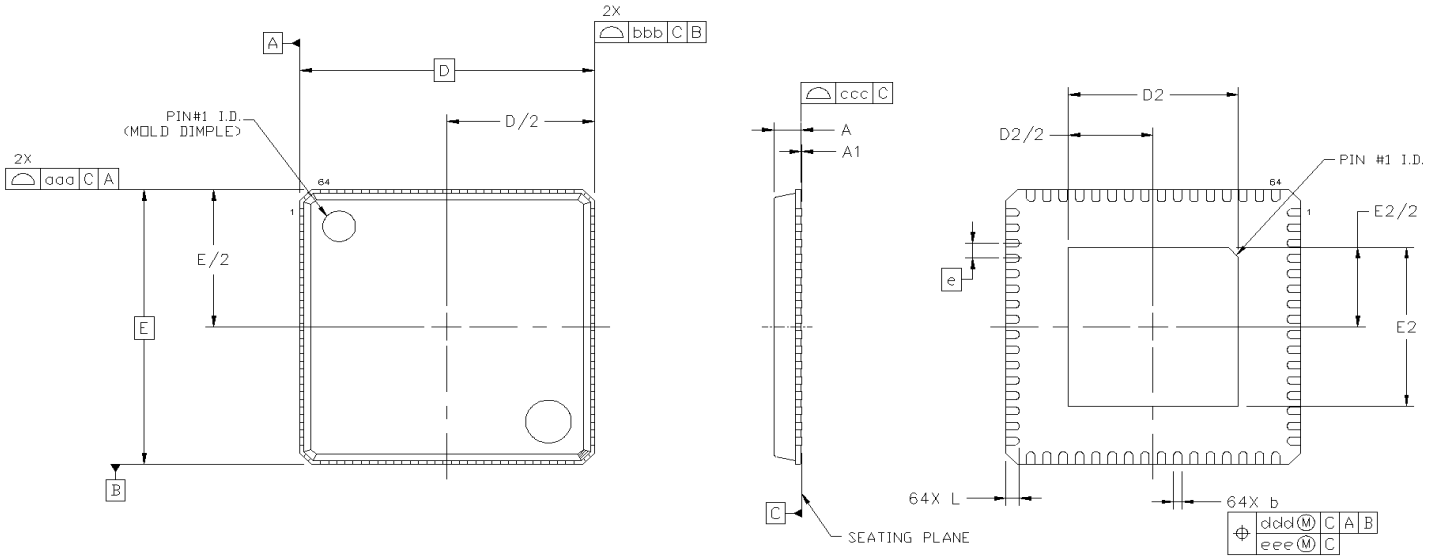


Figure 10.1. Si5348 9x9 mm 64-Pin Quad Flat No-Lead (QFN)

Table 10.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. PCB Land Pattern

The figure below illustrates the PCB land pattern details for the devices. The table below lists the values for the dimensions shown in the illustration. Refer to the Si5348 Reference Manual for information about thermal via recommendations.

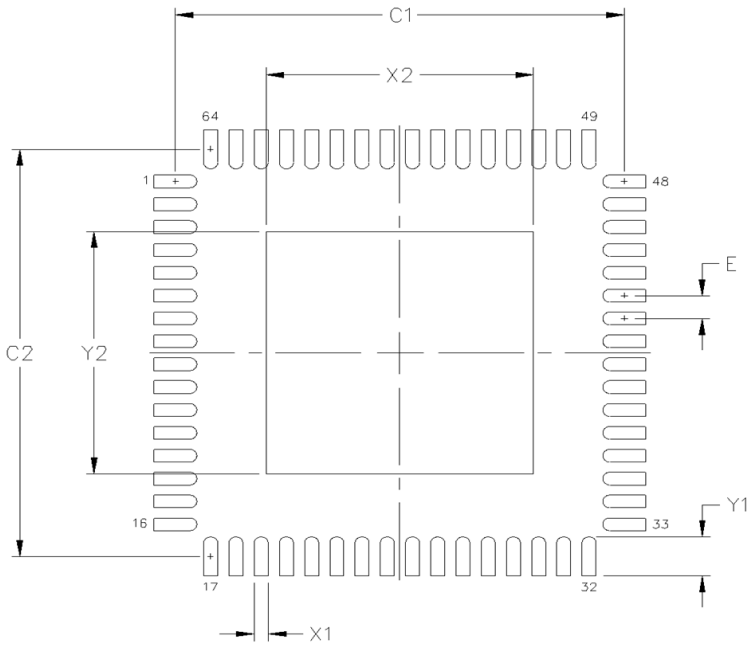


Figure 11.1. Si5348 PCB Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Dimension	Si5348 (Max)
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	5.30
Y2	5.30

Note:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 3x3 array of 1.25 mm square openings on 1.80 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Marking

Figure 12.1. Si5348 Top Marking

Table 12.1. Top Marking

Line	Characters	Description
1	Si5348g-	Base part number and Device Grade. Si5348: Packet Network Synchronizer for SyncE/1588; 64-QFN g = Device Grade. See 2. Ordering Guide for more information. – = Dash character.
2	Rxxxxx-GM	R = Product revision. (See 2. Ordering Guide for current revision.) xxxxx = Customer specific NVM sequence number. (Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices). See 2. Ordering Guide for more information. -GM = Package (QFN) and temperature range (–40 to +85 °C).
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.6 mm (64-QFN) diameter	Pin 1 indicator; left-justified
	e4	Pb-free symbol; Center-Justified
	TW	TW = Taiwan; Country of Origin (ISO Abbreviation)

13. Device Errata

Please go to https://www.skyworksinc.com/en to access the device errata document.

14. Revision History

Revision 1.1

October, 2018

- Updated Figure 3.5 Crystal Resonator Connections on page 11
- Updated Figure 3.6 External Reference Connections on page 12.
- Updated Figure 3.8 Termination of Differential and LVCMOS Input Signals on page 14.
- Updated Figure 3.19 Supported Differential Output Terminations on page 22.
- Updated Figure 3.20 LVCMOS Output Terminations on page 23.
- Updated Table 5.3 Input Clock Specifications on page 30.
  - Updated Input Capacitance specification typical value.
- Updated Table 5.5 Differential Clock Output Specifications on page 33.
  - Update Output-Output Skew Using Same DSPLL specification typical and max values.
- Updated Table 5.6 LVCMOS Clock Output Specifications on page 35.
  - Removed Output-to-Output Skew specification.
- Updated Table 5.8 Performance Characteristics on page 37.
  - Removed Input-to-Output Delay Variation specification.
- Updated Table 5.12 Crystal Specifications[1] on page 42.
- Updated Table 5.14 Absolute Maximum Ratings[1, 2, 3, 4,] on page 43.

Revision 1.0

July, 2016

- Initial release (See "AN1006: Differences between Si534x/8x Revision B and Revision D Silicon" for a list of changes from Rev B to Rev D.)

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