

19-OUTPUT PCIe GEN 3 BUFFER

Features

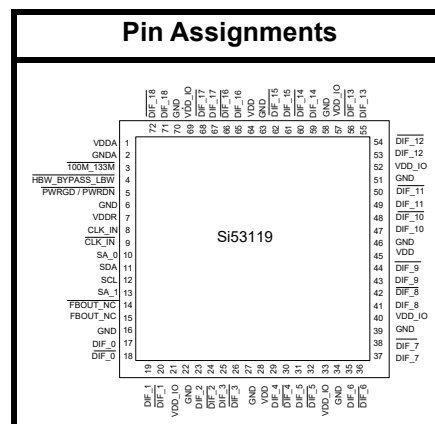
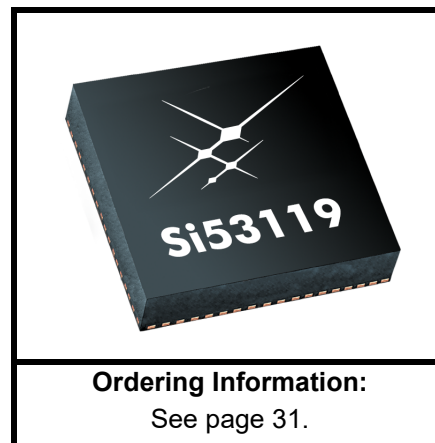
- Nineteen 0.7 V low-power, push-pull HCSL PCIe Gen 3 outputs
- 100 MHz /133 MHz PLL operation, supports PCIe and QPI
- PLL bandwidth SW SMBUS programming overrides the latch value from HW pin
- 9 selectable SMBUS addresses
- SMBus address configurable to allow multiple buffers in a single control network 3.3 V supply voltage operation
- Separate VDDIO for outputs
- PLL or bypass mode
- Spread spectrum tolerable
- 1.05 to 3.3 V I/O supply voltage
- 50 ps output-to-output skew
- 50 ps cyc-cyc jitter (PLL mode)
- Low phase jitter (Intel QPI, PCIe Gen 1/2/3 common clock compliant)
- Gen 3 SRNS Compliant
- 100 ps input-to-output delay
- Extended Temperature: -40 to 85 °C
- 72-pin QFN
- For variations of this device, contact Skyworks Solutions

Applications

- Server
- Storage
- Data center
- Enterprise switches and routers

Description

The Si53119 is a 19-output, low-power HCSL differential clock buffer that meets all of the performance requirements of the Intel DB1200ZL specification. The device is optimized for distributing reference clocks for Intel® QuickPath Interconnect (Intel QPI), PCIe Gen 1/Gen 2/Gen 3/Gen 4, SAS, SATA, and Intel Scalable Memory Interconnect (Intel SMI) applications. The VCO of the device is optimized to support 100 MHz and 133 MHz operation. Each differential output can be enabled through I²C for maximum flexibility and power savings. Measuring PCIe clock jitter is quick and easy with the Skyworks Solutions PCIe Clock Jitter Tool. Download it for free at <https://www.skyworksinc.com/en/application-pages/pci-express-learning-center>.



Patents pending

Functional Block Diagram

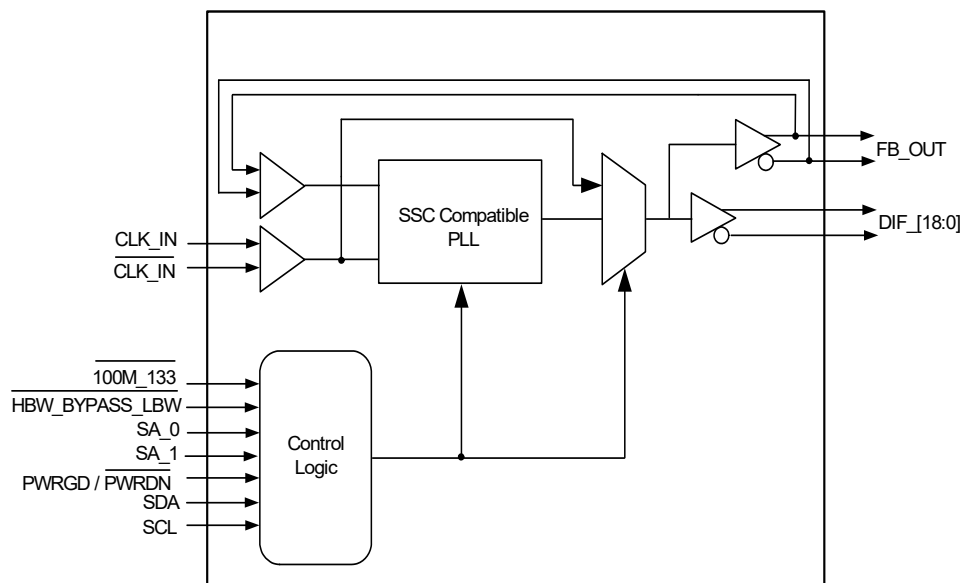


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1. Electrical Specifications

Table 1. DC Operating Characteristics
 $V_{DD_A} = 3.3\text{ V} \pm 5\%$, $V_{DD} = 3.3\text{ V} \pm 5\%$

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|--|---------------------|---------------------------|---------|---------|---------------|
| 3.3 V Core Supply Voltage | VDD/VDD_A | 3.3 V $\pm 5\%$ | 3.135 | 3.465 | V |
| 3.3 V I/O Supply Voltage ¹ | VDD_IO | 1.05 V to 3.3 V $\pm 5\%$ | 0.9975 | 3.465 | V |
| 3.3 V Input High Voltage | V _{IH} | VDD | 2.0 | VDD+0.3 | V |
| 3.3 V Input Low Voltage | V _{IL} | | VSS-0.3 | 0.8 | V |
| Input Leakage Current ² | I _{IL} | 0 < V _{IN} < VDD | -5 | +5 | μA |
| 3.3 V Input High Voltage ³ | V _{IH_FS} | VDD | 0.7 | VDD+0.3 | V |
| 3.3 V Input Low Voltage ³ | V _{IL_FS} | | VSS-0.3 | 0.35 | V |
| 3.3 V Input Low Voltage | V _{IL_Tri} | | 0 | 0.9 | V |
| 3.3 V Input Med Voltage | V _{IM_Tri} | | 1.3 | 1.8 | V |
| 3.3 V Input High Voltage | V _{IH_Tri} | | 2.4 | VDD | V |
| 3.3 V Output High Voltage ⁴ | V _{OH} | I _{OH} = -1 mA | 2.4 | — | V |
| 3.3 V Output Low Voltage ⁴ | V _{OL} | I _{OL} = 1 mA | — | 0.4 | V |
| Input Capacitance ⁵ | C _{IN} | | 2.5 | 4.5 | pF |
| Output Capacitance ⁵ | C _{OUT} | | 2.5 | 4.5 | pF |
| Pin Inductance | L _{PIN} | | — | 7 | nH |
| Ambient Temperature | T _A | No Airflow | -40 | 85 | °C |

Notes:

1. VDD_IO applies to the low-power NMOS push-pull HCSL compatible outputs.
2. Input Leakage Current does not include inputs with pull-up or pull-down resistors. Inputs with resistors should state current requirements.
3. Internal voltage reference is to be used to guarantee V_{IH_FS} and V_{IL_FS} threshold levels over full operating range.
4. Signal edge is required to be monotonic when transitioning through this region.
5. Ccomp capacitance based on pad metallization and silicon device capacitance. Not including pin capacitance.

Table 2. SMBus Characteristics

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|--|--------------|--|-----|-------------|------|
| SMBus Input Low Voltage ¹ | V_{ILSMB} | | | 0.8 | V |
| SMBus Input High Voltage ¹ | V_{IHSMB} | | 2.1 | V_{DDSMB} | V |
| SMBus Output Low Voltage ¹ | V_{OLSMB} | @ I_{PULLUP} | | 0.4 | V |
| Nominal Bus Voltage ¹ | V_{DDSMB} | @ V_{OL} | 2.7 | 5.5 | V |
| SMBus sink Current ¹ | I_{PULLUP} | 3 V to 5 V +/-10% | 4 | | mA |
| SCLK/SDAT Rise Time ¹ | t_{RSMB} | (Max $V_{IL} - 0.15$) to (Min $V_{IH} + 0.15$) | | 1000 | ns |
| SCLK/SDAT Fall Time ¹ | t_{FSMB} | (Min $V_{IH} + 0.15$) to (Max $V_{IL} - 0.15$) | | 300 | ns |
| SMBus Operating Frequency ^{1,2} | f_{MINSMB} | Minimum Operating Frequency | 100 | | kHz |

Notes:

1. Guaranteed by design and characterization
2. The differential input clock must be running for the SMBus to be active

Table 3. Current Consumption

$T_A = -40$ – 85 °C; supply voltage $V_{DD} = 3.3$ V $\pm 5\%$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------|-----------------|--------------------------------------|-----|------|-----|------|
| Operating Current | IDD_{VDD} | 100 MHz, VDD Rail | — | 25 | 35 | mA |
| | IDD_{VDDA} | 100 MHz, VDDA + VDDR, PLL Mode | — | 16 | 20 | mA |
| | IDD_{VDDIO} | 100 MHz, CL = Full Load, VDD IO Rail | — | 130 | 150 | mA |
| Power Down Current | IDD_{VDDPD} | Power Down, VDD Rail | — | 1.5 | 2 | mA |
| | IDD_{VDDAPD} | Power Down, VDDA Rail | — | 8 | 12 | mA |
| | $IDD_{VDDIOPD}$ | Power Down, VDD_IO Rail | — | 0.17 | 0.5 | mA |

Table 4. Clock Input Parameters

T_A = -40–85 °C; supply voltage V_{DD} = 3.3 V ±5%

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------|--------------------|--|--------------------------|--------|------|------|
| Input High Voltage | V _{IHDIF} | Differential Inputs (singled-ended measurement) | 600 | 700 | 1150 | mV |
| Input Low Voltage | V _{IHDIF} | Differential Inputs (singled-ended measurement) | V _{ss} - 300 | 0 | 300 | mV |
| Input Common Mode Voltage | V _{com} | Common mode input voltage | 300 | | 1000 | mV |
| Input Amplitude, CLK_IN | V _{swing} | Peak to Peak Value | 300 | | 1450 | mV |
| Input Slew Rate, CLK_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns |
| Input Duty Cycle | | Measurement from differential wave form | 45 | 50 | 55 | % |
| Input Jitter–Cycle to Cycle | J _{DFin} | Differential measurement | | | 125 | ps |
| Input Frequency | F _{ibyp} | VDD = 3.3 V, bypass mode | 33 | | 150 | MHz |
| | F _{iPLL} | VDD = 3.3 V, 100 MHz PLL Mode | 90 | 100 | 110 | MHz |
| | F _{iPLL} | VDD = 3.3 V, 133.33 MHz PLL Mode | 120 | 133.33 | 147 | MHz |
| Input SS Modulation Rate | fMODIN | Triangle wave modulation | 30 | 31.5 | 33 | kHz |

Table 5. Output Skew, PLL Bandwidth and PeakingT_A = -40–85 °C; supply voltage V_{DD} = 3.3 V ±5%

| Parameter | Test Condition | Min | TYP | Max | Unit |
|--------------------|---|------|-----|-----|------|
| CLK_IN, DIF[x:0] | Input-to-Output Delay in PLL Mode Nominal Value ^{1,2,3,4} | -100 | 18 | 100 | ps |
| CLK_IN, DIF[x:0] | Input-to-Output Delay in Bypass Mode Nominal Value ^{2,4,5} | 2.5 | 3.6 | 4.5 | ns |
| CLK_IN, DIF[x:0] | Input-to-Output Delay Variation in PLL mode Over Voltage and Temperature ^{2,4,5} | -50 | 20 | 50 | ps |
| CLK_IN, DIF[x:0] | Input-to-Output Delay Variation in Bypass Mode Over Voltage and Temperature ^{2,4,5} | -250 | | 250 | ps |
| DIF[11:0] | Output-to-Output Skew across all 19 Outputs (Common to Bypass and PLL Mode) ^{1,2,3,4,5} | 0 | 20 | 50 | ps |
| PLL Jitter Peaking | (HBW_BYPASS_LBW = 0) ⁶ | — | 0.4 | 2.0 | dB |
| PLL Jitter Peaking | (HBW_BYPASS_LBW = 1) ⁶ | — | 0.1 | 2.5 | dB |
| PLL Bandwidth | (HBW_BYPASS_LBW = 0) ⁷ | — | 0.7 | 1.4 | MHz |
| PLL Bandwidth | (HBW_BYPASS_LBW = 1) ⁷ | — | 2 | 4 | MHz |

Notes:

1. Measured into fixed 2 pF load cap. Input-to-output skew is measured at the first output edge following the corresponding input.
2. Measured from differential cross-point to differential cross-point.
3. This parameter is deterministic for a given device.
4. Measured with scope averaging on to find mean value.
5. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
6. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
7. Measured at 3 db down or half power point.

Table 6. Phase Jitter

| Parameter | Test Condition | Min | Typ | Max | Unit |
|--------------------------|--|-----|------|------|-------------|
| Phase Jitter PLL Mode | PCIe Gen 1, Common Clock ^{1,2,3} | — | 25 | 86 | ps |
| | PCIe Gen 2 Low Band, Common Clock $F < 1.5 \text{ MHz}$ ^{1,3,4,5} | — | 2.5 | 3.0 | ps (RMS) |
| | PCIe Gen 2 High Band, Common Clock $1.5 \text{ MHz} < F < \text{Nyquist}$ ^{1,3,4,5} | — | 2.5 | 3.1 | ps (RMS) |
| | PCIe Gen 3, Common Clock (PLL BW 2–4 MHz, CDR = 10 MHz) ^{1,3,4,5} | — | 0.5 | 1.0 | ps (RMS) |
| | PCIe Gen 3 Separate Reference No Spread, SRNS (PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz) ^{1,3,4,5} | — | 0.35 | 0.71 | ps (RMS) |
| | Intel® QPI & Intel SMI (4.8 Gbps or 6.4 Gb/s, 100 or 133 MHz, 12 UI) ^{1,6,7} | — | 0.25 | 0.5 | ps (RMS) |
| | Intel QPI & Intel SMI (8 Gb/s, 100 MHz, 12 UI) ^{1,6} | — | 0.15 | 0.3 | ps (RMS) |
| | Intel QPI & Intel SMI (9.6 Gb/s, 100 MHz, 12 UI) ^{1,6} | — | 0.16 | 0.2 | ps (RMS) |

Notes:

1. Post processed evaluation through Intel supplied Matlab* scripts. Defined for a BER of 1E-12. Measured values at a smaller sample size have to be extrapolated to this BER target.
2. $\zeta = 0.54$ implies a jitter peaking of 3 dB.
3. PCIe* Gen 3 filter characteristics are subject to final ratification by PCISIG. Check the PCI-SIG for the latest specification.
4. Measured on 100 MHz PCIe output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
5. Measured on 100 MHz output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
6. Measured on 100 MHz, 133 MHz output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
7. These jitter numbers are defined for a BER of 1E-12. Measured numbers at a smaller sample size have to be extrapolated to this BER target.
8. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.9.
9. Download the Skyworks Solutions PCIe Clock Jitter Tool at <https://www.skyworksinc.com/en/application-pages/pci-express-learning-center>.

Table 6. Phase Jitter (Continued)

| | | | | | |
|--------------------------------------|--|---|------|---|-------------|
| Additive Phase Jitter Bypass Mode | PCIe Gen 1 ^{1,2,3} | — | 10 | — | ps |
| | PCIe Gen 2 Low Band $F < 1.5 \text{ MHz}$ ^{1,3,4,5} | — | 1.0 | — | ps (RMS) |
| | PCIe Gen 2 High Band $1.5 \text{ MHz} < F < \text{Nyquist}$ ^{1,3,4,5} | — | 1.0 | — | ps (RMS) |
| | PCIe Gen 3 (PLL BW 2–4 MHz, CDR = 10 MHz) ^{1,3,4,5} | — | 0.3 | — | ps (RMS) |
| | PCIe Gen 4, Common Clock (PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz) ^{1,4,5,8} | — | 0.3 | — | ps (RMS) |
| | Intel QPI & Intel® SMI (4.8 Gbps or 6.4 Gb/s, 100 or 133 MHz, 12 UI) ^{1,6,7} | — | 0.15 | — | ps (RMS) |
| | Intel QPI & Intel® SMI (8 Gb/s, 100 MHz, 12 UI) ^{1,6} | — | 0.1 | — | ps (RMS) |
| | Intel QPI & Intel® SMI (9.6 Gb/s, 100 MHz, 12 UI) ^{1,6} | — | 0.1 | — | ps (RMS) |

Notes:

1. Post processed evaluation through Intel supplied Matlab* scripts. Defined for a BER of 1E-12. Measured values at a smaller sample size have to be extrapolated to this BER target.
2. $\zeta = 0.54$ implies a jitter peaking of 3 dB.
3. PCIe* Gen 3 filter characteristics are subject to final ratification by PCISIG. Check the PCI-SIG for the latest specification.
4. Measured on 100 MHz PCIe output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
5. Measured on 100 MHz output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
6. Measured on 100 MHz, 133 MHz output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
7. These jitter numbers are defined for a BER of 1E-12. Measured numbers at a smaller sample size have to be extrapolated to this BER target.
8. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.9.
9. Download the Skyworks Solutions PCIe Clock Jitter Tool at <https://www.skyworksinc.com/en/application-pages/pci-express-learning-center>.

Table 7. DIF 0.7 V AC Timing Characteristics (Non-Spread Spectrum Mode)¹

| Parameter | Symbol | CLK 100 MHz, 133 MHz | | | Unit |
|---|--|----------------------|-----|----------|------|
| | | Min | Typ | Max | |
| Clock Stabilization Time ² | T _{STAB} | — | 1.5 | 1.8 | ms |
| Long Term Accuracy ^{3,4,5} | L _{ACC} | — | — | 100 | ppm |
| Absolute Host CLK Period (100 MHz) ^{3,4,6} | T _{ABS} | 9.94900 | — | 10.05100 | ns |
| Absolute Host CLK Period (133 MHz) ^{3,4,6} | T _{ABS} | 7.44925 | — | 7.55075 | ns |
| Slew Rate ^{3,4,7} | Edge_rate | 1.0 | 3.0 | 4.0 | V/ns |
| Rise Time Variation ^{3,8,9} | Δ Trise | — | — | 125 | ps |
| Fall Time Variation ^{3,8,9} | Δ Tfall | — | — | 125 | ps |
| Rise/Fall Matching ^{3,8,10,11} | T _{RISE_MAT} / T _{FALL_MAT} | — | 7 | 20 | % |
| Voltage High (typ 0.7 V) ^{3,8,12} | V _{HIGH} | 660 | 750 | 850 | mV |

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. This is the time from the valid CLK_IN input clocks and the assertion of the PWRGD signal level at 1.8–2.0 V to the time that stable clocks are output from the buffer chip (PLL locked).
3. Test configuration is R_s = 33.2 Ω, 2 pF for 100 Ω transmission line; R_s = 27 Ω, 2 pF for 85 Ω transmission line.
4. Measurement taken from differential waveform.
5. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 99,750,00 Hz, 133,000,000 Hz.
6. The average period over any 1 μs period of time must be greater than the minimum and less than the maximum specified period.
7. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from –150 mV to +150 mV on the differential waveform. Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge. Only valid for Rising clock and Falling CLOCK. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.
8. Measurement taken from single-ended waveform.
9. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.
10. Measured with oscilloscope, averaging on. The difference between the rising edge rate (average) of clock verses the falling edge rate (average) of CLOCK.
11. Rise/Fall matching is derived using the following, 2*(Trise – Tfall) / (Trise + Tfall).
12. VHigh is defined as the statistical average High value as obtained by using the Oscilloscope VHigh Math function.
13. VLow is defined as the statistical average Low value as obtained by using the Oscilloscope VLow Math function.
14. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK.
15. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
16. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
17. Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = 0.250 + 0.5 (Vhavg – 0.700), Vcross(rel) Max = 0.550 – 0.5 (0.700 – Vhavg), (see Figures 3–4 for further clarification).
18. ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK. This is the maximum allowed variance in Vcross for any particular system.
19. Overshoot is defined as the absolute value of the maximum voltage.
20. Undershoot is defined as the absolute value of the minimum voltage.

Table 7. DIF 0.7 V AC Timing Characteristics (Non-Spread Spectrum Mode)¹ (Continued)

| Parameter | Symbol | CLK 100 MHz, 133 MHz | | | Unit |
|--|--------------------|----------------------|-----|-------------------------|------|
| | | Min | Typ | Max | |
| Voltage Low (Typ 0.7 V) ^{3,8,13} | V _{LOW} | –150 | 15 | 150 | mV |
| Maximum Voltage ⁸ | V _{MAX} | — | 850 | 1150 | mV |
| Minimum Voltage | V _{MIN} | –300 | — | — | mV |
| Absolute Crossing Point Voltages ^{3,8,14,15,16} | V _{OXABS} | 300 | 450 | 550 | mV |
| Total Variation of Vcross Over All Edges ^{3,8,18} | Total Δ Vox | — | 14 | 140 | mV |
| Duty Cycle ^{3,4} | DC | 45 | — | 55 | % |
| Maximum Voltage (Overshoot) ^{3,8,19} | V _{ovs} | — | — | V _{High} + 0.3 | V |
| Maximum Voltage (Undershoot) ^{3,8,20} | V _{uds} | — | — | V _{Low} – 0.3 | V |
| Ringback Voltage ^{3,8} | V _{rb} | 0.2 | — | N/A | V |

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. This is the time from the valid CLK_IN input clocks and the assertion of the PWRGD signal level at 1.8–2.0 V to the time that stable clocks are output from the buffer chip (PLL locked).
3. Test configuration is R_s = 33.2 Ω , 2 pF for 100 Ω transmission line; R_s = 27 Ω , 2 pF for 85 Ω transmission line.
4. Measurement taken from differential waveform.
5. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 99,750,00 Hz, 133,000,000 Hz.
6. The average period over any 1 μ s period of time must be greater than the minimum and less than the maximum specified period.
7. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from –150 mV to +150 mV on the differential waveform. Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge. Only valid for Rising clock and Falling CLOCK. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.
8. Measurement taken from single-ended waveform.
9. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.
10. Measured with oscilloscope, averaging on. The difference between the rising edge rate (average) of clock verses the falling edge rate (average) of CLOCK.
11. Rise/Fall matching is derived using the following, $2 \cdot (\text{Trise} - \text{Tfall}) / (\text{Trise} + \text{Tfall})$.
12. V_{High} is defined as the statistical average High value as obtained by using the Oscilloscope V_{High} Math function.
13. V_{Low} is defined as the statistical average Low value as obtained by using the Oscilloscope V_{Low} Math function.
14. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK.
15. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
16. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
17. V_{cross(rel)} Min and Max are derived using the following, V_{cross(rel)} Min = 0.250 + 0.5 (V_{havg} – 0.700), V_{cross(rel)} Max = 0.550 – 0.5 (0.700 – V_{havg}), (see Figures 3–4 for further clarification).
18. Δ V_{cross} is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK. This is the maximum allowed variance in V_{cross} for any particular system.
19. Overshoot is defined as the absolute value of the maximum voltage.
20. Undershoot is defined as the absolute value of the minimum voltage.

Table 8. Clock Periods Differential Clock Outputs with SSC Disabled

| SSC OFF Center Freq, MHz | Measurement Window | | | | | | | Unit |
|--------------------------------|---------------------------------|----------------------------------|---------------------------------|----------------------------|---------------------------------|----------------------------------|---------------------------------|------|
| | 1 Clock | 1 μ s | 0.1 s | 0.1 s | 0.1 s | 1 μ s | 1 Clock | |
| | –C-C Jitter AbsPer Min | –SSC Short Term AVG Min | –ppm Long Term AVG Min | 0 ppm Period Nominal | +ppm Long Term AVG Max | +SSC Short Term AVG Max | +C-C Jitter AbsPer Max | |
| 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns |
| 133.33 | 7.44925 | | 7.49925 | 7.50000 | 7.50075 | | 7.55075 | ns |

Table 9. Clock Periods Differential Clock Outputs with SSC Enabled

| SSC ON Center Freq, MHz | Measurement Window | | | | | | | Unit |
|-------------------------------|---------------------------------|----------------------------------|---------------------------------|----------------------------|---------------------------------|----------------------------------|---------------------------------|------|
| | 1 Clock | 1 μ s | 0.1 s | 0.1 s | 0.1 s | 1 μ s | 1 Clock | |
| | –C-C Jitter AbsPer Min | –SSC Short Term AVG Min | –ppm Long Term AVG Min | 0 ppm Period Nominal | +ppm Long Term AVG Max | +SSC Short Term AVG Max | +C-C Jitter AbsPer Max | |
| 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns |
| 133.33 | 7.44930 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.58830 | ns |

Table 10. Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|---|----------------|------|-----|------|
| 3.3 V Core Supply Voltage ¹ | VDD/VDD_A | — | 4.6 | V |
| 3.3 V I/O Supply Voltage ¹ | VDD_IO | — | 4.6 | V |
| 3.3 V Input High Voltage ^{1,2} | VIH | — | 4.6 | V |
| 3.3 V Input Low Voltage ¹ | VIL | –0.5 | — | V |
| Storage Temperature ¹ | t _s | –65 | 150 | °C |
| Input ESD protection ³ | ESD | 2000 | — | V |

Notes:

1. Consult manufacturer regarding extended operation in excess of normal dc operating parameters.
2. Maximum VIH is not to exceed maximum V_{DD}.
3. Human body model.

2. Functional Description

2.1. CLK_IN, $\overline{\text{CLK_IN}}$

The differential input clock is expected to be sourced from a clock synthesizer or PCH.

2.2. $\overline{100M_133M}$ —Frequency Selection

The Si53119 is optimized for lowest phase jitter performance at operating frequencies of 100 and 133 MHz. $\overline{100M_133M}$ is a hardware input pin, which programs the appropriate output frequency of the differential outputs. Note that the CLK_IN frequency must be equal to the CLK_OUT frequency; meaning Si53119 is operated in 1:1 mode only. Frequency selection can be enabled by the $\overline{100M_133M}$ hardware pin. An external pull-up or pull-down resistor is attached to this pin to select the input/output frequency. The functionality is summarized in Table 11.

Table 11. Frequency Program Table

| $\overline{100M_133M}$ | Optimized Frequency (DIF_IN = DIF_x) |
|-------------------------|--------------------------------------|
| 0 | 133.33 MHz |
| 1 | 100.00 MHz |

Note: All differential outputs transition from 100 to 133 MHz or from 133 to 100 MHz in a glitch free manner.

2.3. SA_0, SA_1—Address Selection

SA_0 and SA_1 are tri-level hardware pins, which program the appropriate address for the Si53119. The two tri-level input pins that can configure the device to nine different addresses.

Table 12. SMBUS Address Table

| SA_1 | SA_0 | SMBUS Address |
|------|------|---------------|
| L | L | D8 |
| L | M | DA |
| L | H | DE |
| M | L | C2 |
| M | M | C4 |
| M | H | C6 |
| H | L | CA |
| H | M | CC |
| H | H | CE |

2.4. CKPWRGD/ $\overline{\text{PWRDN}}$

CKPWRGD is asserted high and deasserted low. Deassertion of PWRGD (pulling the signal low) is equivalent to indicating a power down condition. CKPWRGD (assertion) is used by the Si53119 to sample initial configurations, such as frequency select condition and SA selections. After CKPWRGD has been asserted high for the first time, the pin becomes a $\overline{\text{PWRDN}}$ (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power-saving mode. $\overline{\text{PWRDN}}$ is a completely asynchronous active low input. When entering power-saving mode, $\overline{\text{PWRDN}}$ should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When $\overline{\text{PWRDN}}$ is asserted low, all clocks will be disabled prior to turning off the VCO. When $\overline{\text{PWRDN}}$ is deasserted high, all clocks will start and stop without any abnormal behavior and will meet all ac and dc parameters.

Note: The assertion and deassertion of $\overline{\text{PWRDN}}$ is absolutely asynchronous.

Warning: Disabling of the CLK_IN input clock prior to assertion of $\overline{\text{PWRDN}}$ is an undefined mode and not recommended. Operation in this mode may result in glitches, excessive frequency shifting, etc.

Table 13. CKPWRGD/ $\overline{\text{PWRDN}}$ Functionality

| CKPWRGD/ $\overline{\text{PWRDN}}$ | DIF_IN/ DINF_IN# | SMBus EN bit | DIF-x/ DIF_x# | FBOUT_NC/ FBOUT_NC# | PLL State |
|------------------------------------|---------------------|-----------------|------------------|------------------------|-----------|
| 0 | X | X | Low/Low | Low/Low | OFF |
| 1 | Running | 0 | Low/Low | Running | ON |
| | | 1 | Running | Running | ON |

2.4.1. $\overline{\text{PWRDN}}$ Assertion

When $\overline{\text{PWRDN}}$ is sampled low by two consecutive rising edges of $\overline{\text{DIF}}$, all differential outputs must be held LOW/LOW on the next DIF high-to-low transition.

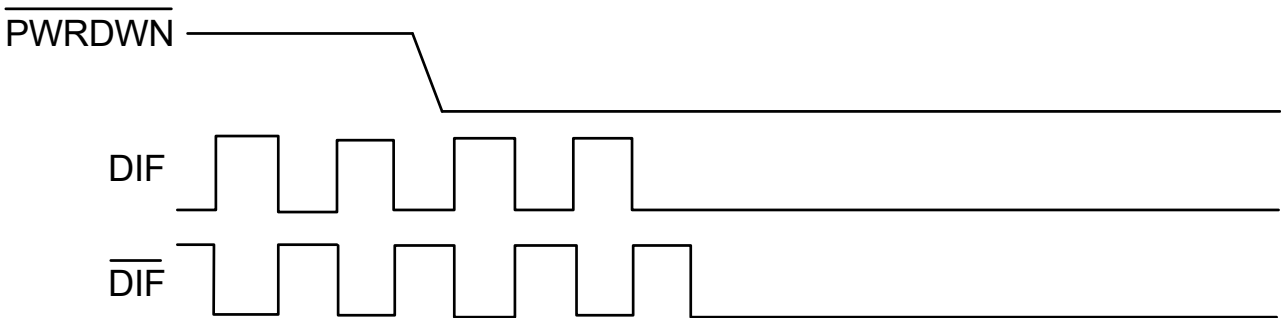


Figure 1. $\overline{\text{PWRDN}}$ Assertion

2.4.2. CKPWRGD Assertion

The powerup latency is to be less than 1.8 ms. This is the time from a valid CLK_IN input clock and the assertion of the PWRGD signal to the time that stable clocks are output from the device (PLL locked). All differential outputs stopped in a LOW/LOW condition resulting from power down must be driven high in less than 300 μ s of $\overline{\text{PWRDN}}$ deassertion to a voltage greater than 200 mV.

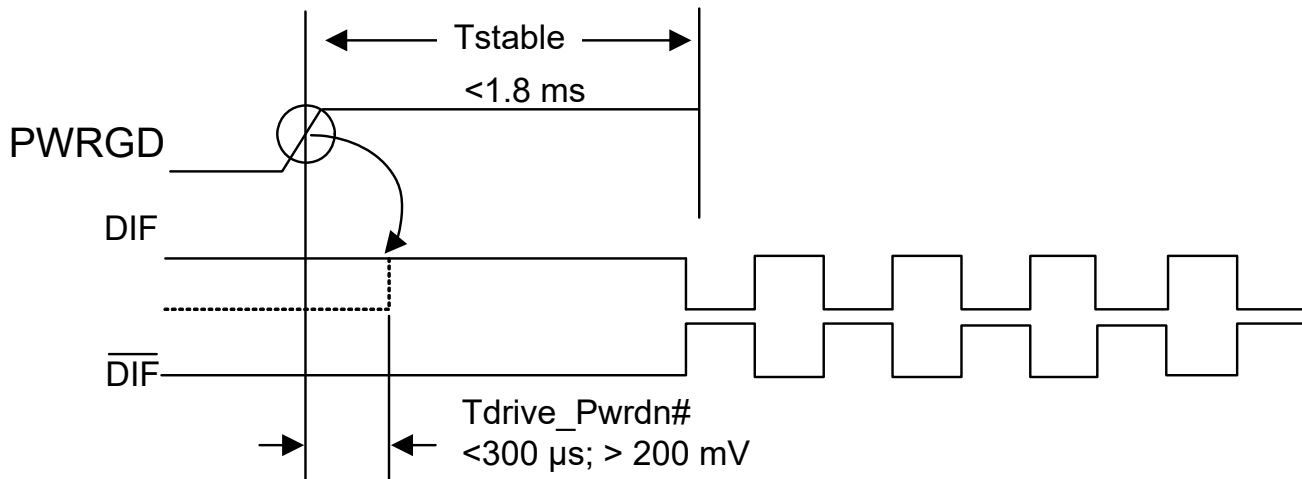


Figure 2. PWRDG Assertion (Pwrdown—Deassertion)

2.5. HBW_BYPASS_LBW

The $\overline{\text{HBW_BYPASS_LBW}}$ pin is a tri-level function input pin (refer to Table 1 for V_{IL_Tri} , V_{IM_Tri} , and V_{IH_Tri} signal levels). It is used to select between PLL high-bandwidth, PLL bypass mode, or PLL low-bandwidth mode. In PLL bypass mode, the input clock is passed directly to the output stage, which may result in up to 50 ps of additive cycle-to-cycle jitter (50 ps + input jitter) on the differential outputs. In PLL mode, the input clock is passed through a PLL to reduce high-frequency jitter. The PLL HBW, BYPASS, and PLL LBW modes may be selected by asserting the $\overline{\text{HBW_BYPASS_LBW}}$ input pin to the appropriate level described in Table 14.

Table 14. PLL Bandwidth and Readback Table

| $\overline{\text{HBW_BYPASS_LBW}}$ Pin | Mode | Byte 0, Bit 7 | Byte 0, Bit 6 |
|--|--------|---------------|---------------|
| L | LBW | 0 | 0 |
| M | BYPASS | 0 | 1 |
| H | HBW | 1 | 1 |

The Si53119 has the ability to override the latch value of the PLL operating mode from hardware strap pin 5 via the use of Byte 18 and bits 1 and 0. Byte 18 bit 2 must be set to 1 to allow the user to change Bits 1 and 0, affecting the PLL. Byte0, Bits 7 and 6 will always read back the original latched value from hardware strap pin5. A warm reset of the external system will have to be accomplished if the user changes these bits.

2.6. Miscellaneous Requirements

Data Transfer Rate: 100 kbps (standard mode) is the base functionality required. Fast mode (400 kbps) functionality is optional.

Logic Levels: SMBus logic levels are based on a percentage of V_{DD} for the controller and other devices on the bus. Assume all devices are based on a 3.3 V supply.

Clock Stretching: The clock buffer must not hold/stretch the SCL or SDA lines low for more than 10 ms. Clock stretching is discouraged and should only be used as a last resort. Stretching the clock/data lines for longer than this time puts the device in an error/time-out mode and may not be supported in all platforms. It is assumed that all data transfers can be completed as specified without the use of clock/data stretching.

General Call: It is assumed that the clock buffer will not have to respond to the “general call.”

Electrical Characteristics: All electrical characteristics must meet the standard mode specifications found in Section 3 of the SMBus 2.0 specification.

Pull-Up Resistors: Any internal resistor pull-ups on the SDATA and SCLK inputs must be stated in the individual datasheet. The use of internal pull-ups on these pins of below 100 K is discouraged. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5–6 k Ω range. Assume one SMBus device per DIMM (serial presence detect), one SMBus controller, one clock buffer, one clock driver plus one/two more SMBus devices on the platform for capacitive loading purposes.

Input Glitch Filters: Only fast mode SMBus devices require input glitch filters to suppress bus noise. The clock buffer is specified as a standard mode device and is not required to support this feature. However, it is considered a good design practice to include the filters.

PWRDN: If a clock buffer is placed in $\overline{\text{PWRDN}}$ mode, the SDATA and SCLK inputs must be Tri-stated and the device must retain all programming information. I_{DD} current due to the SMBus circuitry must be characterized and in the data sheet.

3. Test and Measurement Setup

3.1. Input Edge

Input edge rate is based on single-ended measurement. This is the minimum input edge rate at which the Si53119 is guaranteed to meet all performance specifications.

Table 15. Input Edge Rate

| Frequency | Min | Max | Unit |
|-----------|------|-----|------|
| 100 MHz | 0.35 | N/A | V/ns |
| 133 MHz | 0.35 | N/A | V/ns |

3.1.1. Measurement Points for Differential

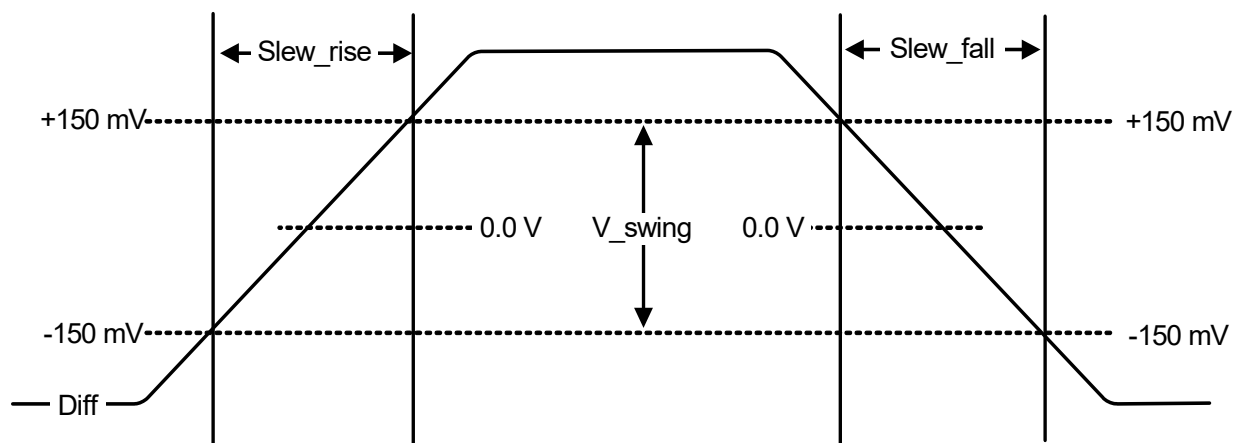


Figure 3. Measurement Points for Rise Time and Fall Time

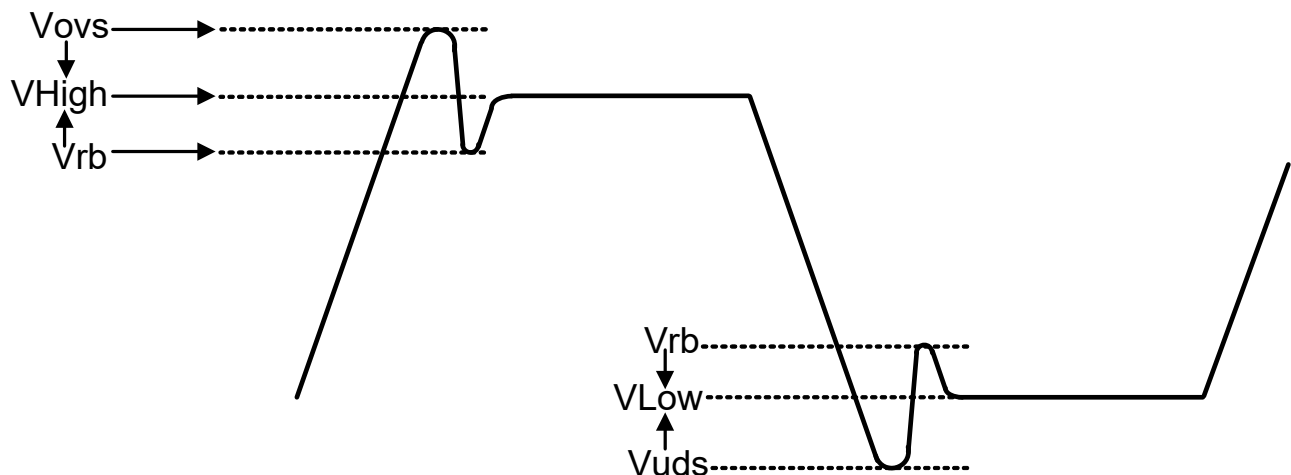


Figure 4. Single-Ended Measurement Points for V_{ovs} , V_{uds} , V_{rb}

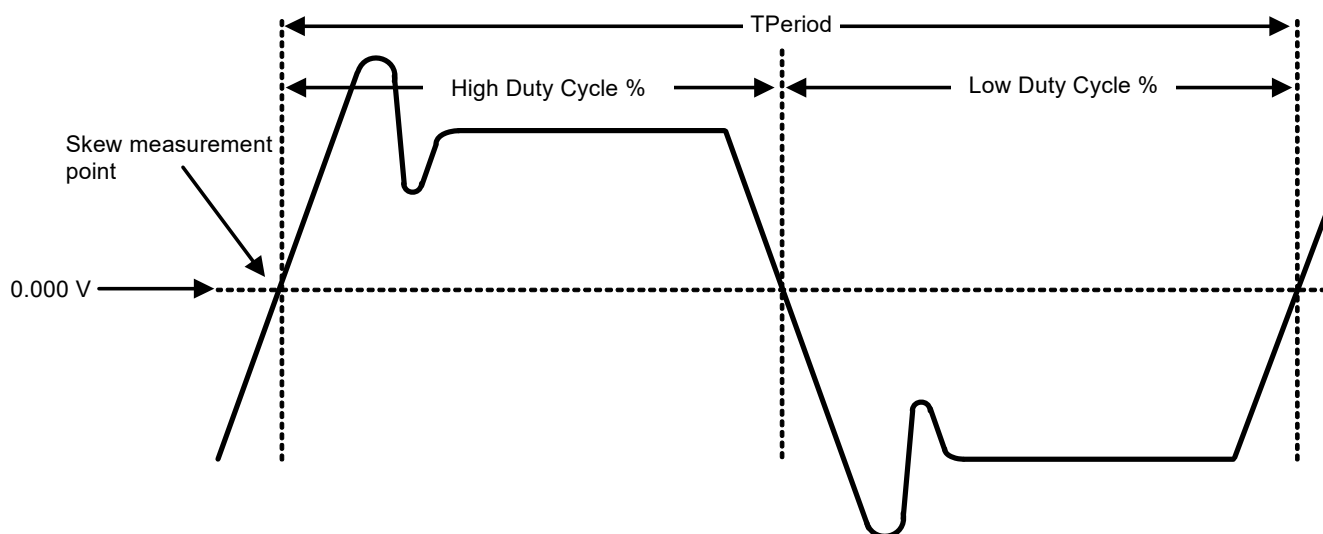


Figure 5. Differential (CLOCK-CLOCK) Measurement Points (T_{period} , Duty Cycle, Jitter)

3.2. Termination of Differential Outputs

All differential outputs are to be tested into a 100 Ω or 85 Ω differential impedance transmission line. Source terminated clocks have some inherent limitations as to the maximum trace length and frequencies that can be supported. For CPU outputs, a maximum trace length of 10" and a maximum of 200 MHz are assumed. For SRC clocks, a maximum trace length of 16" and maximum frequency of 100 MHz is assumed. For frequencies beyond 200 MHz, trace lengths must be restricted to avoid signal integrity problems.

Table 16. Differential Output Termination

| Clock | Board Trace Impedance | R_s | R_p | Unit |
|---------------------------------------|-----------------------|-------------|-------|----------|
| DIFF Clocks—50 Ω configuration | 100 | 33 \pm 5% | N/A | Ω |
| DIFF Clocks—43 Ω configuration | 85 | 27 \pm 5% | N/A | Ω |

3.2.1. Termination of Differential NMOS Push-Pull Type Outputs

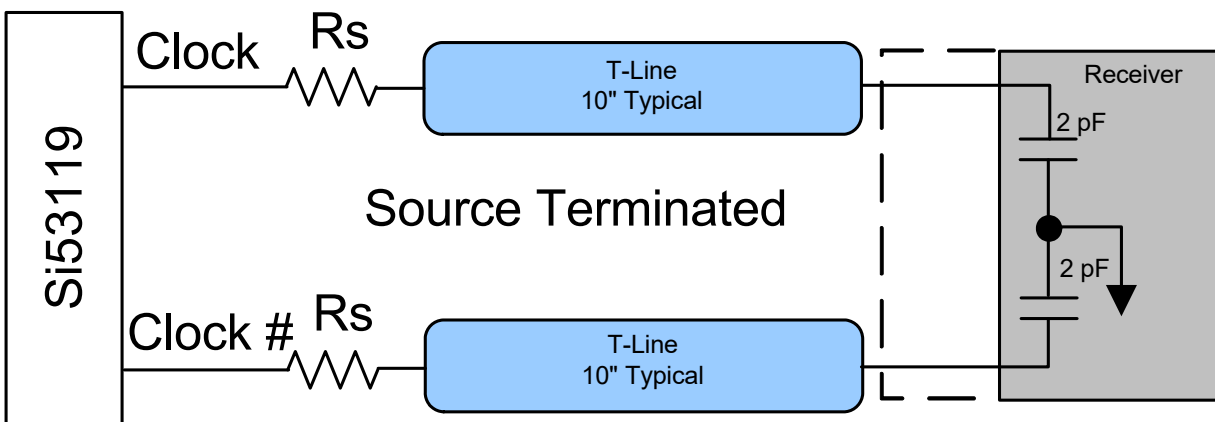


Figure 6. 0.7 V Configuration Test Load Board Termination for NMOS Push-Pull

4. Control Registers

4.1. Byte Read/Write

Reading or writing a register in an SMBus slave device in byte mode always involves specifying the register number.

4.1.1. Byte Read

The standard byte read is as shown in Figure 7. It is an extension of the byte write. The write start condition is repeated; then, the slave device starts sending data, and the master acknowledges it until the last byte is sent. The master terminates the transfer with a NAK, then a stop condition. For byte operation, the 2 x 7th bit of the command byte must be set. For block operations, the 2 x 7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count.

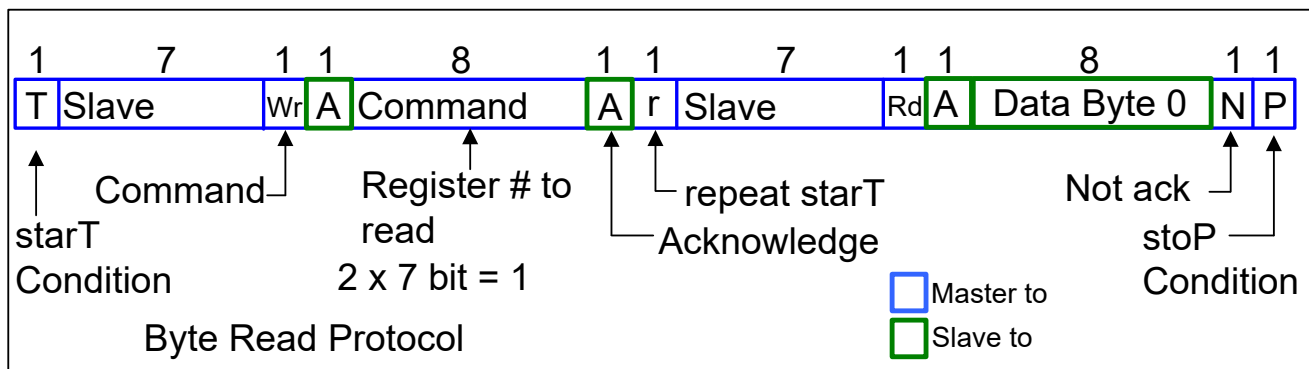


Figure 7. Byte Read Protocol

4.1.2. Byte Write

Figure 8 illustrates a simple, typical byte write. For byte operation, the 2 x 7th bit of the command byte must be set. For block operations, the 2 x 7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count. The count can be between 1 and 32. It is not allowed to be zero or to exceed 32.

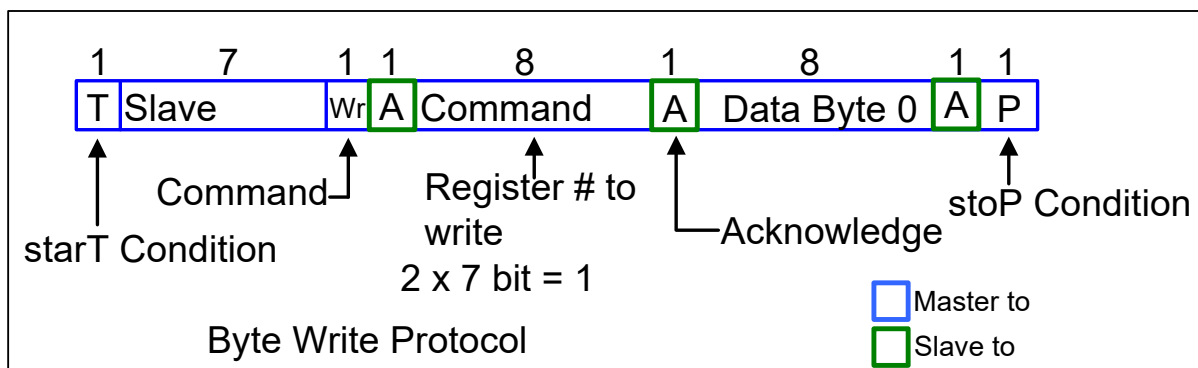


Figure 8. Byte Write Protocol

4.2. Block Read/Write

4.2.1. Block Read

After the slave address is sent with the R/W condition bit set, the command byte is sent with the MSB = 0. The slave acknowledges the register index in the command byte. The master sends a repeat start function. After the slave acknowledges this, the slave sends the number of bytes it wants to transfer (>0 and <33). The master acknowledges each byte except the last and sends a stop function.

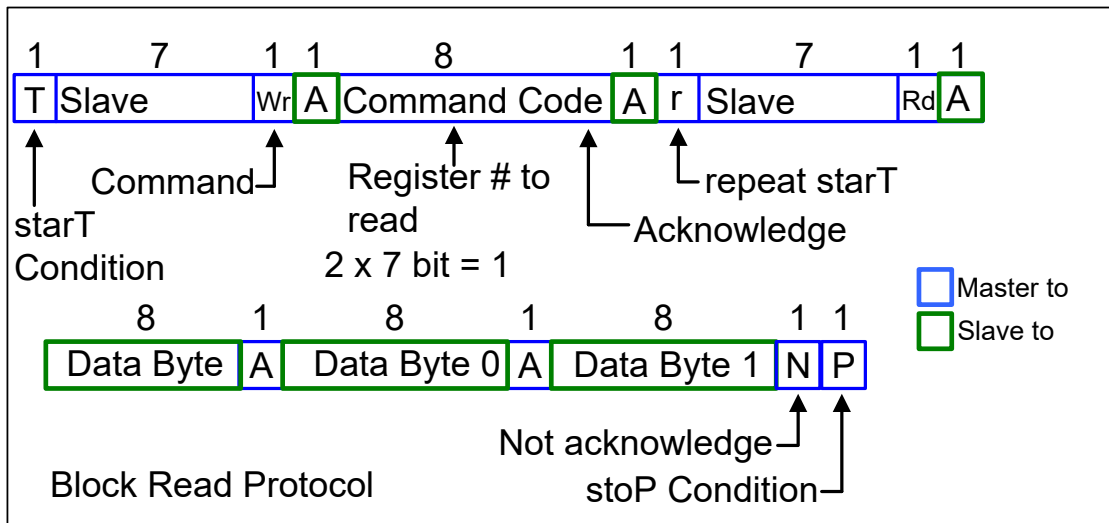


Figure 9. Block Read Protocol

4.2.2. Block Write

After the slave address is sent with the R/W condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate the register at which to start the transfer. If the command byte is 00h, the slave device will be compatible with existing block mode slave devices. The next byte of a write must be the count of bytes that the master will transfer to the slave device. The byte count must be greater than zero and less than 33. Following this byte are the data bytes to be transferred to the slave device. The slave device always acknowledges each byte received. The transfer is terminated after the slave sends the ACK and the master sends a stop function.

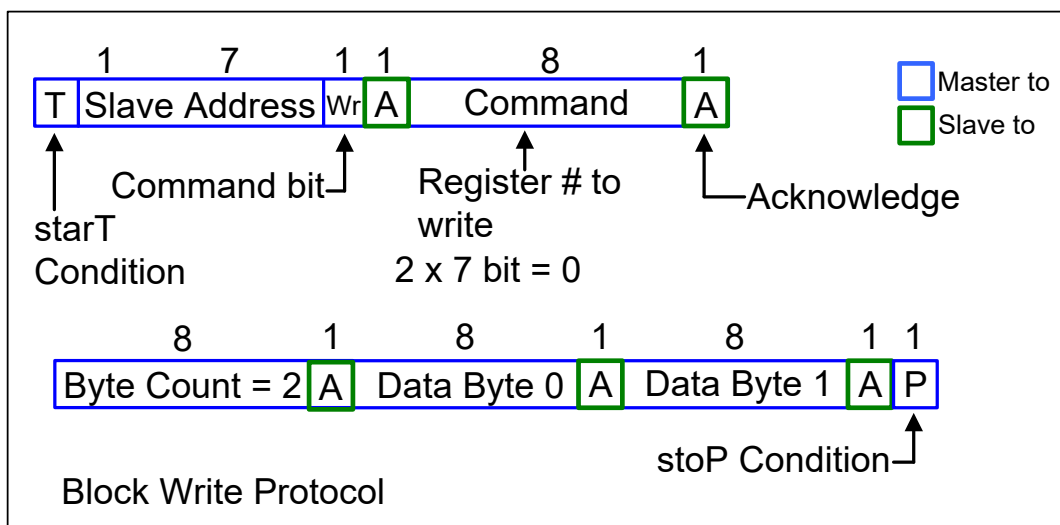


Figure 10. Block Write Protocol

4.3. Control Registers

Table 17. Byte 0: Frequency Select, Output Enable, PLL Mode Control Register

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|--------------------------------|---------------------------------------|------------|------|---------------------|--------------------|
| 0 | 100M_133M# Frequency Select | 133 MHz | 100 MHz | R | Latched at power up | DIF[11:0] |
| 1 | Reserved | | | | 0 | |
| 2 | Reserved | | | | 0 | |
| 3 | Output Enable DIF 16 | Low/Low | Enable | RW | 1 | DIF_16 |
| 4 | Output Enable DIF 17 | Low/Low | Enable | RW | 1 | DIF_17 |
| 5 | Output Enable DIF 18 | Low/Low | Enable | RW | 1 | DIF_18 |
| 6 | PLL Mode 0 | See PLL Operating Mode Readback Table | | R | Latched at power up | |
| 7 | PLL Mode 1 | See PLL Operating Mode Readback Table | | R | Latched at power up | |

Table 18. Byte 1: Output Enable Control Register

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|---------------------|------------|------------|------|---------|--------------------|
| 0 | Output Enable DIF 0 | Low/Low | Enabled | RW | 1 | DIF[0] |
| 1 | Output Enable DIF 1 | Low/Low | Enabled | RW | 1 | DIF[1] |
| 2 | Output Enable DIF 2 | Low/Low | Enabled | RW | 1 | DIF[2] |
| 3 | Output Enable DIF 3 | Low/Low | Enabled | RW | 1 | DIF[3] |
| 4 | Output Enable DIF 4 | Low/Low | Enabled | RW | 1 | DIF[4] |
| 5 | Output Enable DIF 5 | Low/Low | Enabled | RW | 1 | DIF[5] |
| 6 | Output Enable DIF 6 | Low/Low | Enabled | RW | 1 | DIF[6] |
| 7 | Output Enable DIF 7 | Low/Low | Enabled | RW | 1 | DIF[7] |

Table 19. Byte 2: Output Enable Control Register

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|----------------------|------------|------------|------|---------|--------------------|
| 0 | Output Enable DIF 8 | Low/Low | Enabled | RW | 1 | DIF[8] |
| 1 | Output Enable DIF 9 | Low/Low | Enabled | RW | 1 | DIF[9] |
| 2 | Output Enable DIF 10 | Low/Low | Enabled | RW | 1 | DIF[10] |
| 3 | Output Enable DIF 11 | Low/Low | Enabled | RW | 1 | DIF[11] |
| 4 | Output Enable DIF 12 | Low/Low | Enabled | RW | 1 | DIF[112] |
| 5 | Output Enable DIF 13 | Low/Low | Enabled | RW | 1 | DIF[14] |
| 6 | Output Enable DIF 14 | Low/Low | Enabled | RW | 1 | DIF[15] |
| 7 | Output Enable DIF 15 | Low/Low | Enabled | RW | 1 | DIF[16] |

Table 20. Byte 3: Reserved Control Register

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|-------------|------------|------------|------|---------|--------------------|
| 0 | Reserved | | | | 0 | |
| 1 | Reserved | | | | 0 | |
| 2 | Reserved | | | | 0 | |
| 3 | Reserved | | | | 0 | |
| 4 | Reserved | | | | 0 | |
| 5 | Reserved | | | | 0 | |
| 6 | Reserved | | | | 0 | |
| 7 | Reserved | | | | 0 | |

Table 21. Byte 4: Reserved Control Register

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|-------------|------------|------------|------|---------|--------------------|
| 0 | Reserved | | | | 0 | |
| 1 | Reserved | | | | 0 | |
| 2 | Reserved | | | | 0 | |
| 3 | Reserved | | | | 0 | |
| 4 | Reserved | | | | 0 | |
| 5 | Reserved | | | | 0 | |
| 6 | Reserved | | | | 0 | |
| 7 | Reserved | | | | 0 | |

Table 22. Byte 5: Vendor/Revision Identification Control Register

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|---------------------|------------|------------|------|-----------------|--------------------|
| 0 | Vendor ID Bit 0 | | | R | Vendor Specific | 0 |
| 1 | Vendor ID Bit 1 | | | R | Vendor Specific | 0 |
| 2 | Vendor ID Bit 2 | | | R | Vendor Specific | 0 |
| 3 | Vendor ID Bit 3 | | | R | Vendor Specific | 1 |
| 4 | Revision Code Bit 0 | | | R | Vendor Specific | 0 |
| 5 | Revision Code Bit 1 | | | R | Vendor Specific | 0 |
| 6 | Revision Code Bit 2 | | | R | Vendor Specific | 0 |
| 7 | Revision Code Bit 3 | | | R | Vendor Specific | 0 |

Table 23. Byte 6: Device ID Control Register

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|-------------------|------------|------------|------|---------|-----------------------|
| 0 | Device ID 0 | | | R | 0 | |
| 1 | Device ID 1 | | | R | 1 | |
| 2 | Device ID 2 | | | R | 1 | |
| 3 | Device ID 3 | | | R | 1 | |
| 4 | Device ID 4 | | | R | 0 | |
| 5 | Device ID 5 | | | R | 1 | |
| 6 | Device ID 6 | | | R | 1 | |
| 7 | Device ID 7 (MSB) | | | R | 1 | |

Table 24. Byte 7: Byte Count Register

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Output(s) Affected |
|-----|--|------------|------------|------|---------|--------------------|
| 0 | BC0 - Writing to this register configures how many bytes will be read back | | | RW | 0 | |
| 1 | BC1 -Writing to this register configures how many bytes will be read back | | | RW | 0 | |
| 2 | BC2 -Writing to this register configures how many bytes will be read back | | | RW | 0 | |
| 3 | BC3 -Writing to this register configures how many bytes will be read back | | | RW | 1 | |
| 4 | BC4 -Writing to this register configures how many bytes will be read back | | | RW | 0 | |
| 5 | Reserved | | | | 0 | |
| 6 | Reserved | | | | 0 | |
| 7 | Reserved | | | | 0 | |

Table 25. Byte 18: PLL Mode Control Register

| Bit | Description | If Bit = 0 | If Bit = 1 | Type | Default | Outputs Affected |
|-----|-------------|--|-------------------------|------|---------|------------------|
| 0 | PLL_MODE0 | If Byte0[3] = 1 allows the user to override the latch from pin5 via use of Byte0[2:1] 00 = Low Bandwidth Mode 01 = Bypass Mode 11 = High Bandwidth Mode | | R/W | 0 | |
| 1 | PLL_MODE1 | | | R/W | 0 | |
| 2 | PLL_SW_EN | HW Select | I ² C Select | R/W | 0 | |
| 3 | Reserved | | | | 0 | |
| 4 | Reserved | | | | 0 | |
| 5 | Reserved | | | | 0 | |
| 6 | Reserved | | | | 0 | |
| 7 | Reserved | | | | 0 | |

5. Pin Descriptions: 72-Pin QFN

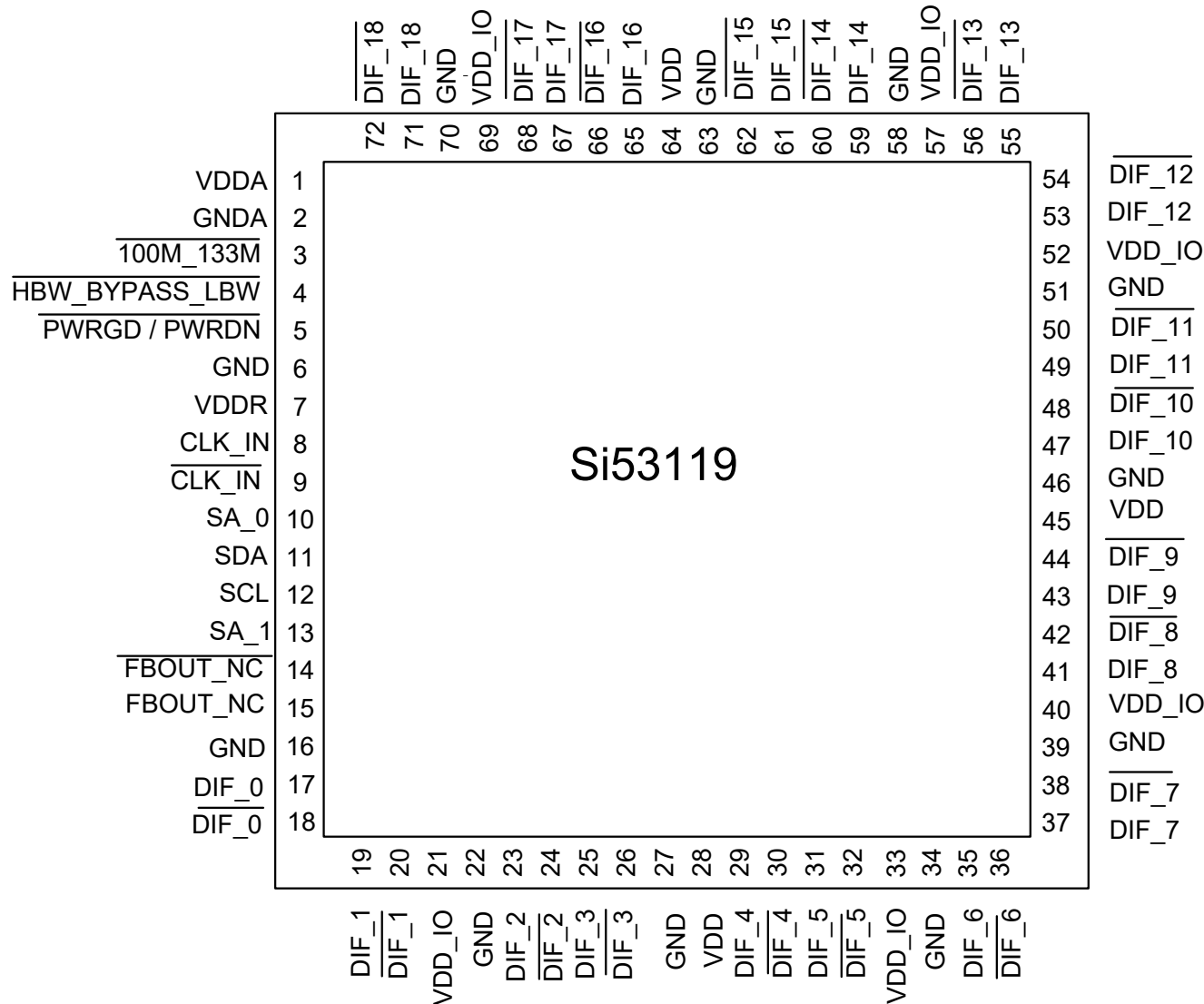


Table 26. Si53119 72-Pin QFN Descriptions

| Pin # | Name | Type | Description |
|-------|-------------------------------|--------|--|
| 1 | VDDA | 3.3 V | 3.3 V power supply for PLL. |
| 2 | GND | GND | Ground for PLL. |
| 3 | $\overline{100M_133M}$ | I, SE | 3.3 V tolerant inputs for input/output frequency selection. An external pull-up or pull-down resistor is attached to this pin to select the input/output frequency. High = 100 MHz output Low = 133 MHz output |
| 4 | $\overline{HBW_BYPASS_LBW}$ | I, SE | Tri-Level input for selecting the PLL bandwidth or bypass mode. High = High BW mode Med = Bypass mode Low = Low BW mode |
| 5 | $\overline{PWRGD/PWRDN}$ | I | 3.3 V LVTTTL input to power up or power down the device. |
| 6 | GND | GND | Ground for outputs. |
| 7 | VDDR | VDD | 3.3 V power supply for differential input receiver. This VDDR should be treated as an analog power rail and filtered appropriately. |
| 8 | CLK_IN | I, DIF | 0.7 V Differential input. |
| 9 | $\overline{CLK_IN}$ | I, DIF | 0.7 V Differential input. |
| 10 | SA_0 | I, PU | 3.3 V LVTTTL input selecting the address. Tri-level input. |
| 11 | SDA | I/O | Open collector SMBus data. |
| 12 | SCL | I/O | SMBus slave clock input. |
| 13 | SA_1 | I, PU | 3.3 V LVTTTL input selecting the address. Tri-level input. |
| 14 | $\overline{FBOUT / NC}$ | I/O | Complementary differential feedback output. Do not connect this pin to anything. |
| 15 | FBOUT / NC | I/O | True differential feedback output. Do not connect this pin to anything. |
| 16 | GND | GND | Ground for outputs. |
| 17 | DIF_0 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 18 | $\overline{DIF_0}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 19 | DIF_1 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 20 | $\overline{DIF_1}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 21 | VDD_IO | VDD | Power supply for differential outputs. |
| 22 | GND | GND | Ground for outputs. |
| 23 | DIF_2 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 24 | $\overline{DIF_2}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |

Table 26. Si53119 72-Pin QFN Descriptions (Continued)

| Pin # | Name | Type | Description |
|-------|------------------------------|--------|---|
| 25 | DIF_3 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 26 | $\overline{\text{DIF}}_3$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 27 | GND | GND | Ground for outputs. |
| 28 | VDD | 3.3 V | 3.3 V power supply for outputs. |
| 29 | DIF_4 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 30 | $\overline{\text{DIF}}_4$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 31 | DIF_5 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 32 | $\overline{\text{DIF}}_5$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 33 | VDD_IO | VDD | Power supply for differential outputs. |
| 34 | GND | GND | Ground for outputs. |
| 35 | DIF_6 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 36 | $\overline{\text{DIF}}_6$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 37 | DIF_7 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 38 | $\overline{\text{DIF}}_7$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 39 | GND | GND | Ground for outputs. |
| 40 | VDD_IO | VDD | Power supply for differential outputs. |
| 41 | DIF_8 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 42 | $\overline{\text{DIF}}_8$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 43 | DIF_9 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 44 | $\overline{\text{DIF}}_9$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 45 | VDD | 3.3 V | 3.3 V power supply for outputs. |
| 46 | GND | GND | Ground for outputs. |
| 47 | DIF_10 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 48 | $\overline{\text{DIF}}_{10}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 49 | DIF_11 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 50 | $\overline{\text{DIF}}_{11}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 51 | GND | GND | Ground for outputs. |
| 52 | VDD_IO | VDD | Power supply for differential outputs. |
| 53 | DIF_12 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |

Table 26. Si53119 72-Pin QFN Descriptions (Continued)

| Pin # | Name | Type | Description |
|-------|------------------------------|--------|---|
| 54 | $\overline{\text{DIF}}_{12}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 55 | DIF_13 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 56 | $\overline{\text{DIF}}_{13}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 57 | VDD_IO | VDD | Power supply for differential outputs. |
| 58 | GND | GND | Ground for outputs. |
| 59 | DIF_14 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 60 | $\overline{\text{DIF}}_{14}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 61 | DIF_15 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 62 | $\overline{\text{DIF}}_{15}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 63 | GND | GND | Ground for outputs. |
| 64 | VDD | 3.3 V | 3.3 V power supply for outputs. |
| 65 | DIF_16 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 66 | $\overline{\text{DIF}}_{16}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 67 | DIF_17 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 68 | $\overline{\text{DIF}}_{17}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 69 | VDD_IO | VDD | Power supply for differential outputs. |
| 70 | GND | GND | Ground for outputs. |
| 71 | DIF_18 | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 72 | $\overline{\text{DIF}}_{18}$ | O, DIF | 0.7 V Differential clock outputs. Default is 1:1. |
| 73 | GND | GND | Ground for outputs. |

7. Ordering Guide

| Part Number | Package Type | Temperature |
|------------------|--------------------------|------------------------|
| Lead-free | | |
| Si53119-A01AGM | 72-pin QFN | Extended, –40 to 85 °C |
| Si53119-A01AGMR | 72-pin QFN—Tape and Reel | Extended, –40 to 85 °C |

8. Package Outline

Figure 12 illustrates the package details for the Si53119. Table 27 lists the values for the dimensions shown in the illustration.

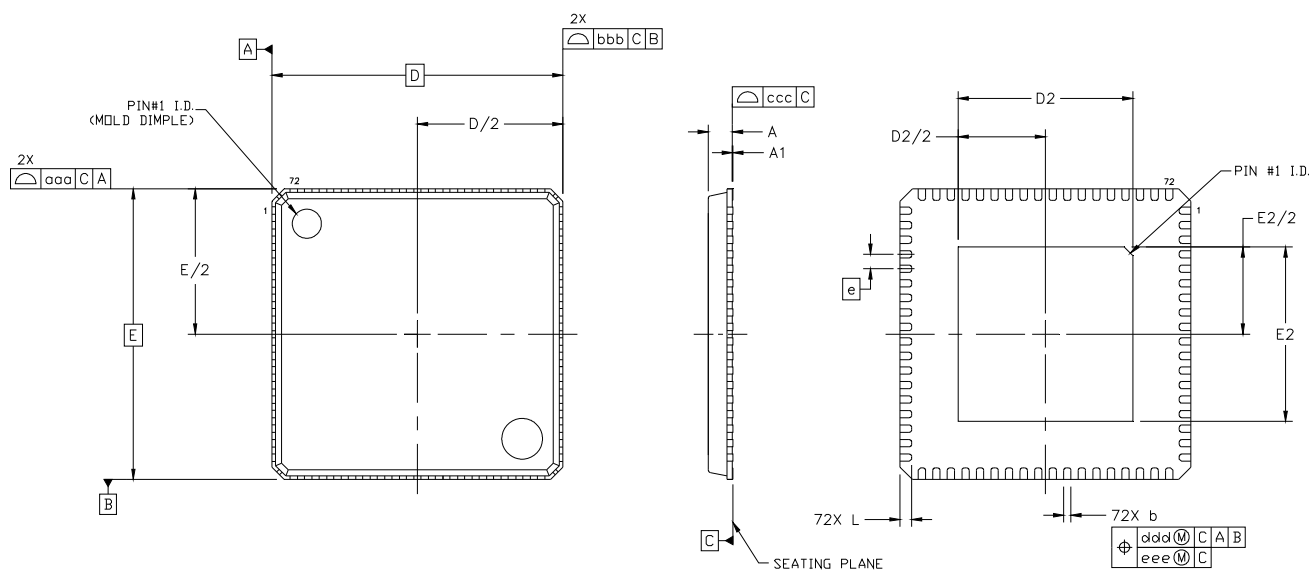


Figure 12. 72-Pin Quad Flat No Lead (QFN) Package

Table 27. Package Dimensions

| Dimension | Min | Nom | Max | Dimension | Min | Nom | Max |
|-----------|------------|------|------|-----------|------|------|------|
| A | 0.80 | 0.85 | 0.90 | E2 | 5.90 | 6.00 | 6.10 |
| A1 | 0.00 | 0.02 | 0.05 | L | 0.30 | 0.40 | 0.50 |
| b | 0.18 | 0.25 | 0.30 | aaa | 0.10 | | |
| D | 10.00 BSC. | | | bbb | 0.10 | | |
| D2 | 5.90 | 6.00 | 6.10 | ccc | 0.08 | | |
| e | 0.50 BSC. | | | ddd | 0.10 | | |
| E | 10.00 BSC. | | | eee | 0.05 | | |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Land Pattern: 72-pin QFN

Figure 13 shows the recommended land pattern details for the Si53119 in a 72-pin QFN package. Table 28 lists the values for the dimensions shown in the illustration.

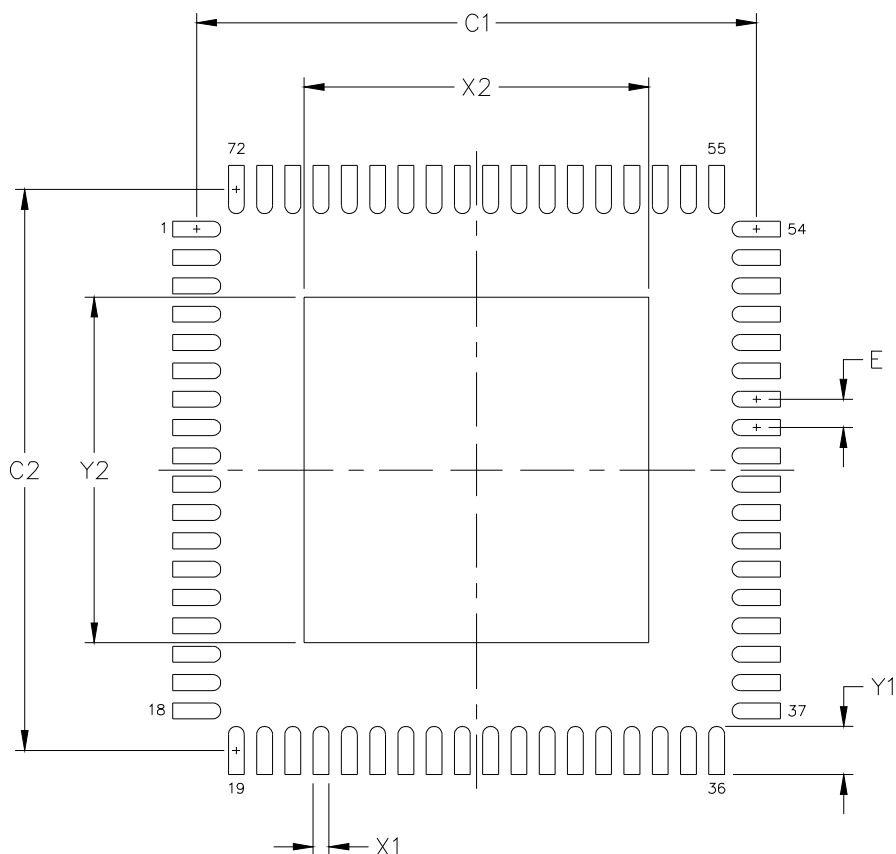


Figure 13. 72-pin QFN Land Pattern

Table 28. PCB Land Pattern Dimensions

| Dimension | mm |
|-----------|------|
| C1 | 9.90 |
| C2 | 9.90 |
| E | 0.50 |
| X1 | 0.30 |
| Y1 | 0.85 |
| X2 | 6.10 |
| Y2 | 6.10 |

DOCUMENT CHANGE LIST

Revision 0.9 to Revision 1.0

- Corrected specs in Table 6, “Phase Jitter,” on page 8.

Revision 1.0 to Revision 1.1

- Updated Features on page 1.
- Updated Description on page 1.
- Updated specs in Table 6, “Phase Jitter,” on page 8.

Revision 1.1 to Revision 1.2

February 22, 2016

- Corrected specs in Table 1, “DC Operating Characteristics,” on page 4.
- Updated operating characteristics in Table 3, Table 4, and Table 5.

Revision 1.2 to Revision 1.3

November 22, 2017

- Removed Gen4 PLL mode jitter spec.
- Added Table 25, “Byte 18: PLL Mode Control Register,” on page 25.



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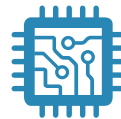
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