DATA SHEET



SKY77762 Power Amplifier Module for CDMA/ WCDMA/ HSDPA/ HSUPA/ HSPA+/ LTE – Band II (1850–1910 MHz)

Applications

- WCDMA handsets
- HSDPA
- HSUPA
- HSPA+
- LTE
- Band 25 (1850 MHz–1915 MHz)
- Band 39 (1850 MHz-1920 MHz)
- CDMA2000
- EVD0

Features

- Low voltage positive bias supply 3.0 V to 4.5 V
- · Good linearity
- High efficiency
- 46% at 28.6 dBm
- Large dynamic range
- Small, low profile package
 3 mm x 3 mm x 0.9 mm
- 10-pad configuration
- Power down control
- InGaP
- Supports low collector voltage operation
- Digital Enable
- No VREF required
- CMOS compatible control signals
- Integrated Directional Coupler



Skyworks Green[™] products are compliant with all applicable legislation and are halogen-free. For additional information, refer to Skyworks *Definition of Green^{™M}*, document number S004-0074.

Description

The SKY77762 Power Amplifier Module (PAM) is a fully matched 10-pad surface mount module developed for Wideband Code Division Multiple Access (WCDMA) applications. This small and efficient module packs full 1850-1910 MHz bandwidth coverage into a single compact package. Because of high efficiencies attained throughout the entire power range, the SKY77762 delivers unsurpassed talk-time advantages. The SKY77762 meets the stringent spectral linearity requirements of High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), and Long Term Evolution (LTE) data transmission with high power added efficiency. An integrated directional coupler eliminates the need for any external coupler.

The Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all amplifier active circuitry, including input and interstage matching circuits. The silicon CMOS support die, providing precision biasing for the MMIC affords a true CMOS-compatible control interface. Output match into a 50-ohm load, realized off-chip within the module package, optimizes efficiency and power performance.

The SKY77762 is manufactured with Skyworks' InGaP GaAs Heterojunction Bipolar Transistor (HBT) process which provides for all positive voltage DC supply operation and maintains high efficiency and good linearity. While primary bias to the SKY77762 can be supplied directly from any suitable battery with an output of 3.2 V to 4.2 V, optimal performance is obtained with VCC2 sourced from a DC-DC power supply adjusted within 0.5 V to 3.6 V based on target output power levels. Power down executes by setting VENABLE to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

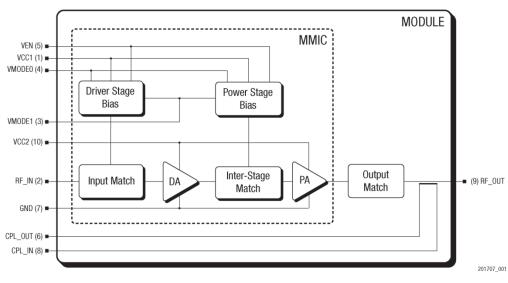


Figure 1. SKY77762 Functional Block Diagram

Electrical Specifications

The following tables list the electrical characteristics of the SKY77762 Power Amplifier. Table 1 lists the absolute maximum ratings and Table 2 shows the recommended operating conditions. Electrical specifications for nominal operating conditions are listed in Table 4. Table 3 presents a truth table for the power settings. Tables 5 through 8 provide the standard test configurations for WCDMA (STC1), HSDPA (STC2), and HSUPA (STC3, STC4) respectively.

No damage as	suming only or	ne parameter set	at limit at a time with	all other parameters se	et at nominal value.	-
Parameter		Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power		Pin	—	0	10	dBm
Supply Voltage	No RF	Vcc1	—	3.4	6.0	Volts
	With RF	Vcc2	—	—	4.6	
Enable Control Voltage		VEN	—	1.8	4.2	Volts
Mode Control Voltage		VMODEO	—	1.8	4.2	Volts
		VMODE1	—	1.8	4.2	
Case Temperature ¹	Operating	TCASE	-30	25	+110	°C
	Storage	Тѕтс	-40	—	+150	

 Table 1. Absolute Maximum Operating Conditions

 No damage assuming only one parameter set at limit at a time with all other parameters set at nominal values.

¹ Case Operating Temperature (TCASE) refers to the temperature of the GROUND PAD at the underside of the package.

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
		-		Hommu	maximum	
RF Output Power ¹	WCDMA	Pout_max	28.60	—	_	dBm
	HSDPA		27.60	—	_	
	HSUPA		25.00	—	—	
	LTE		27.60	—	—	
	CDMA2000		28.25	—	—	
Operating Frequency		fo	1850	1880	1910	MHz
Supply Voltage ²		Vcc1	3.0	3.4	4.5	Volts
		Vcc2	0.5	—	3.6	
Enable Control Voltage	Low	Ven_L	0.00	0.00	0.50	Volts
	High	Ven_h	1.35	1.80	3.10	
Mode Control Voltage	Low	VMODEO	0.0	0.0	0.5	Volts
		VMODE1	0.0	0.0	0.5	
	High	VMODEO	1.35	1.8	3.1	
		VMODE1	1.35	1.8	3.1	
Case Operating Temperature ³		TCASE	-20	+25	+85	°C

Table 2. Recommended Operating Conditions

¹ For VCC < 3.4 V, output power back-off = 0.5 dB.

² Specifications in Table 4 are specified at VCC1 = 3.2 V to 4.2 V.

³ Equivalent to -30 °C to +75 °C Ambient Operating Temperature.

le	anie 2. moues of ohere		Table 5. Modes of Operation								
Power Setting	ENABLE	VMODEO	VMODE1	VCC							
Power Down Mode	Low	Low	Low	On							
Standby Mode	Low	—	—	On							
High Power Mode (17.0 dBm \le Pout \le 28.6 dBm)	High	Low	—	On							
Medium Power Mode (7.0 dBm \leq Pout \leq 17.0 dBm)	High	High	Low	On							
Low Power Mode (Pout \leq 7.0 dBm)	High	High	High	On							

Table 3. Modes of Operation

 Table 4. Electrical Specifications for Nominal Operating Conditions (1 of 2)

 Per Table 2 over dynamic range up to 28.6 dBm output power for STC1 modulation, unless otherwise specified.

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain ¹		Glow	Роит = 7.0 dBm Vcc2 = 0.8 V	12.0	16.5	19.0	dB
		Gmed	Роит = 17.0 dBm Vcc2 = 1.5 V	20.0	24.5	28.0	
		Ghigh	Pout = 28.6 dBm	25.0	28.6	32.0	
Rx Band Gain		RxG	Pout = 28.6 dBm	—		-1	dB
		RxG_gps	Pout = 28.6 dBm	—		-2	
		RxG_ISM	Pout = 28.6 dBm	—	_	-7	
Power Added Efficiency		PAELOW	Pout = 7.0 dBm, Vcc2 = 0.8 V	11	13	—	%
		PAEMED	Pout = 17.0 dBm, Vcc2 = 1.5 V	22	26	—	
		PAEHIGH	Pout = 28.6 dBm	43	46	_	
Total Supply Current		Icc_low	Pout = 7.0 dBm, Vcc2 = 0.8 V	—	46	60	mA
		ICC_MED	Pout = 17.0 dBm, Vcc2 = 1.5 V	—	126	150	
		Ісс_нідн	Pout = 28.6 dBm	—	458	500	
Quiescent Current		lq_low	Low Power Mode	—	24	35	mA
		IQ_MED	Medium Power Mode		35	45	
Enable Control Current		len	-	—	20	40	μA
Mode Control Current		IMODEO	-	—	20	40	μA
		IMODE1	-	—	20	40	
Total Supply Current in Power Down Mode		IPD	$V_{CC} = 4.5 V$ $V_{EN} = Low$ $V_{MODE0} = Low$ $V_{MODE1} = Low$	_	1	10	μA
ICC1 Current		Ісс1_нідн	—	—	_	10	mA
Adjacent Channel Leakage power Ratio ²	5 MHz offset	ACLR5	Pout = 7.0 dBm	—	-43	-39	dBc
			Pouτ = 17.0 dBm	—	-45	-39	
			Pout = 28.6 dBm	—	-41	-39	
	10 MHz offset	ACLR10	Pouτ = 7.0 dBm	—	-67	-51	
			Pouτ = 17.0 dBm	—	-63	-51	
			Pout = 28.6	_	-55	-51	

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Adjacent Channel Leakage power Ratio ³	EUTRA offset	ACLR_EUTRA	Pout \leq (Pout_max – MPR ⁴)		-40	_	dBc
	UTRA offset	ACLR1_UTRA		_	-42	_	
		ACLR2_UTRA		_	_	— —	
Adjacent Channel Leakage power Ratio ³	EUTRA offset	ACLR_EUTRA	$POUT \le (POUT_MAX - MPR^4)$	_	-36.5	—	dBc
Band 25 (1850–1915 MHz)	UTRA offset	ACLR1_UTRA	_	_	-41.0	—	
		ACLR2_UTRA	_	_	-43.0	_	
	EUTRA offset	ACLR_EUTRA	$POUT \le (POUT_MAX - MPR^4)$	_	-37	_	dBc
Band 39 (1850-1920 MHz)	UTRA offset	ACLR1_UTRA		_	-41	_	
		ACLR2_UTRA		_	-43	_	
Adjacent Channel Power Ratio ^{5,6}	1.25 MHz offset	ACPR1	Pout = 28.25 dBm	_	-48	—	dBc
	1.98 MHz offset	ACPR2		_	-55	_	
Harmonic Suppression	Second	fo2	Pout ≤ 28.6 dBm	_	-53	-35	dBc
	Third	fo3		_	-50	-43	
Tx Noise in Rx Bands ¹	Rx Band II		1930 MHz–1990 MHz Pout = 28.6 dBm	-	_	-135.0	dBm/Hz
	GPS Rx		1574 MHz–1577 MHz Роит = 28.6 dBm	-	_	-137.0	
	ISM Rx		2400 MHz-2483.5 MHz Pout = 28.6 dBm	-	_	-144.5	
EVM		EVM1	Pout = Pout_max	—		3.75	%
		EVM2	Pout = Pout_max - 3	_	_	3.25	
Rise / Fall Time	DC	TON_DC	_	_	_	20	μs
		TOFF_DC	_	_		20	
	RF	TON_RF	_	—		6	
		TOFF_RF	_	_	_	6	
Coupling Factor		CPL	Pout = Pout_max	-22	-20	-18	dB
CPL_out / Pout Power Ratio Variation Over Outpu	t VSWR		2.5:1 VSWR at Pou⊤ all VSWR phases CPL_N 50 Ω terminated	_	±0.30	_	dB
Daisy-chain	VSWR		CPL_IN and CPL_OUT ports 698 MHz to 2620 MHz VEN = Low	—	_	1.6:1	
	Insertion Loss			—		0.25	dB
Input Voltage Standing Wave Ratio		VSWR	—	_	1.6:1	1.85:1	
Stability (Spurious output) ¹		S	6:1 VSWR All phases	_		-70	dBc
Ruggedness – no damage ^{1,7}		Ru	Pout ≤ 28.6 dBm	10:1	_	_	VSWR

 Table 4. [continued]
 Electrical Specifications for Nominal Operating Conditions (2 of 2)

 Table 2 over dynamic range up to 28.6 dBm output power for STC1 modulation. unless otherwise specified.

¹ Over conditions

² ACLR is expressed as a ratio of total adjacent power to WCDMA modulated in-band, both measured in 3.84 MHz bandwidth at specified offsets.

³ LTE: ACLR is measured with QPSK modulation with 20 MHz bandwidth and 18 resource blocks. (Maximum Power Reduction = 0 dBm per 3GPP TS36.101.

⁴ MPR is the maximum power reduction as defined in 3GPP TS36.101

⁵ ACPR is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

⁶ For CDMA2000 test configured as [PCD @ -7.40 dB, DCCH–9600 bps @ -15.35 dB; SCH0–9600 bps @ -15.63 dB] and other test configurations that yield a peak-to-average up to 4.02 dB for CCDF = 1%, up to 1 dB power back off from the maximum listed for IS95 may be required to meet specified maximum ACP performance under worst-case conditions.

⁷ All phases, time = 10 seconds.

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Parameter	Level	Spread Code	Spread Factor	I/Q	βc	βd	βhs	βec	βed	Relative Power (dB)
DPCCH	15 kbps	0	256	Q	8/15	—	—		—	-6.547
DPDCH	60 kbps	16	64	I	—	15/15	—		—	-1.087

Table 5. Standard Test Configuration – STC1 WCDMA Mode

Table 6.	Standard Test	Configuration –	STC2	HSDPA	Mode
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Parameter	Level	Spread Code	Spread Factor	I/Q	βc	βd	βhs	βec	βed	Relative Power (dB)
DPCCH	15 kbps	0	256	Q	12/15	—	_		—	-7.095
DPDCH	60 kbps	16	64	I	_	15/15	_	_	—	-5.157
HS-DPCCH	15 kbps	64	256	Q		—	24/15		—	-3.012

	Table 7. Standard Test Configuration – 5105 fisch A mode									
Parameter	Level	Spread Code	Spread Factor	I/Q	βc	βd	βhs	βec	βed	Relative Power (dB)
DPCCH	15 kbps	0	256	Q	8/15	_			—	-19.391
DPDCH	960 kbps	1	4	I	-	15/15	-	-	—	-13.931
HS- DPCCH	15 kbps	64	256	Q	_	_	8/15	_	—	-19.391
E-DPCCH	15 kbps	1	256	I	_	_	_	10/15	—	-17.338
E-DPDCH	960 kbps	2	4	I	_	_	_	_	71.5/15	-0.371

Table 7. Standard Test Configuration – STC3 HSUPA Mode

 Table 8. Standard Test Configuration – STC4 HSUPA Mode

Parameter	Level	Spread Code	Spread Factor	I/Q	βc	βd	βhs	βес	βed	Relative Power (dB)
DPCCH	15 kbps	0	256	Q	6/15		—	—	—	-12.499
DPDCH	960 kbps	1	4	I	—	15/15	—	—	—	-4.540
HS- DPCCH	15 kbps	64	256	Q	—		2/15	—	—	-22.041
E-DPCCH	15 kbps	1	256	I	—		—	12/15	—	-6.478
E-DPDCH	960 kbps	2	4	ļ	—	_	—	—	15/15	-4.425

Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the SKY77762, the evaluation board schematic and assembly diagrams are included for analysis and design. Figure 2 shows

the basic schematic of the board for the 1850 MHz to 1910 MHz range shown in Figure 3. Figure 4 is a schematic of the recommended application shown in Figure 5.

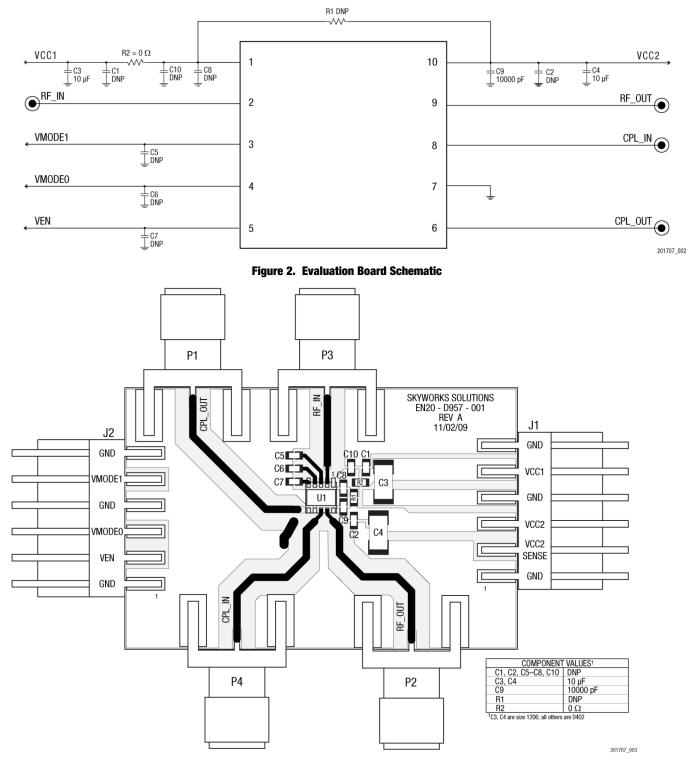


Figure 3. Evaluation Board Assembly Diagram

VCC1 = 3.2 V to 4.2 V from Battery VCC2 = 0.5 V to 4.2 V from DC/DC (10 mA MAX current drain) (High Current Drain) VCC1 VCC2 └_ C9 ┬─ 10000 pF 1850 to 1910 MHz 1850 to 1910 MHz RF Output to Band Duplexer **RF Input from Transceiver** RF_OUT $Z0 = 50 \Omega$ RF_IN $Z0 = 50 \Omega$ VMODE1 Digital Control from Transceiver Hi Z VMODE1 CPL_IN $Z0 = 50 \Omega$ $\leq 50 \Omega$ 1..... VMODE0 Digital Control from Transceiver Hi Z VMODEO GND VEN Digital 1850 to 1910 MHz Coupled to Power Detector Control from Transceiver CPL_OUT Hi 7 Z0 = 50 Ω VEN GROUND PAD ӡ

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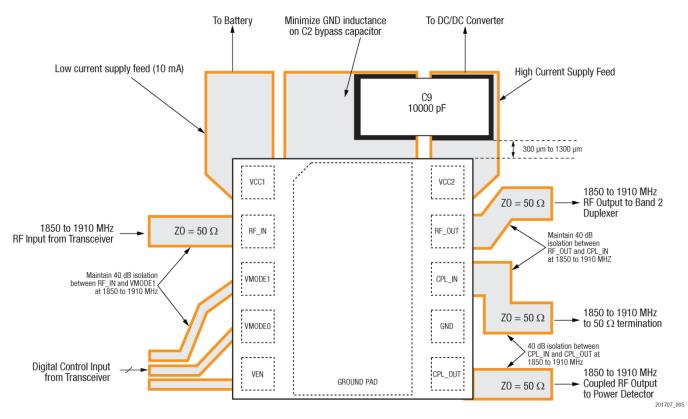


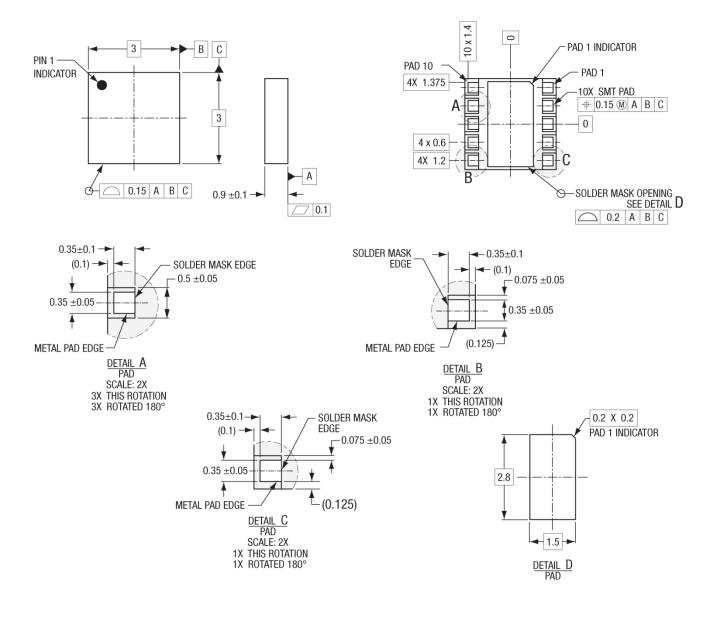
Figure 5. SKY77762 Recommended Application Diagram

DATA SHEET

Package Dimensions

The SKY77762 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board. Figure 6 is a mechanical drawing of the pad layout for this package. Figure 7 provides a

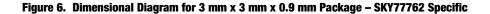
recommended phone board layout footprint for the PAM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50-ohm terminals.

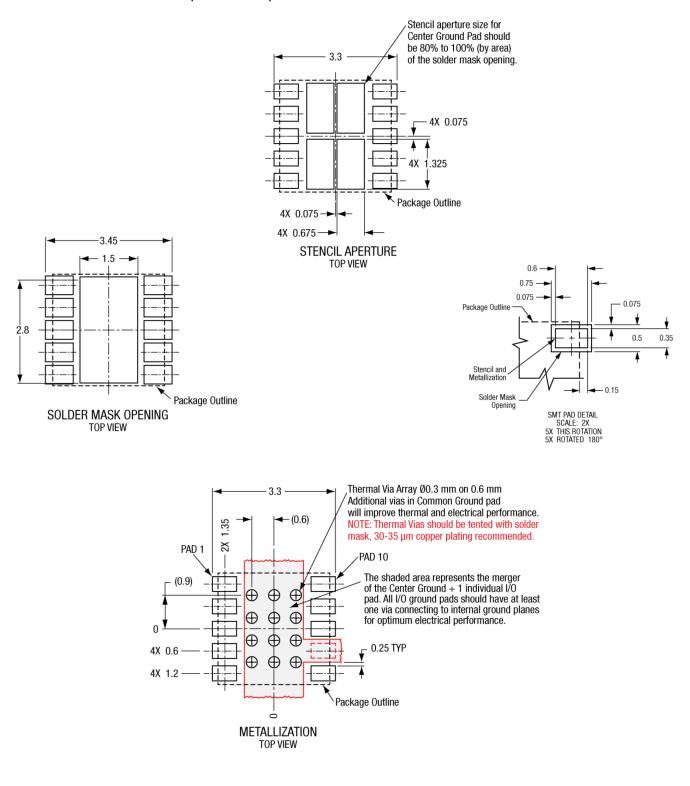


NOTES: Unless otherwise specified.

Dimensioning and Tolerancing in accordance with ASME Y14.5M–1994
 All dimensions are in millimeters.

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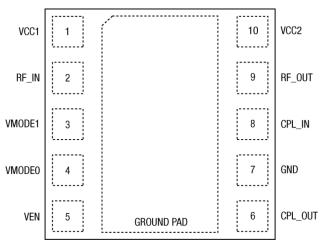


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Figure 7. Phone PCB Layout Diagram – 3 mm x 3 mm, 10-Pad Package – SKY77762

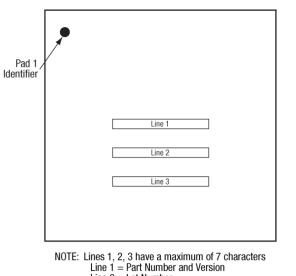
Package Description

Figure 8 shows the pad functions and the pad numbering convention, which starts with pad 1 in the upper left and increments counter-clockwise around the package. Typical case markings are illustrated in Figure 9.



Pad layout as seen from Top View looking through the package. GROUND PAD is package underside. $$_{\rm 201707\ 006}$$

Figure 8. SKY77762 Pad Names and Configuration (Top View)



Line 2 = Lot Number Line 3 = Year–Week–Country Code (MX)

Figure 9. Typical Case Markings

Package Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY77762 is capable of withstanding an MSL3/260 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 3 °C per second; maximum temperature should not exceed 260 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 260 °C for more than 10 seconds. For details on attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to Skyworks Application Note: *PCB Design and SMT Assembly/Rework*, Document Number 101752. Additional information on standard SMT reflow profiles can also be found in the JEDEC Standard J-STD-020.

Production quantities of this product are shipped in the standard tape-and-reel format (Figure 10).

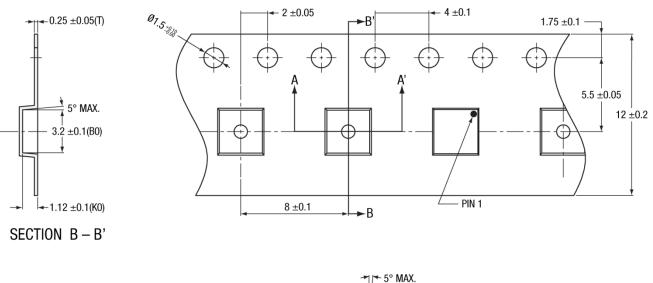
Electrostatic Discharge (ESD) Sensitivity

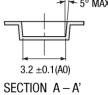
The SKY77762 meets class 1C JESD22-A114 Human Body Model (HBM), class IV JESD22-C101 Charged-Device Model (CDM), and class A JESD22-A115 Machine Model (MM) electrostatic discharge (ESD) sensitivity classification.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the ESD handling precautions listed below.

- Personnel Grounding
 - Wrist Straps
 - Conductive Smocks, Gloves and Finger Cots
 - Antistatic ID Badges
- Protective Workstation
 - Dissipative Table Top
 - Protective Test Equipment (Properly Grounded)
 - Grounded Tip Soldering Irons
 - Solder Conductive Suckers
 - Static Sensors
- Facility
- Relative Humidity Control and Air Ionizers
- Dissipative Floors (less than 1,000 MΩ to GND)
- Protective Packaging and Transportation
 - Bags and Pouches (Faraday Shield)
 - Protective Tote Boxes (Conductive Static Shielding)
 - Protective Trays
 - Grounded Carts
 - Protective Work Order Holders

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NOTES:

- 1. CARRIER TAPE IS BLACK CONDUCTIVE POLYCARBONATE OR POLYSTYRENE.
- 2. COVER TAPE IS TRANSPARENT AND CONDUCTIVE.
- 3. ESD-SURFACE RESISTIVITY IS \leq 1 X 10¹⁰ OHMS/SQUARE PER EIA, JEDEC TNR SPECIFICATION. 4. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE: ±0.2 mm
- 5. Ao & Bo MEASURED ON PLANE 0.3 mm ABOVE THE BOTTOM OF THE POCKET.
- 6. ALL DIMENSIONS ARE IN MILLIMETERS.

CARRIER TAPE OVERMOLD MCM / RFLGA 3 x 3 x 0.75 / 0.90 mm BODY SIZE -108A 201075_008



Ordering Information

Product Name	Manufacturing Part Number	Evaluation Board Part Number
SKY77762 Power Amplifier Module	SKY77762-11	EN20-D957-001 REV A

Revision History

Revision	Date	Description
А	December 27, 2011	Initial Release – Information
В	March 9, 2012	Revise: Figure 1–3, 6, 7; Table 4 and footnotes 4, 5 Add: Figures 4, 5
C	May 5, 2012	Revise: Data Sheet status from ADVANCE to PRELIMINARY; Features list (p1); Description (p1); Tables 2, 4; Figures 4, 5
D	August 1, 2012	Revise: Add footnote 3 to Table 2
E	August 3, 2012	Revise: Change Data Sheet status from PRELIMINARY to FINAL; Table 4; Order Information Table (last page)
F	September 20, 2012	Revise: Features list (p1); Tables 2, 4

References

Skyworks Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752.

Standard SMT Reflow Profiles: JEDEC Standard J-STD-020

Electrostatic Discharge Sensitivity (ESD) Testing: JEDEC Standard, JESD22-A114 Human Body Model (HBM)

Electrostatic Discharge Sensitivity (ESD) Testing: JEDEC Standard, JESD22-A115 Machine Model (MM)

Electrostatic Discharge Sensitivity (ESD) Testing: JEDEC Standard, JESD22-C101 Charged Device Model (CDM).

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