

DATA SHEET

SKY13550-667LF: 0.4 to 3.8 GHz DP8T (SP4T/SP4T) Main/Receive Diversity Switch with MIPI RFFE Interface for Carrier Aggregation

Applications

- 3G/4G multimode cellular handsets (UMTS and CDMA2000)
- Carrier aggregation diversity

Features

- Broadband frequency range: 0.4 to 3.8 GHz
- Single, positive DC power supply (2.5 to 4.8 V)
- Excellent Band 13 2nd harmonic performance
- Excellent Band 17 3rd harmonic performance
- Integrated, programmable MIPI interface using separate registers for ANT_A and ANT_B bands
- Dual antenna ports can be connected externally to a diplexer
- Small QFN (14-pin, 1.6 x 2.0 x 0.55 mm) package (MSL1, 260 °C per JEDEC J-STD-020)



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Description

The SKY13550-667LF is a dual single-pole, four-throw (2xSP4T) Mobile Industry Processor Interface (MIPI) controlled antenna switch designed specifically for receive diversity in carrier aggregation applications.

The 2xSP4T switch is optimized for broadband performance. Using advanced switching technologies, the SKY13550-667LF maintains low insertion loss and high isolation for all switching paths. The high linearity performance and low insertion loss achieved by the SKY13550-667LF makes it an ideal choice for carrier aggregation applications. The switch also exhibits excellent second/third order intermodulation distortion (IMD2/IMD3) performance.

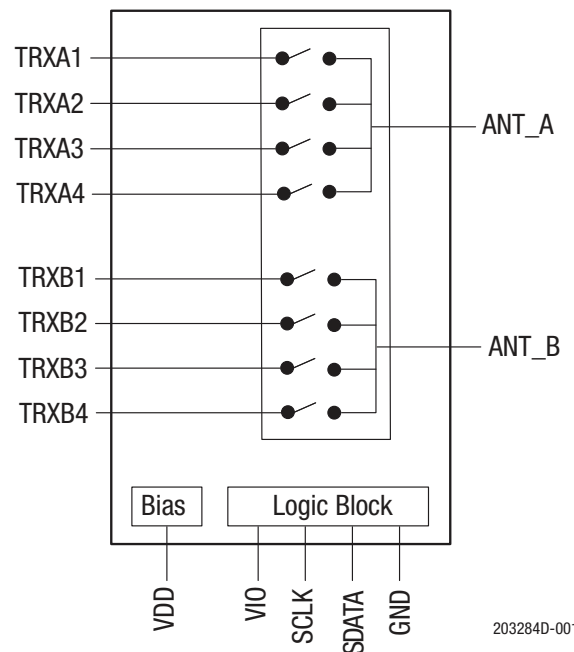


Figure 1. SKY13550-667LF Block Diagram

Switching is controlled by an integrated MIPI decoder. The two switches can be configured independently. There are separate registers for each SP4T. No external DC blocking capacitors are required on the RF paths as long as no DC voltage is applied to those paths.

The SKY13550-667LF is manufactured in a compact, 1.6 x 2.0 x 0.55 mm, 14-pin surface-mount Quad Flat No-Lead (QFN) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

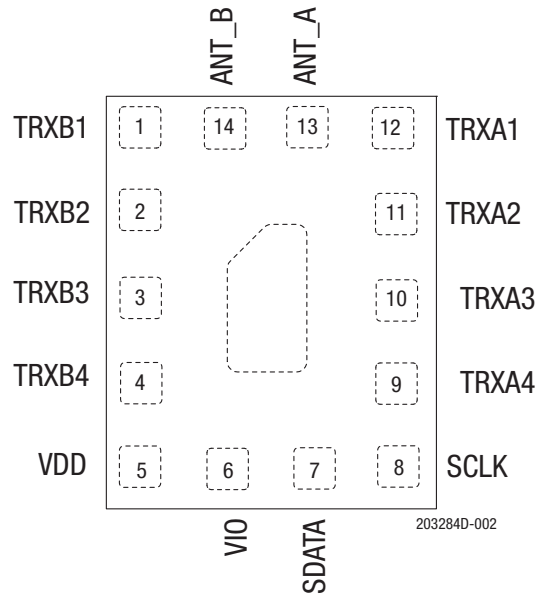


Figure 2. SKY13550-667LF Pinout (Top View)

Table 1. SKY13550-667LF Signal Descriptions¹

| Pin | Name | Description | Pin | Name | Description |
|-----|-------|------------------------------|-----|-------|------------------------------|
| 1 | TRXB1 | ANT_B transmit/receive arm 1 | 8 | SCLK | Clock |
| 2 | TRXB2 | ANT_B transmit/receive arm 2 | 9 | TRXA4 | ANT_A transmit/receive arm 4 |
| 3 | TRXB3 | ANT_B transmit/receive arm 3 | 10 | TRXA3 | ANT_A transmit/receive arm 3 |
| 4 | TRXB4 | ANT_B transmit/receive arm 4 | 11 | TRXA2 | ANT_A transmit/receive arm 2 |
| 5 | VDD | DC supply voltage | 12 | TRXA1 | ANT_A transmit/receive arm 1 |
| 6 | VIO | MIPI interface DC voltage | 13 | ANT_A | Antenna A port |
| 7 | SDATA | Data | 14 | ANT_B | Antenna B port |

¹ Bottom ground paddles must be connected to ground.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13550-667LF are provided in Table 2. Electrical specifications are provided in Tables 3 and 4.

IMD2 and IMD3 test conditions for various frequencies are listed in Tables 5 and 6, respectively.

Figure 3 illustrates the test setup used to measure intermodulation products. This industry standardized test is used to simulate the WCDMA linearity of the antenna switch. A +20 dBm Continuous Wave (CW) signal, f_{FUND} , is sequentially applied to the TRX ports, while a -15 dBm CW blocker signal, f_{BLK} , is applied to the ANT port.

The resulting third order intermodulation distortion (IMD3), f_{RX} , is measured over all phases of f_{FUND} . The SKY13550-667LF exhibits exceptional performance for all RF ports.

Table 7 describes the register content and programming read/write sequences. Refer to the *MIPI Alliance Specification for RF Front-End Control Interface (RFFE)*, v1.10 (26 July 2011) for additional information on MIPI programming sequences and MIPI bus specifications.

Figure 4 provides the timing diagram for register write commands. Figure 5 provides the timing diagram for register read commands.

Register descriptions and programming information is provided in Table 8. Tables 9 and 10 provide the Register_0 and Register_1 logic, respectively.

Table 2. SKY13550-667LF Absolute Maximum Ratings¹

| Parameter | Symbol | Minimum | Maximum | Units |
|------------------------|--------|---------|---------|-------|
| Supply voltage | VDD | 2.5 | 5.0 | V |
| Digital control signal | VIO | | 2 | V |
| SCLK port voltage | SCLK | | VIO | V |
| SDATA port voltage | SDATA | | VIO | V |
| LTE input power | PIN | | +31 | dBm |
| Storage temperature | TSTG | -55 | +150 | °C |
| Operating temperature | TOP | -30 | +90 | °C |

¹ Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 3. SKY13550-667LF RF Electrical Specifications¹ (1 of 2)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z₀] = 50 Ω, Unless Otherwise Noted)

| Parameter | Symbol | Test Condition | Min | Typical | Max | Units | |
|---------------------|--------|--|-----|---------|------|-------|--|
| Operating frequency | f | | 0.4 | | 3.8 | GHz | |
| Insertion loss | IL | ANT_A to any TRXA port, ANT_B to any TRXB port: | | | | | |
| | | 400 to 824 MHz | | 0.35 | 0.55 | dB | |
| | | 824 to 960 MHz | | 0.4 | 0.6 | dB | |
| | | 1427 to 1511 MHz | | 0.5 | 0.7 | dB | |
| | | 1710 to 2170 MHz | | 0.65 | 0.8 | dB | |
| | | 2170 to 2690 MHz | | 0.8 | 0.95 | dB | |
| | | 3400 to 3800 MHz | | 1.4 | 1.6 | dB | |
| Isolation | Iso | ANT_A to any OFF TRXA port, ANT_B to any OFF TRXB port: | | | | | |
| | | Up to 787 MHz | 33 | 36 | | dB | |
| | | Up to 960 MHz | 32 | 34 | | dB | |
| | | Up to 1511 MHz | 25 | 29 | | dB | |
| | | Up to 1990 MHz | 24 | 27 | | dB | |
| | | Up to 2170 MHz | 23 | 26 | | dB | |
| | | Up to 2690 MHz | 21 | 23 | | dB | |
| | | Up to 3800 MHz | 17 | 19 | | dB | |
| | | ANT_A to any TRxB port, ANT_B to any TRxA port: | | | | | |
| | | Up to 704 MHz | 41 | 43 | | dB | |
| | | Up to 960 MHz | 39 | 41 | | dB | |
| | | Up to 1511 MHz | 35 | 37 | | dB | |
| | | Up to 1990 MHz | 33 | 35 | | dB | |
| | | Up to 2170 MHz | 32 | 34 | | dB | |
| | | Up to 2690 MHz | 30 | 32 | | dB | |
| | | Up to 3800 MHz | 25 | 27 | | dB | |
| | | ANT_A to ANT_B: | | | | | |
| | | 400 to 960 GHz | 32 | 34 | | dB | |
| 1427 to 1511 MHz | 28 | 30 | | dB | | | |
| 1710 to 1980 GHz | 26 | 28 | | dB | | | |
| 1980 to 2690 MHz | 23 | 25 | | dB | | | |
| 3400 to 3800 GHz | 20 | 22 | | dB | | | |

Table 3. SKY13550-667LF RF Electrical Specifications¹ (2 of 2)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z₀] = 50 Ω, Unless Otherwise Noted)

| Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|--|-----------------|---|-----|---------|-------|-------|
| ON state match | VSWR | 400 to 2170 MHz | | 1.2:1 | 1.5:1 | |
| Second order intermodulation distortion | IMD2 | See Table 5 | | -110 | -105 | dBm |
| Third order intermodulation distortion | IMD3 | See Table 6 | | -110 | -105 | dBm |
| Low band 2 nd and 3 rd harmonic | 2fo, 3fo | Any TRX port, P _{IN} = +25 dBm, f = 900 MHz | | -70 | -65 | dBm |
| Low band 2 nd and 3 rd harmonic | 2fo, 3fo | Any TRX port, P _{IN} = +25 dBm, f ₀ = 900 MHz, VSWR = 5:1 | | -65 | -60 | dBm |
| Mid band 2 nd and 3 rd harmonic | 2fo, 3fo | Any TRXA and any TRXB port, P _{IN} = +26 dBm, f ₁ = 1462 MHz, f ₂ = 1910 MHz | | -70 | -65 | dBm |
| Mid band 2 nd and 3 rd harmonic | 2fo, 3fo | Any TRXA and any TRXB port, P _{IN} = +26 dBm, f ₁ = 1462 MHz, f ₂ = 1910 MHz, VSWR = 5:1 | | -63 | -60 | dBm |
| High band 2 nd and 3 rd harmonic | 2fo, 3fo | Any TRXA and any TRXB port, P _{IN} = +25 dBm, f ₀ = 2690 MHz | | -70 | -65 | dBm |
| High band 2 nd and 3 rd harmonic | 2fo, 3fo | Any TRXA and any TRXB port, P _{IN} = +25 dBm, f ₀ = 2690 MHz, VSWR = 5:1 | | -62 | -60 | dBm |
| Band 13 2 nd harmonic | 2fo | Any TRX port, P _{IN} = +25 dBm, f ₀ = 777 to 787 MHz | | -81 | | dBm |
| Band 17 3 rd harmonic | 3fo | Any TRX port, P _{IN} = +25 dBm, f = 707 MHz | | -80 | | dBm |
| Turn-on time | t _{ON} | From application of V _{DD} and V _{IO} , or transition from low power mode | | 4 | 10 | μs |
| Wake-up time | t _w | From isolation state | | 2 | 5 | μs |
| Switching speed | t _s | Any state to any other state | | 2 | 5 | μs |

¹ Performance is guaranteed only under the conditions listed in this table.

Table 4. SKY13550-667LF DC Electrical Specifications¹
 (V_{DD} = 2.85 V, V_{IO} = 1.8 V, T_{OP} = +25 °C, Characteristic Impedance [Z₀] = 50 Ω, Unless Otherwise Noted)

| Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|--|------------------|----------------|----------------------------|---------|--|--------|
| Supply voltage | V _{DD} | | 2.50 | 2.85 | 4.8 | V |
| Supply current, active mode | I _{DD} | | | 50 | 100 | μA |
| Interface supply voltage level | V _{IO} | | 1.65 | 1.80 | 1.95 | V |
| Digital data and clock signals: High Low | SDATA, SCLK | | 0.8 × V _{IO} 0 | | V _{IO} 0.2 × V _{IO} | V V |
| Interface supply current | I _{vio} | | | 5 | 50 | μA |

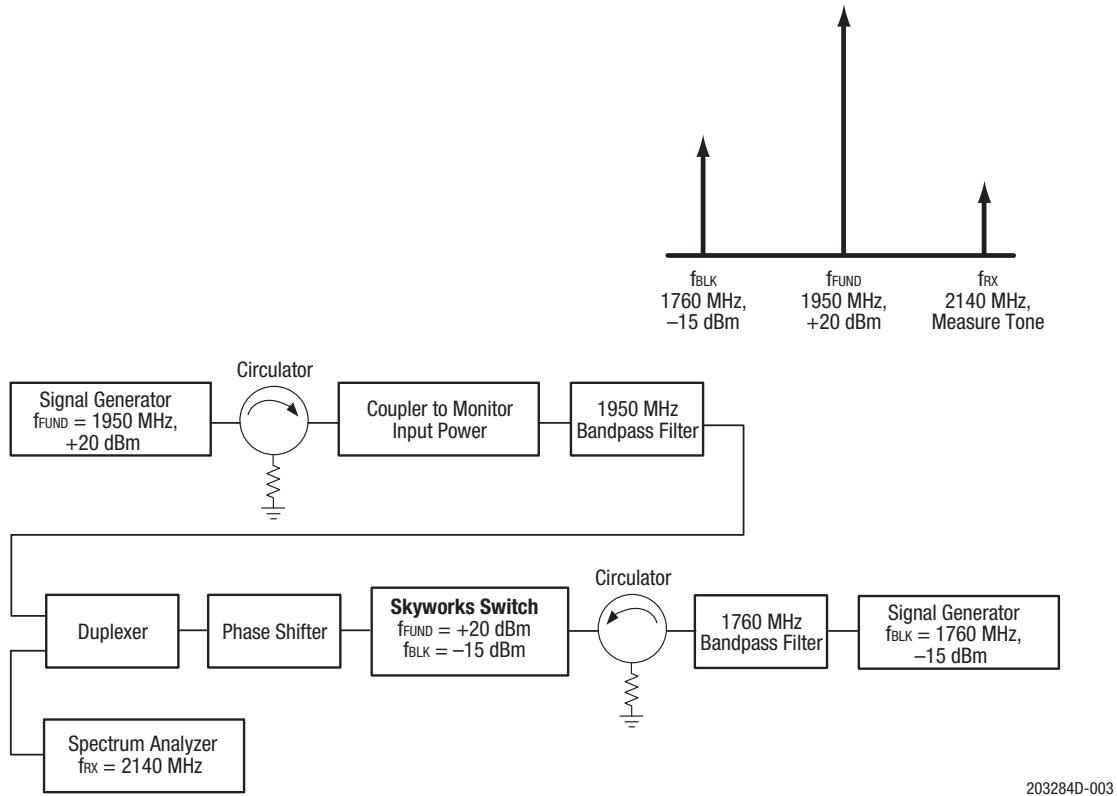
¹ Performance is guaranteed only under the conditions listed in this table.

Table 5. IMD2 Test Conditions

| Band | Transmit Frequency (MHz) | Transmit Power (dBm) | Frequency Blocker, Low (MHz) | Frequency Blocker, High (MHz) | Power Blocker (dBm) | Receive Frequency (MHz) |
|-------|--------------------------|----------------------|------------------------------|-------------------------------|---------------------|-------------------------|
| 1 | 1950.0 | +20 | 190 | 4090 | -15 | 2140.0 |
| 2 | 1880.0 | | 80 | 3840 | | 1960.0 |
| 4 | 1732.0 | | 400 | 3864 | | 2132.0 |
| 5 | 836.5 | | 45 | 1718 | | 881.5 |
| 7 | 2535.0 | | 120 | 5190 | | 2655.0 |
| 8 | 897.0 | | 45 | 1839 | | 942.0 |
| 11/21 | 1452.0 | | | 2952 | | 1500 |

Table 6. IMD3 Test Conditions

| Band | Transmit Frequency (MHz) | Transmit Power (dBm) | Frequency Blocker (MHz) | Power Blocker (dBm) | Receive Frequency (MHz) |
|-------|--------------------------|----------------------|-------------------------|---------------------|-------------------------|
| 1 | 1950.0 | +20 | 1760.0 | -15 | 2140.0 |
| 2 | 1880.0 | | 1800.0 | | 1960.0 |
| 4 | 1732.0 | | 1332.0 | | 2132.0 |
| 5 | 836.5 | | 791.5 | | 881.5 |
| 7 | 2535.0 | | 2415.0 | | 2655.0 |
| 8 | 897.0 | | 852.0 | | 942.0 |
| 11/21 | 1452 | | 1404 | | 1500 |



203284D-003

Figure 3. Typical Third Order Intermodulation Test Setup

Table 7. Command Sequence Bit Definitions

| Type | SSC | C11-C8 | C7 | C6-C5 | C4 | C3-C0 | Parity Bits | BPC | Extended Operation | | | | | |
|----------------------------|-----|---------|----|-----------|---------|-----------|-------------|-----|--------------------|-------------|-----|---------------|-------------|-----|
| | | | | | | | | | DA7(1)-DA0(1) | Parity Bits | BPC | DA7(n)-DA0(n) | Parity Bits | BPC |
| Reg_0 Write, Short Command | Y | SA[3:0] | 1b | Data[6:5] | Data[4] | Data[3:0] | Y | Y | - | - | - | - | - | - |
| Reg_0 Write, Long Command | Y | SA[3:0] | 0 | 10b | Addr[4] | Addr[3:0] | Y | - | Data[7:0] | - | - | - | Y | Y |
| Reg_1 Write | Y | SA[3:0] | 0 | 10b | Addr[4] | Addr[3:0] | Y | - | Data[7:0] | - | - | - | Y | Y |
| Reg Read | Y | SA[3:0] | 0 | 11b | Addr[4] | Addr[3:0] | Y | Y | Data[7:0] | - | - | - | Y | Y |

Legend:

SSC = Sequence start command
C = Command frame bits

DA = Data/address frame bits
BPC = Bus park cycle

BC = Byte count (number of consecutive addresses)

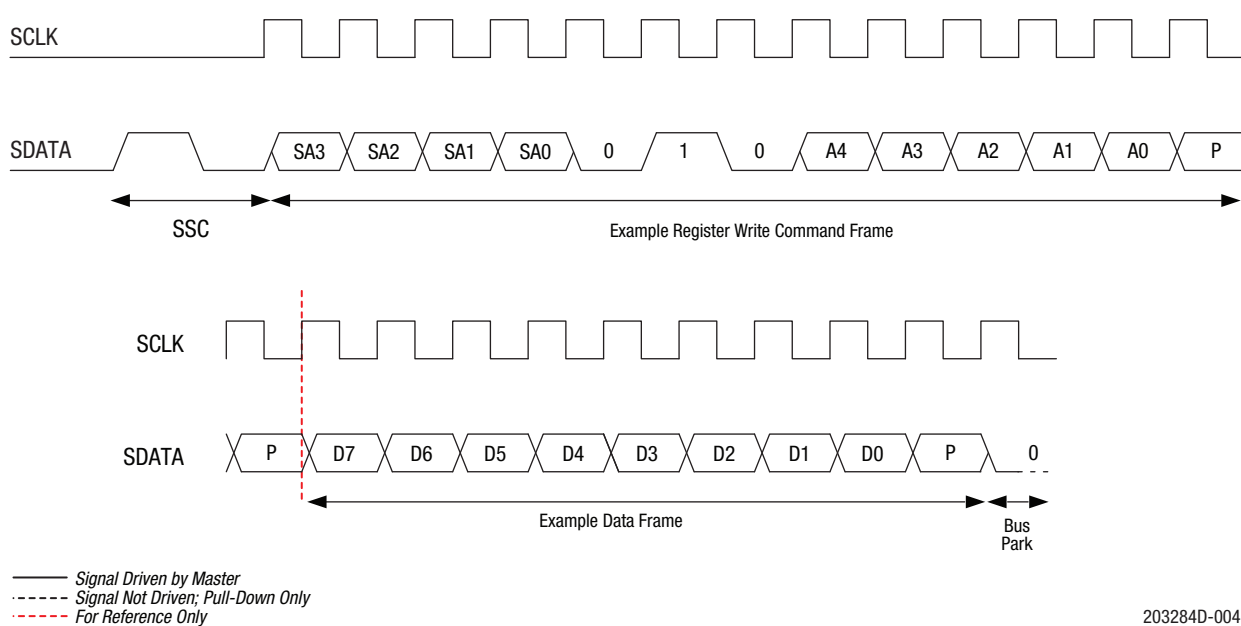


Figure 4. Register Write Command Timing Diagram

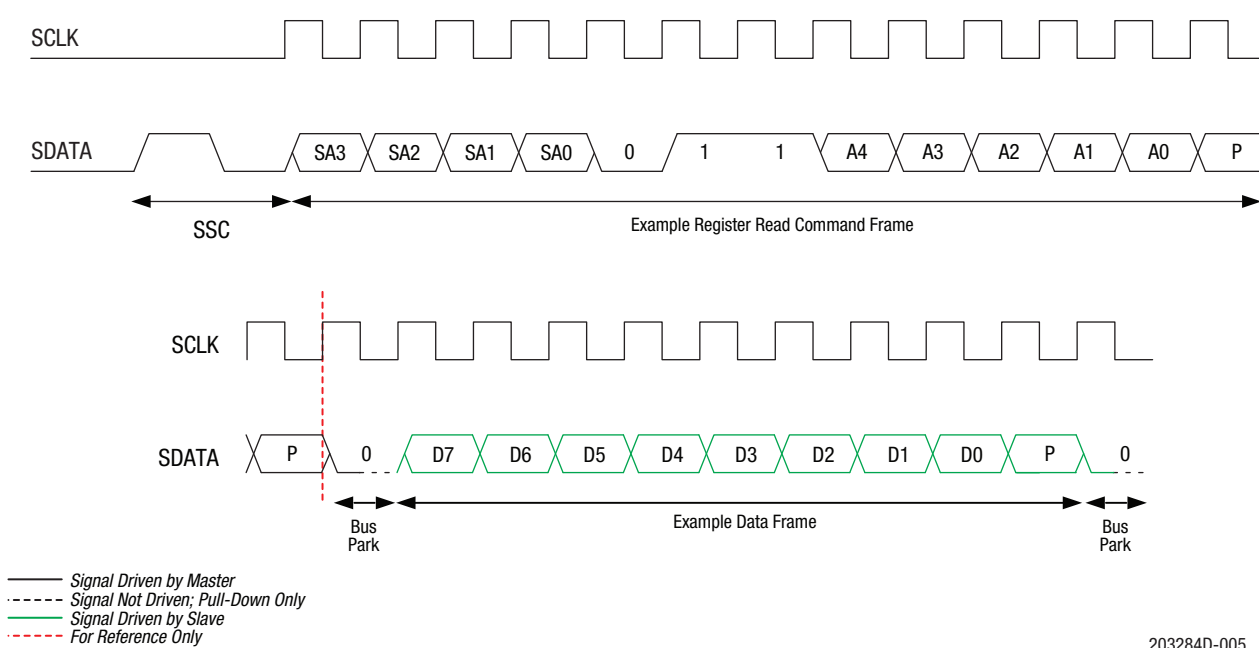


Figure 5. Register Read Command Timing Diagram

Table 8. Register Description and Programming¹

| Register | | Parameter | Description | Default (Binary) |
|---------------------|---------------|-----------------|---|------------------|
| Name | Address (Hex) | | | |
| Register_0 | 0000 | MODE_CTRL | Bits[6:0]: See Table 10 for logic | 0000000 |
| Register_1 | 0001 | MODE_CTRL | Bits[7:0]: See Table 11 for logic | 00000000 |
| PM_TRIG (Note 1) | 001C | PWR_MODE | Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved | 00 |
| | | Trigger_Mask_2 | Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register. | 0 |
| | | Trigger_Mask_1 | Bit[4]: If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register. | 0 |
| | | Trigger_Mask_0 | Bit[3]: If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register. | 0 |
| | | Trigger_2 | Bit[2]: If this bit is set, data is loaded into the trigger 2 registers. | 0 |
| | | Trigger_1 | Bit[1]: If this bit is set, data is loaded into the trigger 1 registers. | 0 |
| | | Trigger_0 | Bit[0]: If this bit is set, data is loaded into the trigger 0 registers. | 0 |
| PRODUCT_ID | 001D | PRODUCT_ID | Bits[7:0]: This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed. | 11010011 |
| MANUFACTURER_ID | 001E | MANUFACTURER_ID | Bits[7:0]: Read-only register | 10100101 |
| MAN_USID | 001F | Reserved | Bits[7:6]: Reserved | 00 |
| | | MANUFACTURER_ID | Bits[5:4]: Read-only register | 01 |
| | | USID | Bits[3:0]: Programmable USID. A write to these bits programs the USID. | 1010 |

¹ Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification, this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular trigger used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

Table 9. Register_0 Truth Table (ANT_B)

| ON State | Register 0 Bits | | | | | | | |
|---------------|-----------------|----|----|----|----|----|----|----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| All isolation | | | | 0 | 0 | 0 | 0 | 0 |
| TRXB1 | | | | 0 | 0 | 0 | 0 | 1 |
| TRXB2 | | | | 0 | 0 | 0 | 1 | 0 |
| TRXB3 | | | μ | 0 | 0 | 0 | 1 | 1 |
| TRXB4 | | | | 0 | 0 | 1 | 0 | 0 |
| Isolation | | | | 0 | 0 | 1 | 0 | 1 |
| Isolation | | | | 0 | 0 | 1 | 1 | 0 |
| Isolation | | | | 0 | 0 | 1 | 1 | 1 |
| TRXB4 | | | | 0 | 1 | 0 | 0 | 0 |
| TRXB3 | | | | 0 | 1 | 0 | 0 | 1 |
| TRXB2 | | | | 0 | 1 | 0 | 1 | 0 |
| TRXB1 | | | | 0 | 1 | 0 | 1 | 1 |
| TRXB4 | | | | 0 | 1 | 1 | 0 | 0 |
| TRXB3 | | | | 0 | 1 | 1 | 0 | 1 |
| TRXB2 | | | | 0 | 1 | 1 | 1 | 0 |
| TRXB1 | | | | 0 | 1 | 1 | 1 | 1 |
| TRXB4+3 | | | | 1 | 0 | 0 | 0 | 0 |
| TRXB4+2 | | | | 1 | 0 | 0 | 0 | 1 |
| TRXB4+1 | | | | 1 | 0 | 0 | 1 | 0 |
| TRXB3+2 | | | | 1 | 0 | 0 | 1 | 1 |
| TRXB3+1 | | | | 1 | 0 | 1 | 0 | 0 |
| TRXB2+1 | | | | 1 | 0 | 1 | 0 | 1 |
| All isolation | | | | 1 | 0 | 1 | 1 | 0 |
| All isolation | | | | 1 | 0 | 1 | 1 | 1 |
| All isolation | | | | 1 | 1 | 0 | 0 | 0 |
| All isolation | | | | 1 | 1 | 0 | 0 | 1 |
| All isolation | | | | 1 | 1 | 0 | 1 | 0 |
| All isolation | | | | 1 | 1 | 0 | 1 | 1 |
| All isolation | | | | 1 | 1 | 1 | 0 | 0 |
| All isolation | | | | 1 | 1 | 1 | 0 | 1 |
| All isolation | | | | 1 | 1 | 1 | 1 | 0 |
| All isolation | | | | 1 | 1 | 1 | 1 | 1 |

Table 10. Register_1 Truth Table (ANT_A)

| Mode | Register 1 Bits | | | | | | | |
|---------------|-----------------|----|----|----|----|----|----|----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| All isolation | | | | 0 | 0 | 0 | 0 | 0 |
| TRXA1 | | | | 0 | 0 | 0 | 0 | 1 |
| TRXA2 | | | | 0 | 0 | 0 | 1 | 0 |
| TRXA3 | | | | 0 | 0 | 0 | 1 | 1 |
| TRXA4 | | | | 0 | 0 | 1 | 0 | 0 |
| Isolation | | | | 0 | 0 | 1 | 0 | 1 |
| Isolation | | | | 0 | 0 | 1 | 1 | 0 |
| Isolation | | | | 0 | 0 | 1 | 1 | 1 |
| TRXA4 | | | | 0 | 1 | 0 | 0 | 0 |
| TRXA3 | | | | 0 | 1 | 0 | 0 | 1 |
| TRXA2 | | | | 0 | 1 | 0 | 1 | 0 |
| TRXA1 | | | | 0 | 1 | 0 | 1 | 1 |
| TRXA4 | | | | 0 | 1 | 1 | 0 | 0 |
| TRXA3 | | | | 0 | 1 | 1 | 0 | 1 |
| TRXA2 | | | | 0 | 1 | 1 | 1 | 0 |
| TRXA1 | | | | 0 | 1 | 1 | 1 | 1 |
| TRXA4+3 | | | | 1 | 0 | 0 | 0 | 0 |
| TRXA4+2 | | | | 1 | 0 | 0 | 0 | 1 |
| TRXA4+1 | | | | 1 | 0 | 0 | 1 | 0 |
| TRXA3+2 | | | | 1 | 0 | 0 | 1 | 1 |
| TRXA3+1 | | | | 1 | 0 | 1 | 0 | 0 |
| TRXA2+1 | | | | 1 | 0 | 1 | 0 | 1 |
| All isolation | | | | 1 | 0 | 1 | 1 | 0 |
| All isolation | | | | 1 | 0 | 1 | 1 | 1 |
| All isolation | | | | 1 | 1 | 0 | 0 | 0 |
| All isolation | | | | 1 | 1 | 0 | 0 | 1 |
| All isolation | | | | 1 | 1 | 0 | 1 | 0 |
| All isolation | | | | 1 | 1 | 0 | 1 | 1 |
| All isolation | | | | 1 | 1 | 1 | 0 | 0 |
| All isolation | | | | 1 | 1 | 1 | 0 | 1 |
| All isolation | | | | 1 | 1 | 1 | 1 | 0 |
| All isolation | | | | 1 | 1 | 1 | 1 | 1 |

Evaluation Board Description

The SKY13550-667LF Evaluation Board is used to test the performance of the SKY13550-667LF DP8T Switch. An Evaluation Board schematic diagram is provided in Figure 6. A recommended ESD protection circuit diagram is provided in Figure 7. An assembly drawing for the Evaluation Board is shown in Figure 8.

Package Dimensions

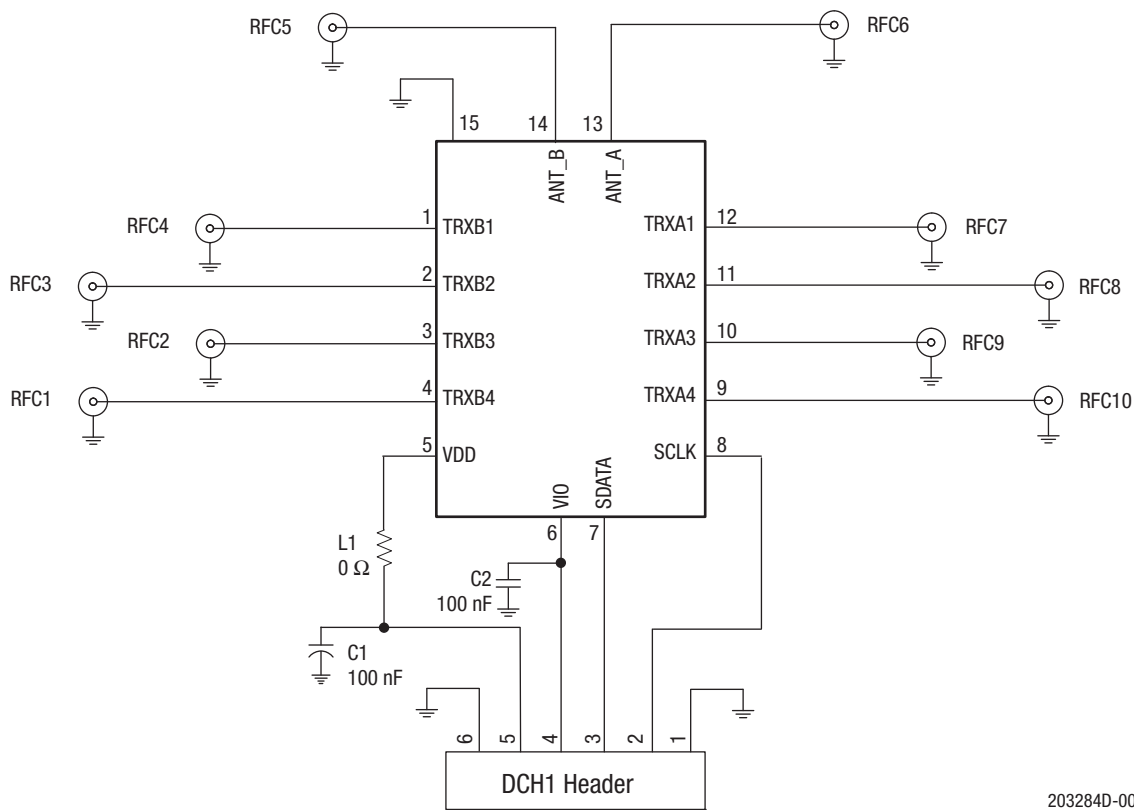
The PCB layout footprint for the SKY13550-667LF is provided in Figure 9. Typical part markings are shown in Figure 10. Package dimensions are shown in Figure 11, and tape and reel dimensions are provided in Figure 12.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

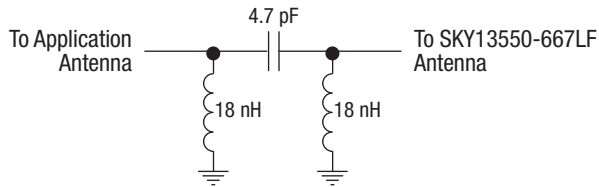
The SKY13550-667LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

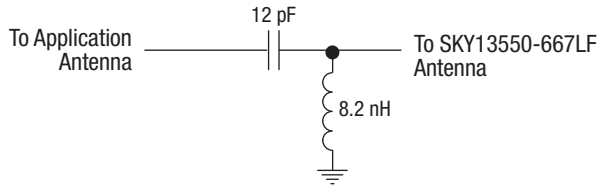


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Figure 6. SKY13550-667LF Evaluation Board Schematic



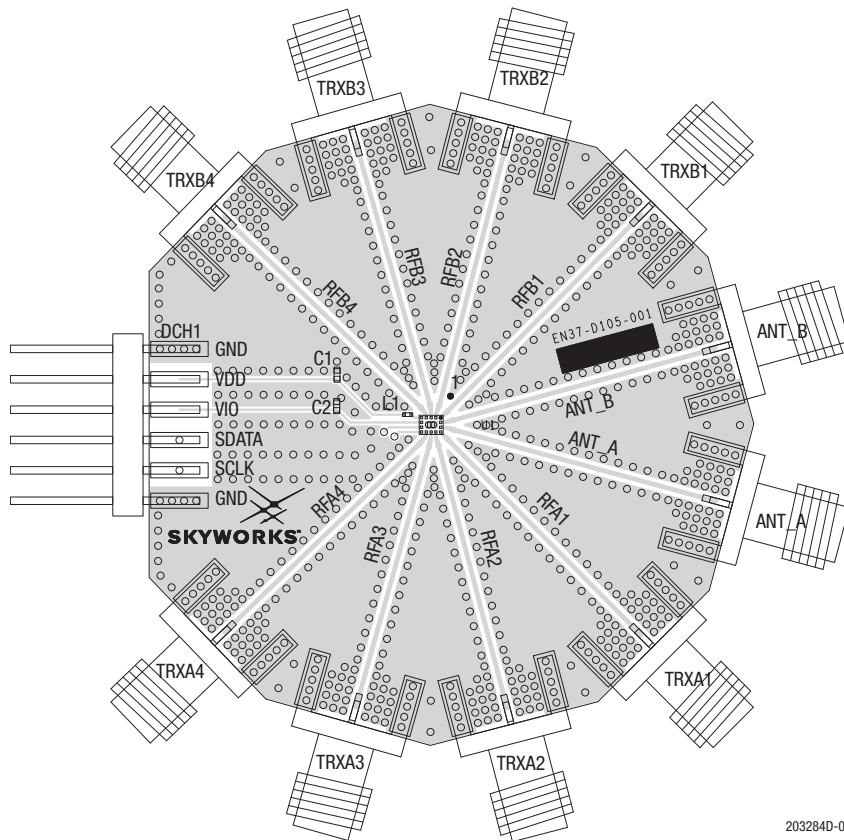
ESD Circuit 1



ESD Circuit 2

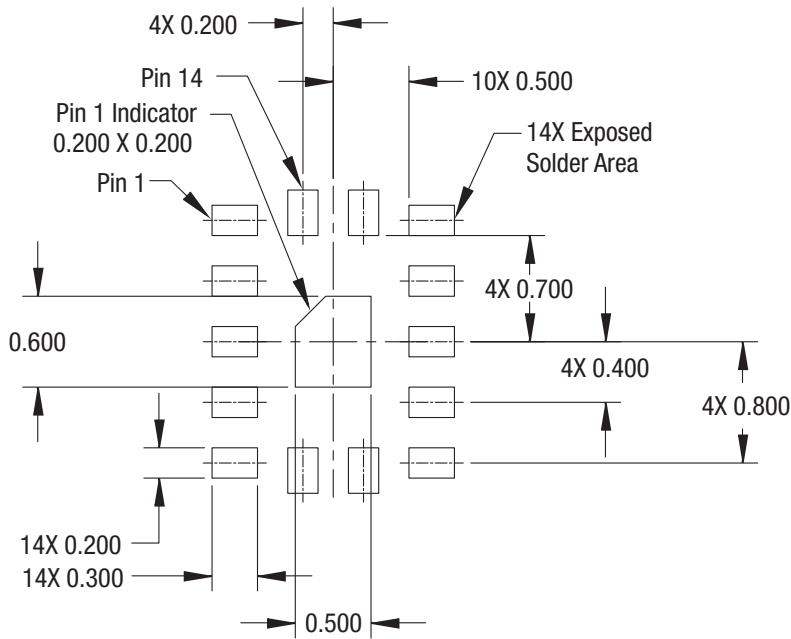
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Figure 7. SKY13550-667LF Recommended ESD Protection Circuits



203284D-008

Figure 8. SKY13550-667LF Evaluation Board Assembly Diagram



Dimensions are in millimeters

203284D-009

Figure 9. SKY13550-667LF PCB Layout Footprint (Top View)

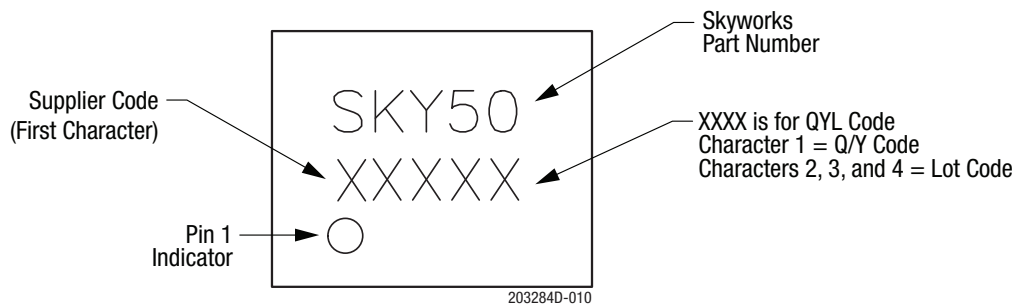


Figure 10. Typical Part Markings (Top View)

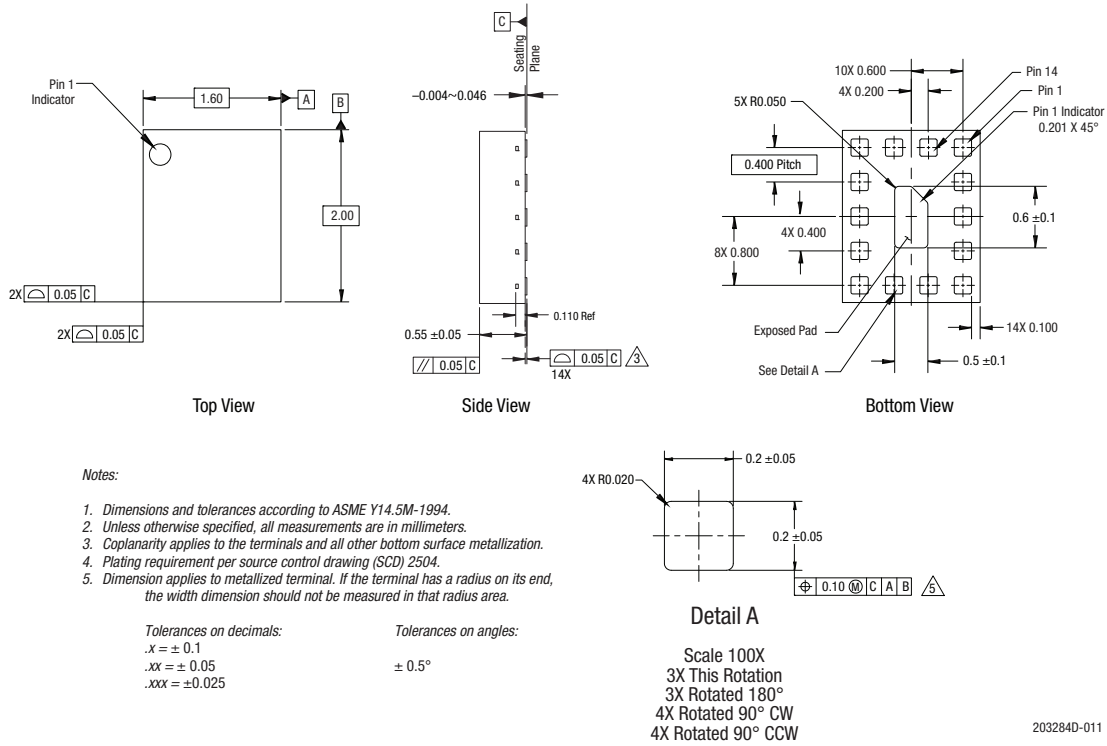


Figure 11. SKY13550-667LF Package Dimensions

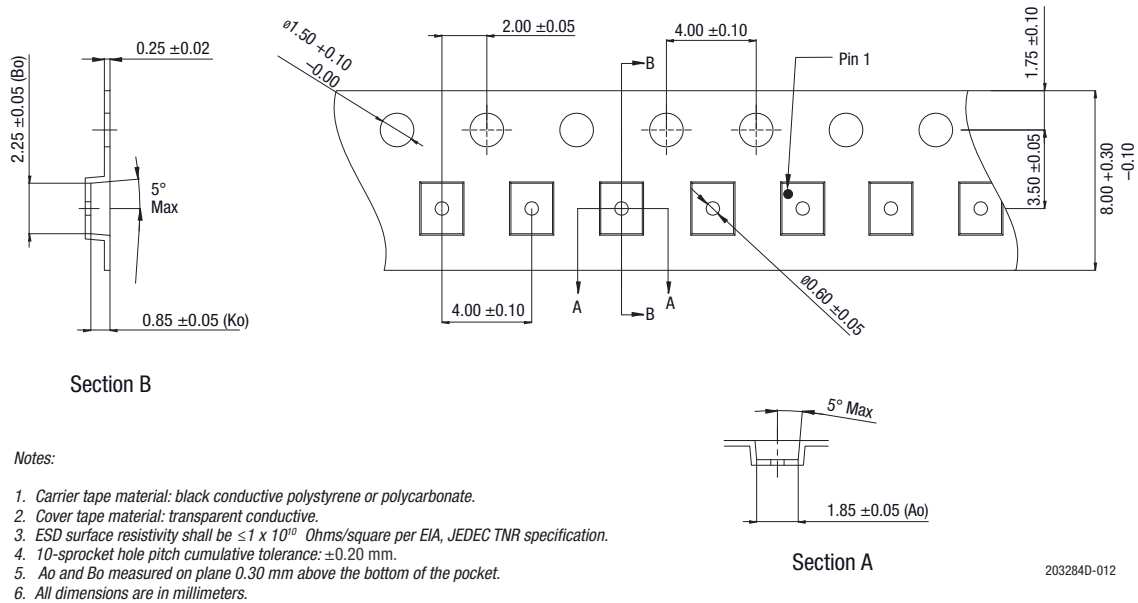


Figure 12. SKY13550-667LF Tape and Reel Dimensions

Ordering Information

| Model Name | Manufacturing Part Number | Evaluation Board Part Number |
|--|---------------------------|------------------------------|
| SKY13550-667LF: 0.4 to 3.8 GHz DP8T Switch | SKY13550-667LF | SKY13550-667LF-EVB |

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