GENERAL DESCRIPTION

The F2912 is a high reliability, low insertion loss, 50 Ω SP2T absorptive RF switch designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 9 kHz to 9000 MHz. In addition to providing low insertion loss, the F2912 also delivers excellent linearity and isolation performance while providing a 50 Ω termination to the unused RF input port.

The F2912 uses a single positive supply voltage of 3.3 V supporting three states using either 3.3 V or 1.8 V user-selectable control voltage. An added feature includes a Mode CTL pin allowing the user to control the device with either 1-pin or 2-pin control.

COMPETITIVE ADVANTAGE

The F2912 provides extremely low insertion loss; particularly important for RF receiver front-end use.

- ✓ Insertion Loss : 0.4 dB @ 1 GHz
- ✓ IIP3: +66 dBm
- ✓ RF1 to RF2 Isolation: 74 dB@ 1 GHz
- ✓ Negative supply voltage not required
- ✓ Extended temperature -55 °C to +125 °C

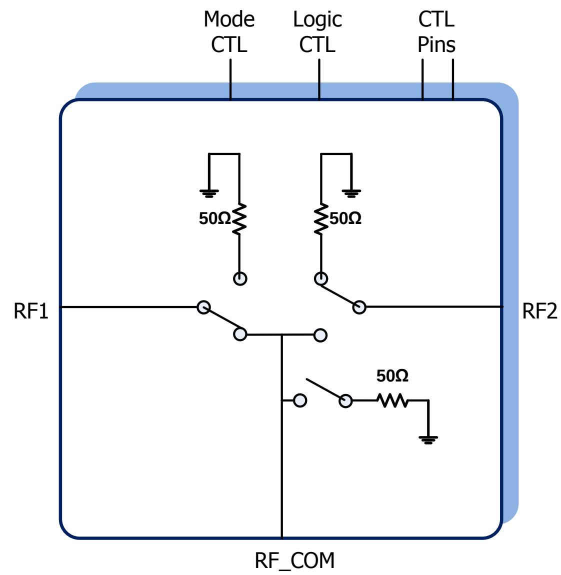
APPLICATIONS

- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID handheld and portable readers
- Cable Infrastructure
- Wireless LAN
- Test / ATE Equipment

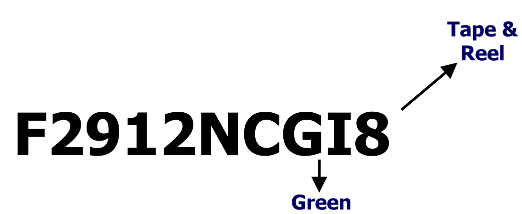
FEATURES

- Very low insertion loss: 0.4 dB @ 1GHz
- High Input IP3: +66 dBm
- RF1 to RF2 Isolation: 74 dB @ 1GHz
- 1-pin or 2-pin device control option
- Low DC current; 20 μA using 3.3 V logic
- Single positive supply voltage: 3.3 V
- 3.3 V or 1.8 V user-selectable control logic
- Operating temperature -55 °C to +125 °C
- 4 mm x 4 mm 20 pin TQFN package

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
VCC to GND	V_{CC}	-0.3	+3.9	V
CTL1, CTL2, LogicCTL	V_{CNTL}	-0.3	V_{cc} + 0.3	V
RF1, RF2, RF_Com	V_{RF}	-0.3	+0.3	V
Maximum Junction Temperature	T_{Jmax}		+140	°C
Storage Temperature Range	T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		Class 2 (2000)	V
ElectroStatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		Class IV (1500)	V

RF Power For Case Temperatures up to +85 °C*

RF1, RF2 (RF1 or RF2 is connected to RF_COM, State 3 and 2)	+33 dBm
RF1, RF2 (RF1 or RF2 is NOT connected to RF_COM, State 1, 2 and 3)	+24 dBm
RF_COM (RF_COM port is NOT connected to RF1 or RF2, State 1)	+24 dBm

RF Power For Case Temperatures up to +105 °C*

RF1, RF2 (RF1 or RF2 is connected to RF_COM, State 3 and 2)	+33 dBm
RF1, RF2 (RF1 or RF2 is NOT connected to RF_COM, State 1, 2 and 3)	+21 dBm
RF_COM (RF_COM port is NOT connected to RF1 or RF2, State 1)	+21 dBm

RF Power For Case Temperatures up to +120 °C*

RF1, RF2 (RF1 or RF2 is connected to RF_COM, State 3 and 2)	+27 dBm
RF1, RF2 (RF1 or RF2 is NOT connected to RF_COM, State 1, 2 and 3)	+18 dBm
RF_COM (RF_COM port is NOT connected to RF1 or RF2, State 1)	+18 dBm

* Note: These Absolute Maximum RF power limits are reduced if the RF frequency is lower than 400 MHz.

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ_{JA} (Junction – Ambient)	60.0 °C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	3.9 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL 1

F2912 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CC}	Using 3.3 V logic (Pin 18 low)	2.7		3.6	V
		Using 1.8 V logic (Pin 18 high)	3.15		3.45	
Operating Temperature Range	T_{CASE}	Case Temperature	-55		+125	^{o}C
RF Frequency Range	F_{RF}		0.009		9000	MHz
RF1 Port Impedance	Z_{RF1}			50		Ω
RF2 Port Impedance	Z_{RF2}			50		
RF_COM Port Impedance	Z_{RF_COM}			50		

F2912 SPECIFICATION

Typical Application Circuit, V_{CC} = +3.3 V, T_C = +25 °C, F_{RF} = 1 GHz, 2 GHz, and or 4 GHz as noted below. Input power = 0 dBm or +13 dBm/tone unless otherwise stated. PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Input High Threshold	V_{IH}	For all control pins Pin 18 low for 3.3 V logic	***0.7 x V_{CC}***		***3.6***	V
		For all control pins Pin 18 high for 1.8 V logic	***1.1*** [1]		***2***	
Logic Input Low Threshold	V_{IL}	For all control pins Pin 18 low for 3.3 V logic			***0.3 x V_{CC}***	V
		For all control pins Pin 18 high for 1.8 V logic			***0.63***	V
Logic Current	I_{IH}, I_{IL}	For all control pins		180	***500***	nA
DC Current	I_{CC}	Pin 18 low for 3.3 V logic		20	***25***	µA
		Pin 18 high for 1.8 V logic		126	***153***	
Insertion Loss RF1/RF2 to RF_COM (State 2 or 3)	IL	RF = 1.0 GHz		0.4	***0.6***	dB
		RF = 2.0 GHz		0.5	***0.7***	
		RF = 4.0 GHz		0.6	***0.8***	
		RF = 6.0 GHz		0.61	0.9 [2]	
		RF = 8.1 GHz		0.81	1.0	
		RF = 9.0 GHz		1.00	1.4	
Isolation RF1 / RF2 to RF_COM (State 2 or 3)	ISO_1	RF = 1.0 GHz	***58***	61.5		dB
		RF = 2.0 GHz	***52***	57		
		RF = 4.0 GHz	50	52		
		RF = 6.0 GHz	45	53		
		RF = 8.1 GHz	30	33		
		RF = 9.0 GHz	26	29		
Isolation RF1 to RF2 (State 2 or 3)	ISO_2	RF = 1.0 GHz	71	74		dB
		RF = 2.0 GHz	60	62		
		RF = 4.0 GHz	46	47		
		RF = 6.0 GHz	36	38		
		RF = 8.1 GHz	27	31		
		RF = 9.0 GHz	23	27		
Return Loss RF_COM (State 1)	RL_1	RF = 1.0 GHz		27		dB
		RF = 2.0 GHz		24		
		RF = 4.0 GHz		20		
		RF = 6.0 GHz		12		
		RF = 8.1 GHz		11		
		RF = 9.0 GHz		9		

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: The input 1 dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power.
Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.

F2912 SPECIFICATION (CONT.)

Typical Application Circuit, V_{CC} = +3.3 V, T_C = +25 °C, F_{RF} = 1 GHz, 2 GHz, and or 4 GHz as noted below. Input power = 0 dBm or +13 dBm/tone unless otherwise stated. PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Return Loss RF_COM (State 2 or 3)	RL_2	RF = 1.0 GHz		25		dB
		RF = 2.0 GHz		23		
		RF = 4.0 GHz		26		
		RF = 6.0 GHz		18		
		RF = 8.1 GHz		20		
		RF = 9.0 GHz		15		
Return Loss RF1, RF2 (State 1)	RL_3	RF = 1.0 GHz		27		dB
		RF = 2.0 GHz		27		
		RF = 4.0 GHz		20		
		RF = 6.0 GHz		18		
		RF = 8.1 GHz		14		
		RF = 9.0 GHz		10		
Return Loss RF1, RF2 (State 2 or 3)	RL_4	RF = 1.0 GHz		26		dB
		RF = 2.0 GHz		25		
		RF = 4.0 GHz		21		
		RF = 6.0 GHz		17		
		RF = 8.1 GHz		14		
		RF = 9.0 GHz		10		
Input IP2 RF1 / RF2 (State 2 or 3)	IIP2	RF = 1.0 GHz		102		dBm
		RF = 2.0 GHz		110		
		RF = 3.0 GHz		110		
Input IP3 RF1 / RF2 (State 2 or 3)	IIP3	RF = 1.0 GHz		66		dBm
		RF = 2.0 GHz		64		
		RF = 3.0 GHz		64		
Input 1dB compression RF1 / RF2 (State 2 or 3) [3]	IP1dB	F_{RF} = 2.0 GHz	29	30		dBm
Switching Time	T_{SW}	RF = 1.0 GHz 50% control to 90% RF		1.1		µs
		RF = 1 GHz 50% control to 10% RF		0.5		
Maximum Switching Frequency	SW_{FREQ}			25		kHz
Maximum video feed-through RF_COM port	VIDFT	5 MHz to 1 GHz Measured with 2.5 ns risetime, 0 to 3.3 V control pulse		5		mV_{pp}
Maximum spurious level on any RF port [4]	$Spur_{MAX}$	RF ports terminated into 50 Ω		-145		dBm

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: The input 1 dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power.
Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.

CONTROL MODES

The F2912 switch states are designed to be controlled by using either a 2 pin logic control (see Table 1) or a 1 pin logic control (see Table 2). Table 3 describes the settings to enable one or two pin control. The F2912 also has the ability to be controlled by 3 V or 1.8 V control logic based on the setting of Pin 18 (See Table 4). See Pin Compatibility in the Applications Information section for more details.

Table 1 - Switch Control Truth Table for 2 pin logic control (ModeCTL = GND)

State	Control pin input		RF1, RF2 Input / Output	
	CTL1 (Pin 17)	CTL2 (Pin 16)	RF1 to RF Com	RF2 to RF Com
1	Low	Low	OFF	OFF
2	Low	High	OFF	ON
3	High	Low	ON	OFF
4	High	High	N/A	N/A

Table 2 – Switch Control Truth Table for 1 pin logic control (ModeCTL = VCC)

State	Control Pin Input		RF1, RF2 Input / Output	
	CTL1 (Pin 17)	CTL2 (Pin 16)	RF1 to RF Com	RF2 to RF Com
2	Don't Care	High	OFF	ON
3	Don't Care	Low	ON	OFF

Table 3 – Mode Control Truth Table to set for 1 or 2 pin logic control

ModeCTL (Pin 19)	Pin Control Mode
GND	2-pin control: CTL1 and CTL2
V_{CC}	1-pin control: CTL2

Notes:

1. When RF1 and RF2 ports are both open (State 1), all 3 RF ports are terminated to an internal 50 Ω termination resistor.
2. When RF1 or RF2 port is open (State 2 or State 3 OFF condition), the open port is connected to an internal 50 Ω termination resistor.
3. When RF1 or RF2 port is closed (State 2 or State 3 ON condition), the closed port is connected to the RF Com port.

Table 4 - Logic Control (pin 18) Truth Table

LogicCTL (Pin 18)	Logic Voltage
V_{CC}	1.8 V
GND	3.3 V

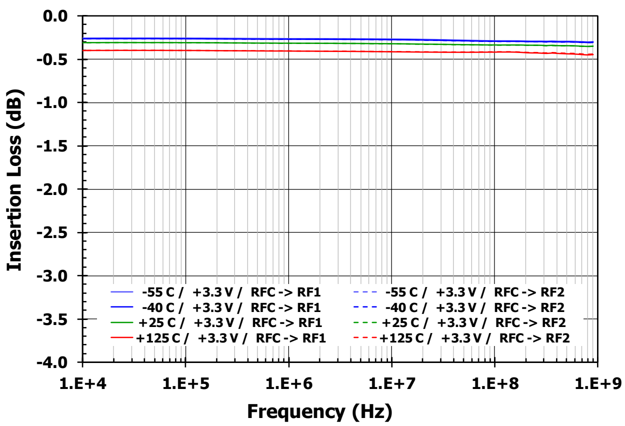
TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

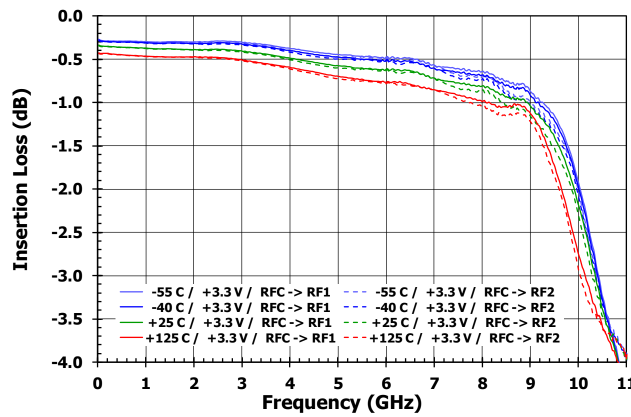
1. **EVKit connector and trace losses de-embedded**
2. **V_{cc} = 3.3 V**
3. **T_{AMB} = 25 °C**
4. **Small signal parameters measured with P_{IN} = 0 dBm.**
5. **Two tone tests P_{IN} =+13 dBm/tone with 50 MHz tone spacing for F_{RF} > 500 MHz.**
6. **Z_S= Z_L = 50 Ω**

TYPICAL OPERATING CONDITIONS (- 1 -)

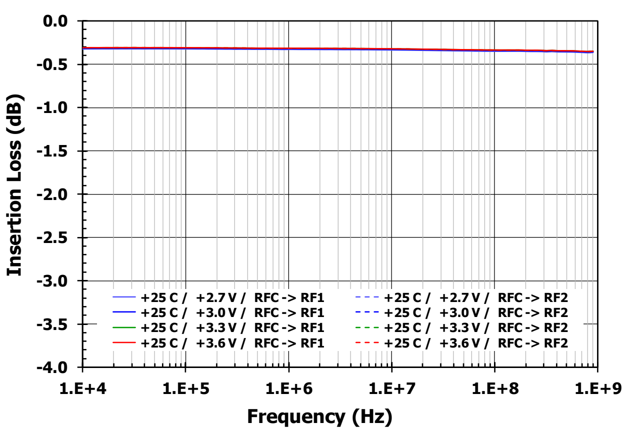
Insertion Loss vs. Temperature



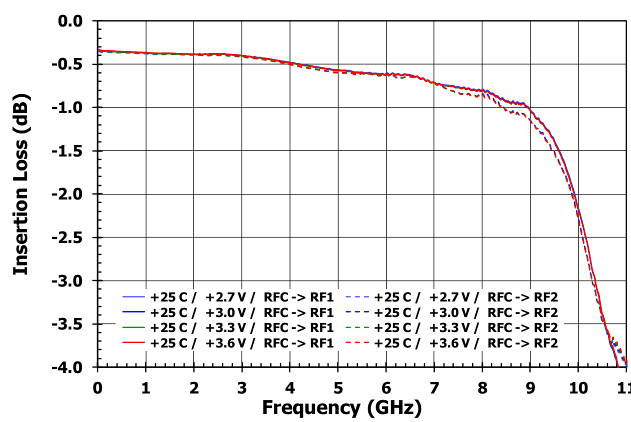
Insertion Loss vs. Temperature



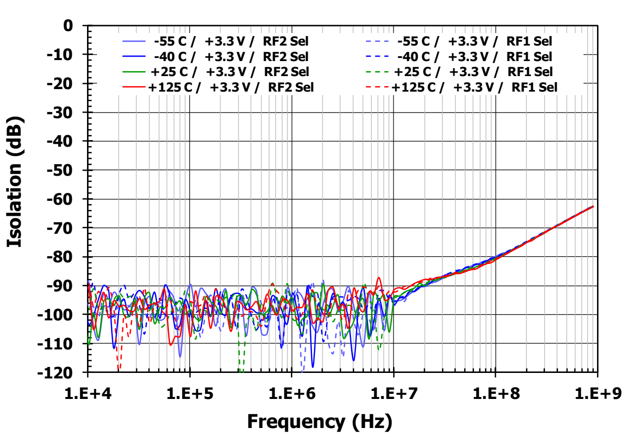
Insertion Loss vs. Voltage



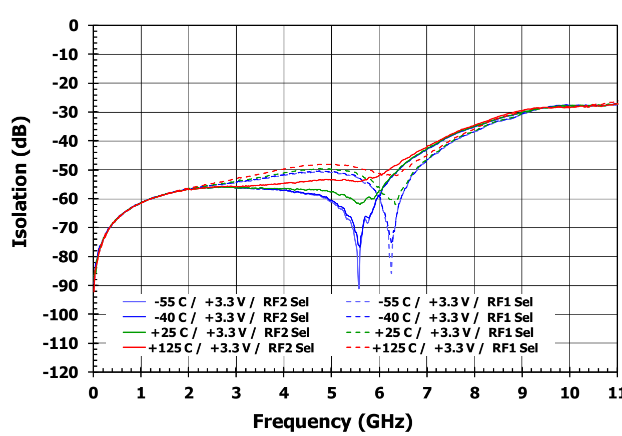
Insertion Loss vs. Voltage



Isolation vs. Temperature [RFC → RF1 / RF2]

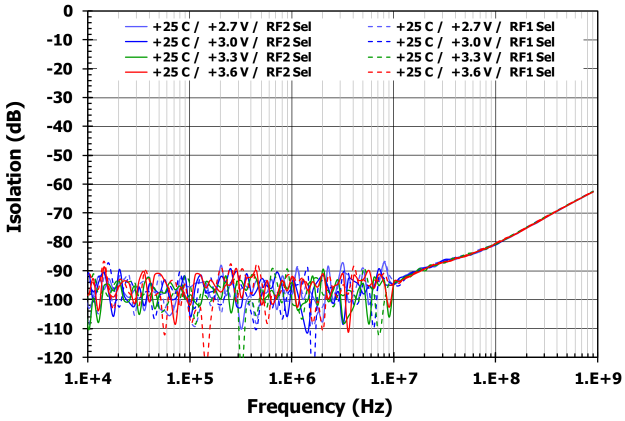


Isolation vs. Temperature [RFC → RF1 / RF2]

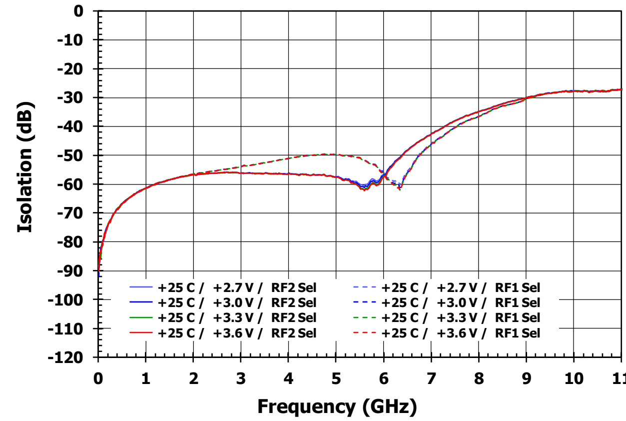


TYPICAL OPERATING CONDITIONS (- 2 -)

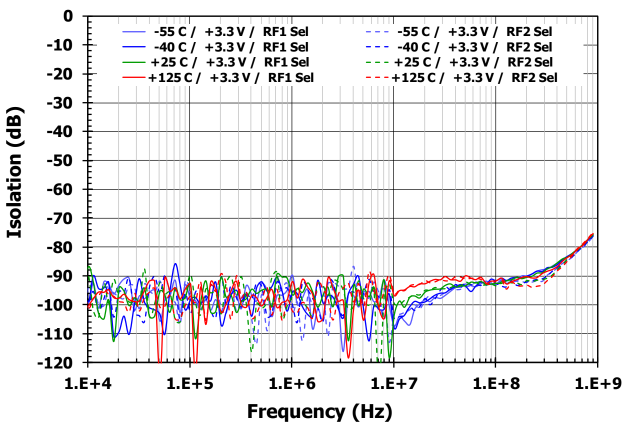
Isolation vs. Voltage [RFC → RF1 / RF2]



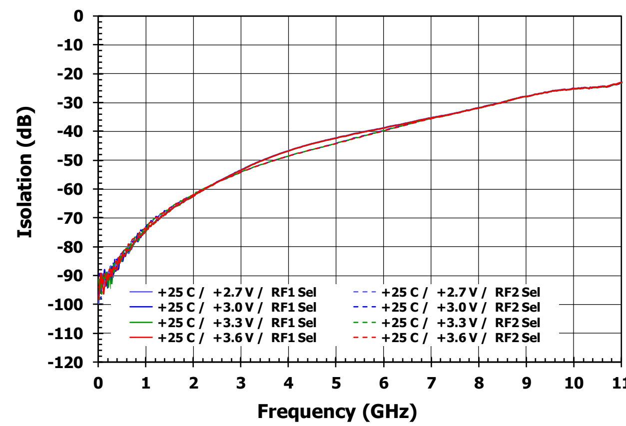
Isolation vs. Voltage [RFC → RF1 / RF2]



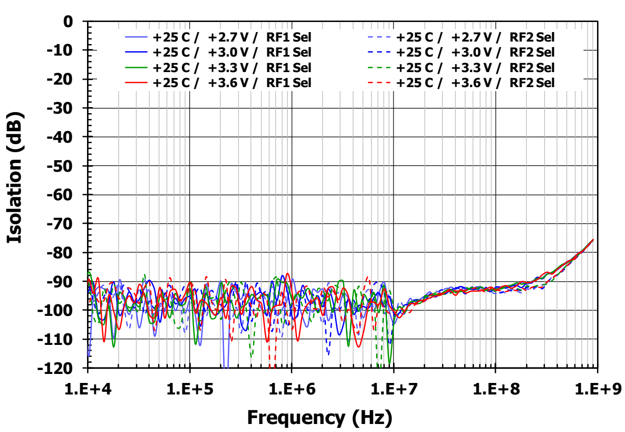
Isolation vs. Temperature [RF1 → RF2]



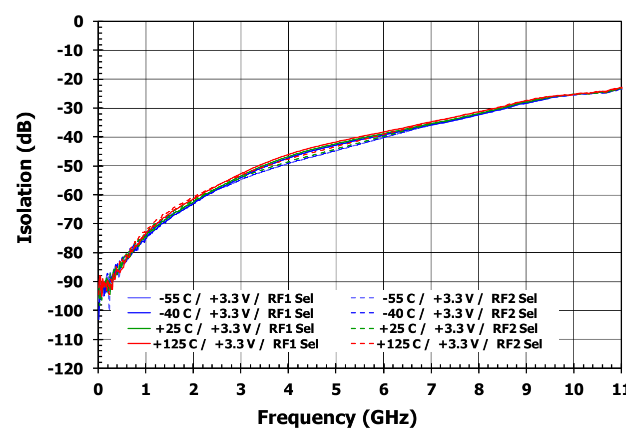
Isolation vs. Temperature [RF1 → RF2]



Isolation vs. Voltage [RF1 → RF2]

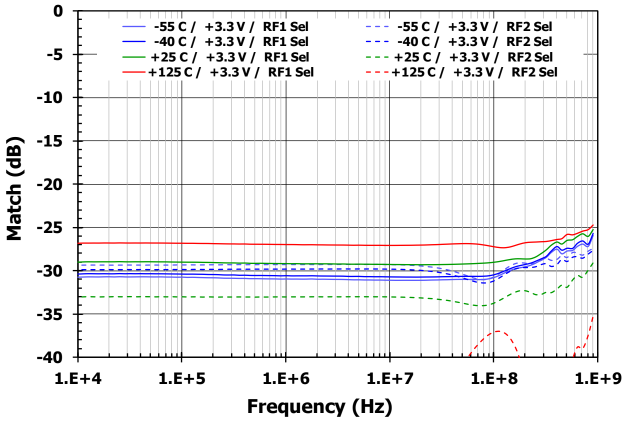


Isolation vs. Voltage [RF1 → RF2]

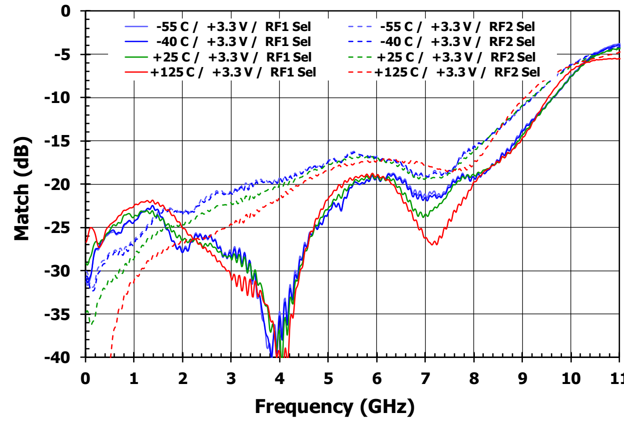


TYPICAL OPERATING CONDITIONS (- 3 -)

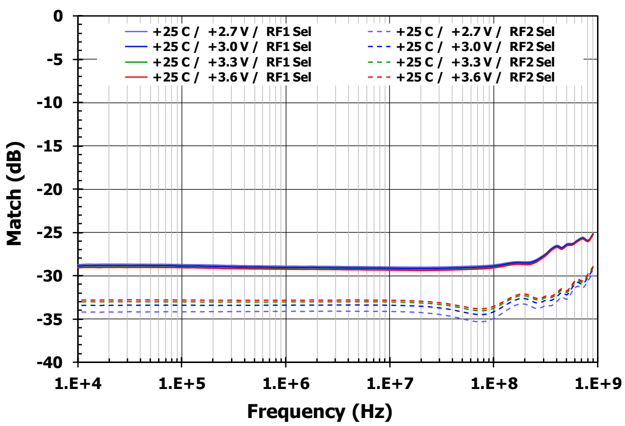
RF1 Return Loss vs. Temperature



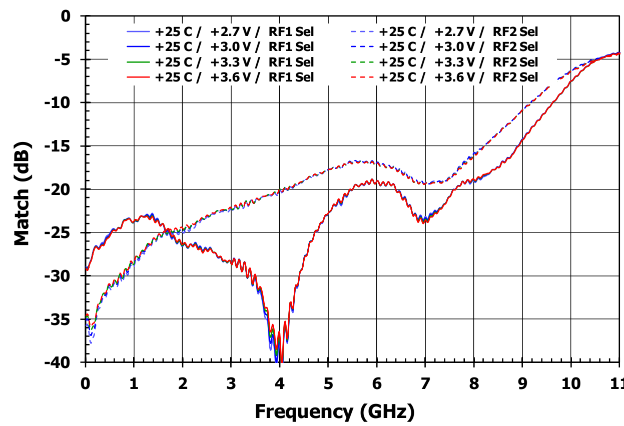
RF1 Return Loss vs. Temperature



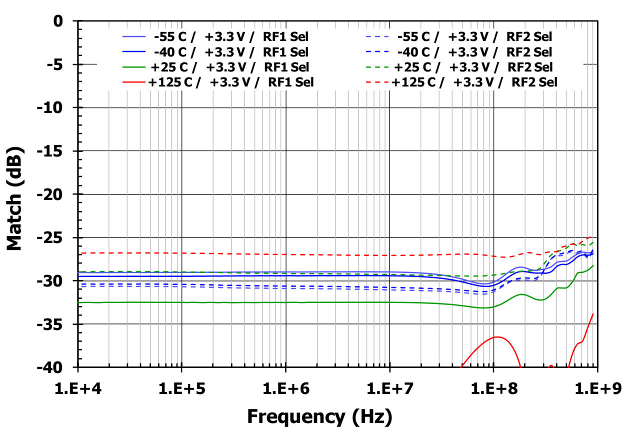
RF1 Return Loss vs. Voltage



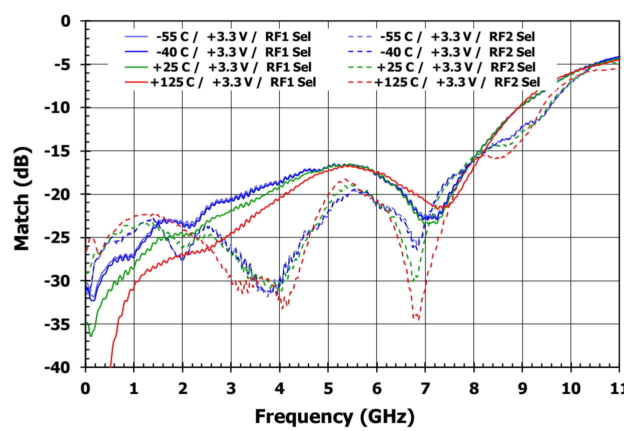
RF1 Return Loss vs. Voltage



RF2 Return Loss vs. Temperature

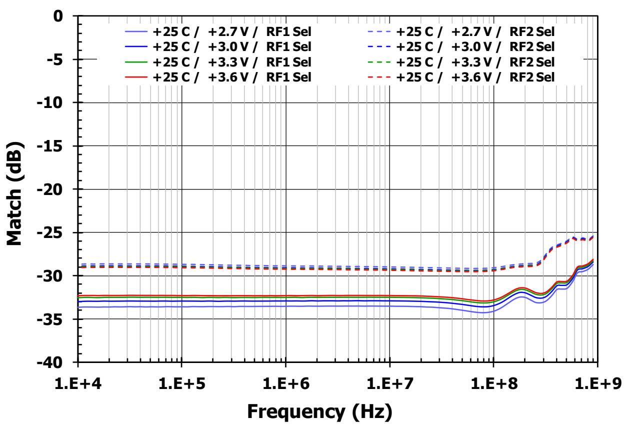


RF2 Return Loss vs. Temperature

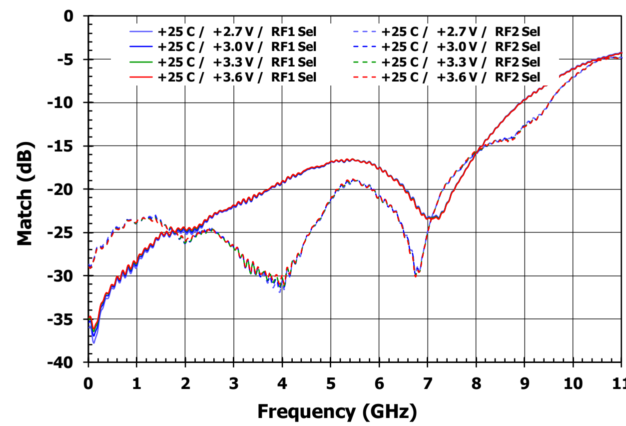


TYPICAL OPERATING CONDITIONS (- 4 -)

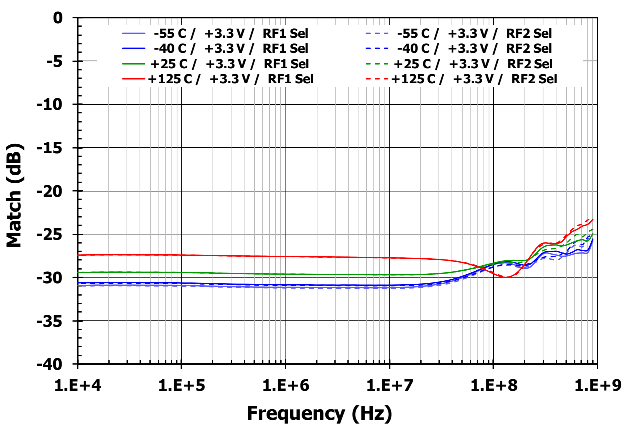
RF2 Return Loss vs. Voltage



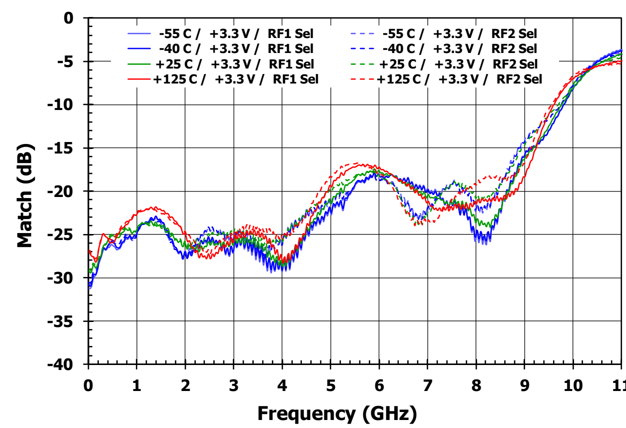
RF2 Return Loss vs. Voltage



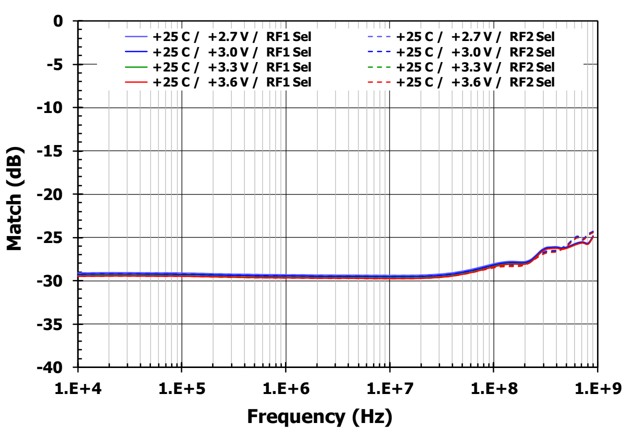
RFC Return Loss vs. Temperature



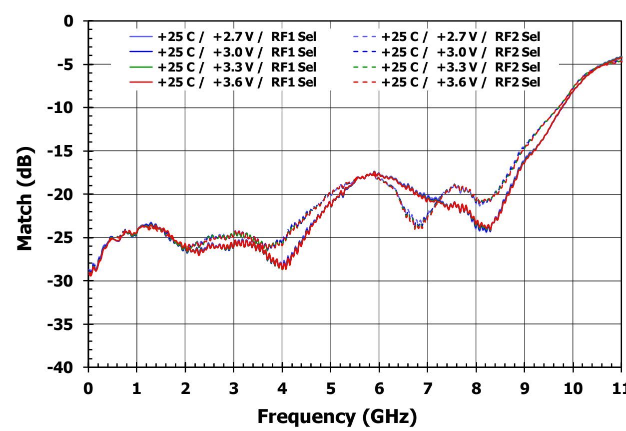
RFC Return Loss vs. Temperature



RFC Return Loss vs. Voltage

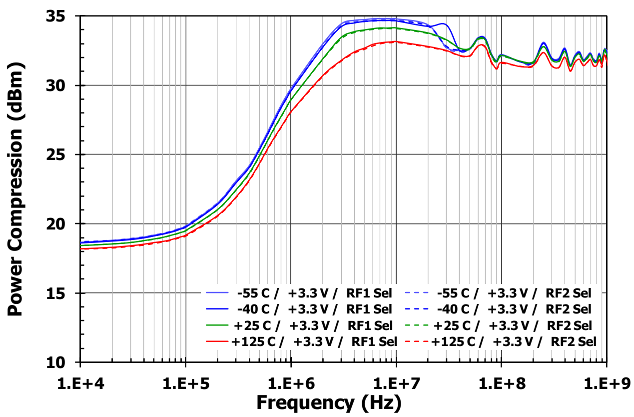


RFC Return Loss vs. Voltage

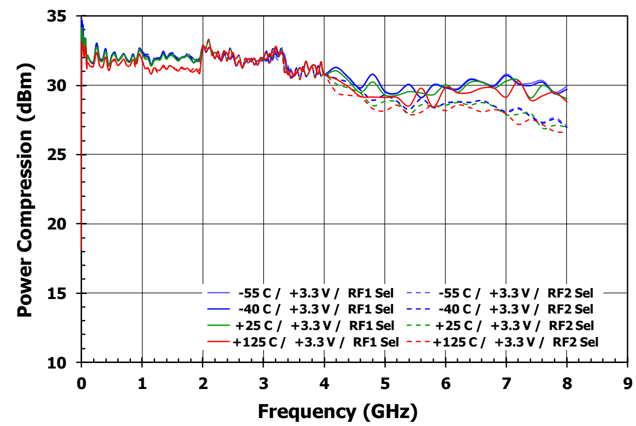


TYPICAL OPERATING CONDITIONS (- 5 -)

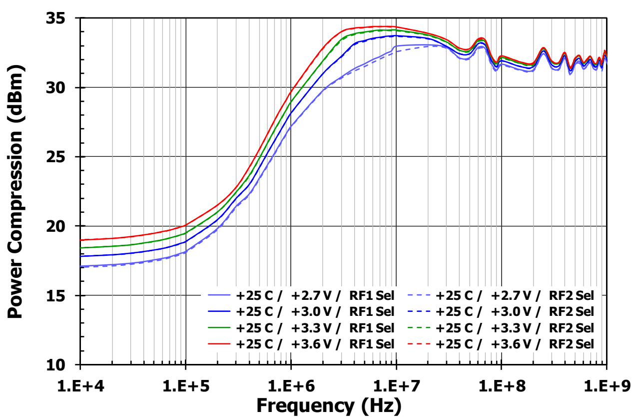
Input Power Compression vs. Temperature



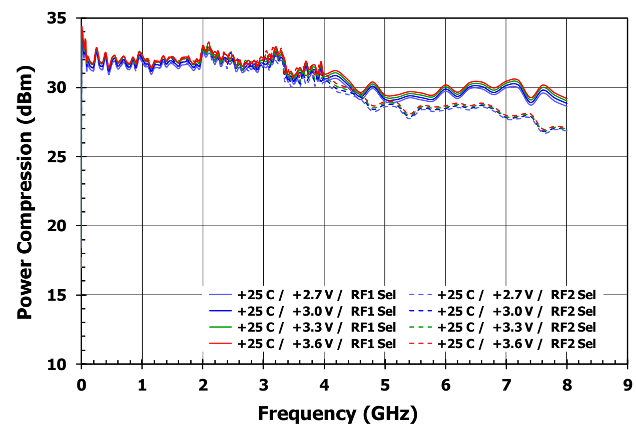
Input Power Compression vs. Temperature



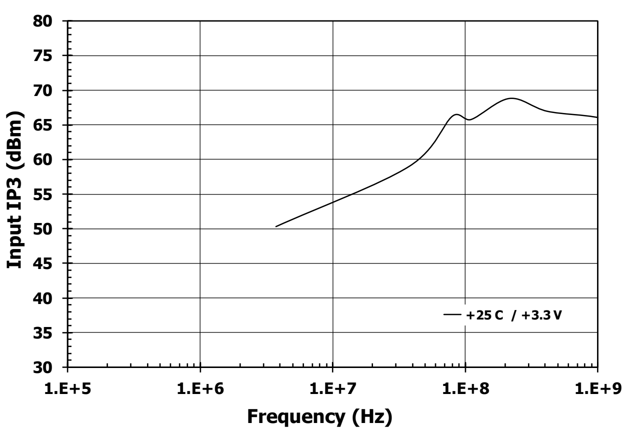
Input Power Compression vs. Voltage



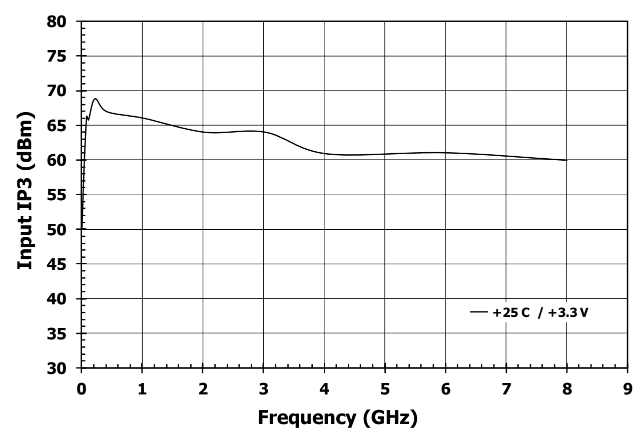
Input Power Compression vs. Voltage



Input IP3

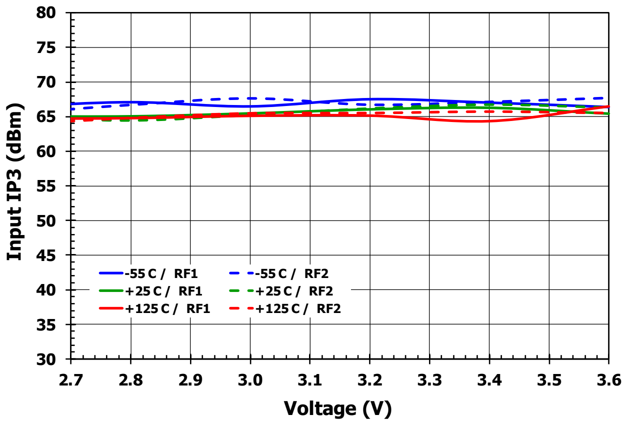


Input IP3

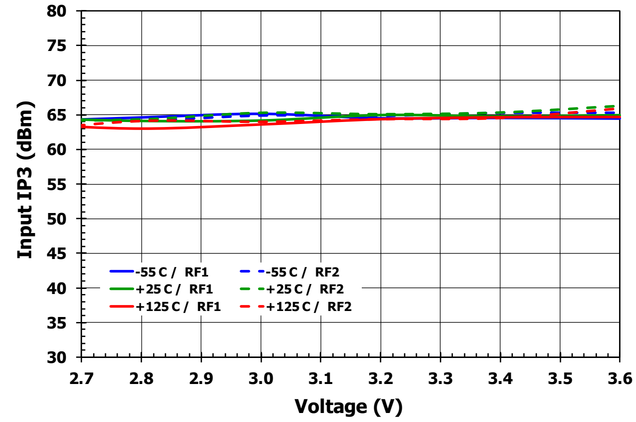


TYPICAL OPERATING CONDITIONS (- 6 -)

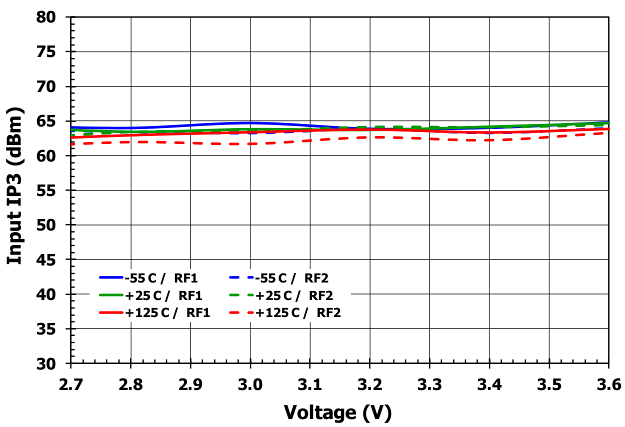
Input IP3 [2 GHz]



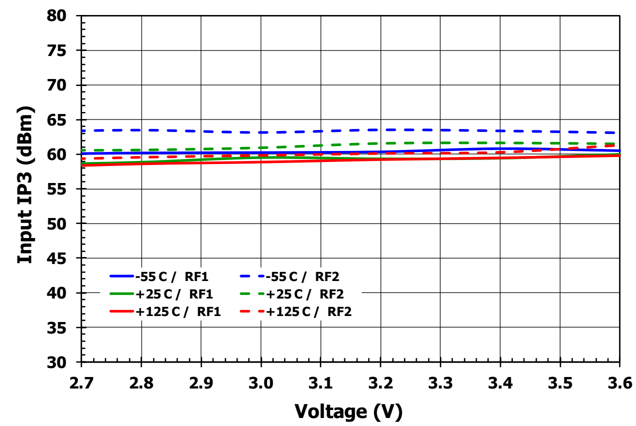
Input IP3 [3 GHz]



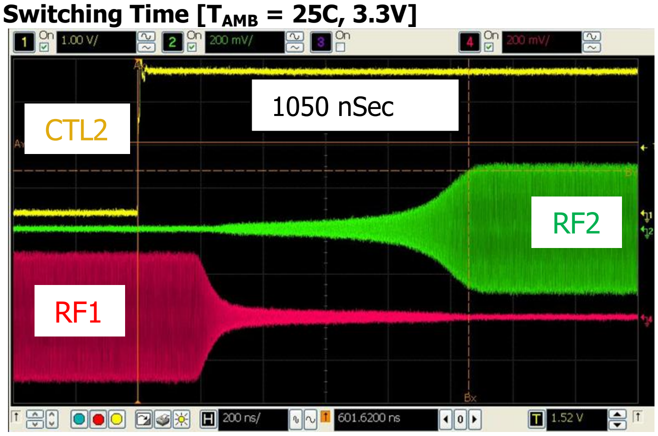
Input IP3 [4 GHz]



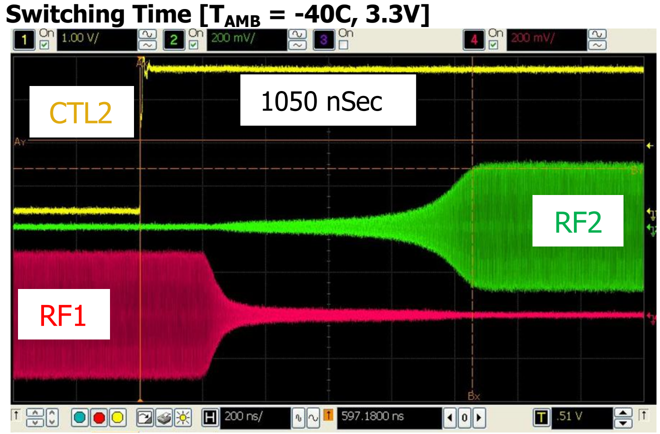
Input IP3 [6 GHz]



Switching Time [T_{AMB} = 25C, 3.3V]

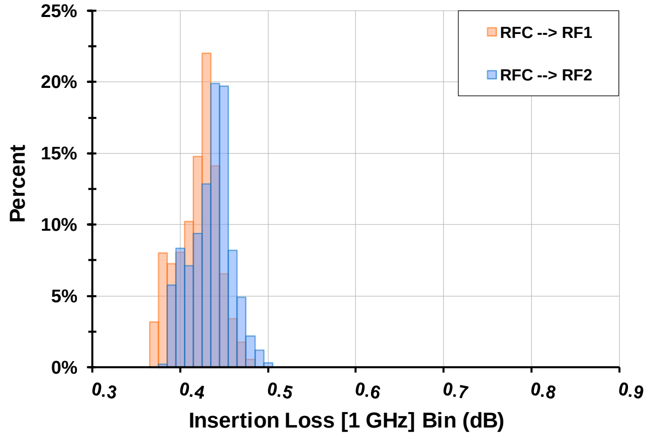


Switching Time [T_{AMB} = -40C, 3.3V]

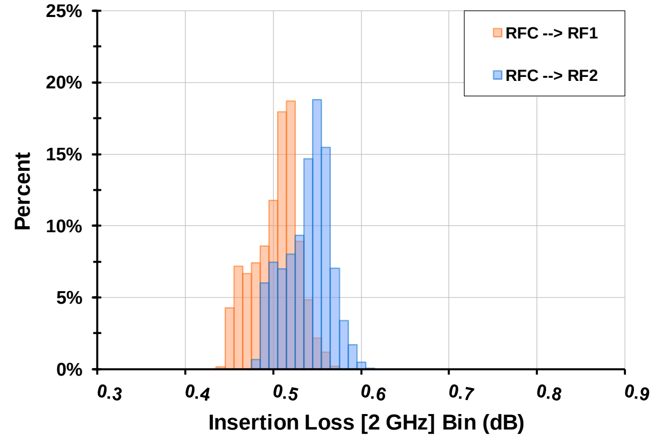


TYPICAL OPERATING CONDITIONS HISTOGRAMS [N=4800, T_{CASE}= 25C] (-4-)

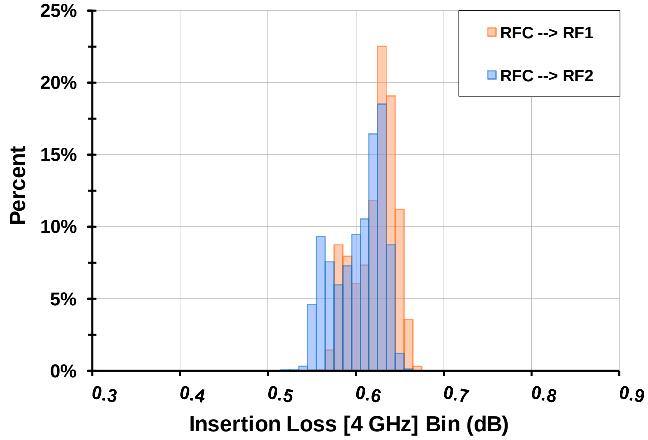
Insertion Loss [RF = 1 GHz]



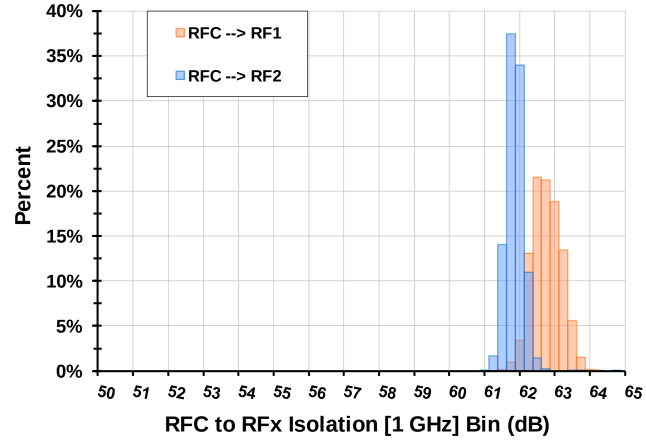
Insertion Loss [RF = 2 GHz]



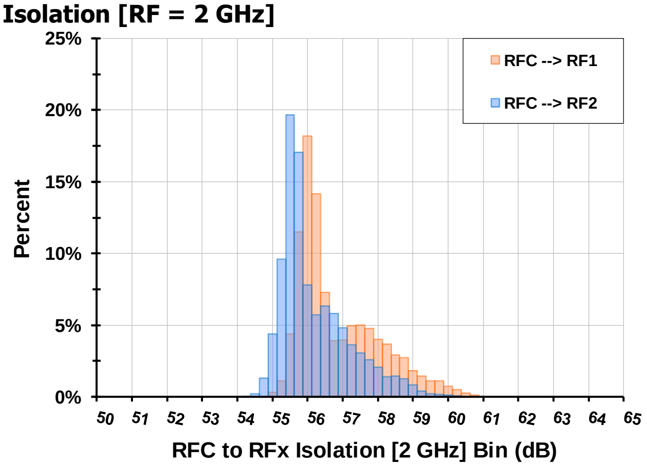
Insertion Loss [RF = 4 GHz]



Isolation [RF = 1 GHz]

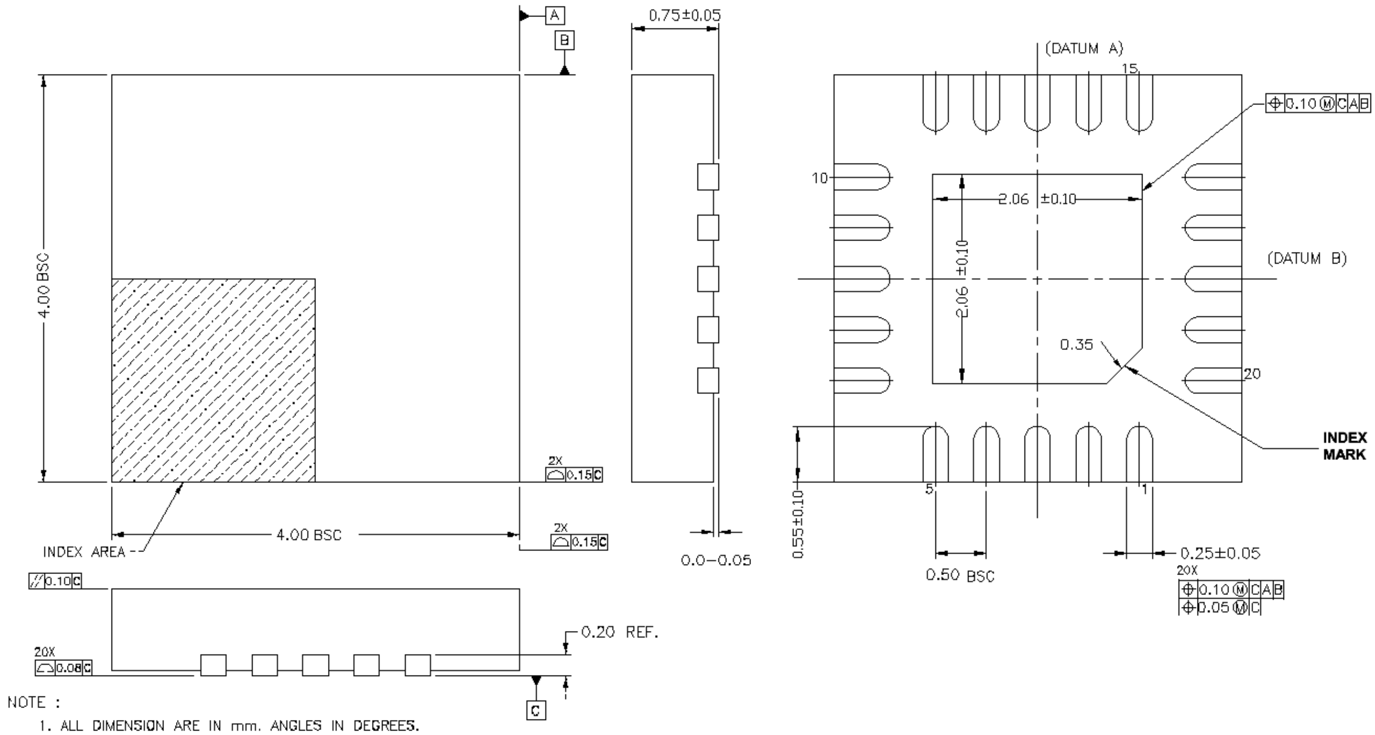


Isolation [RF = 2 GHz]



Package Drawing

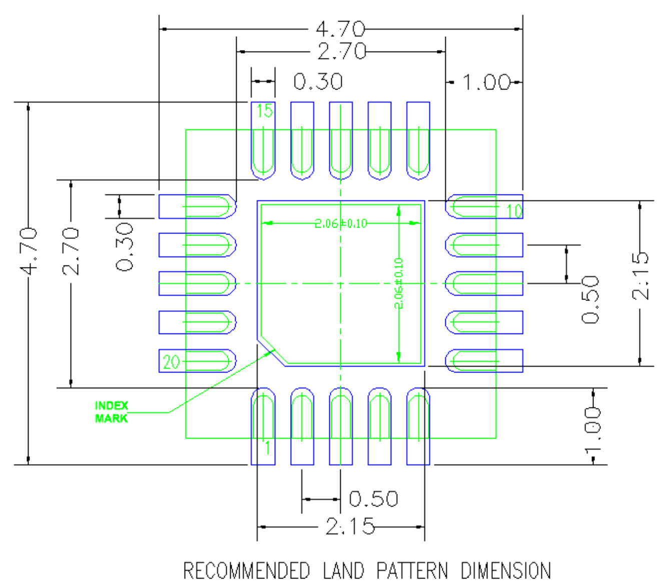
(4 mm x 4 mm 20-pin TQFN), NCG20



NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. REFER JEDEC MO-220.

Land Pattern Dimension

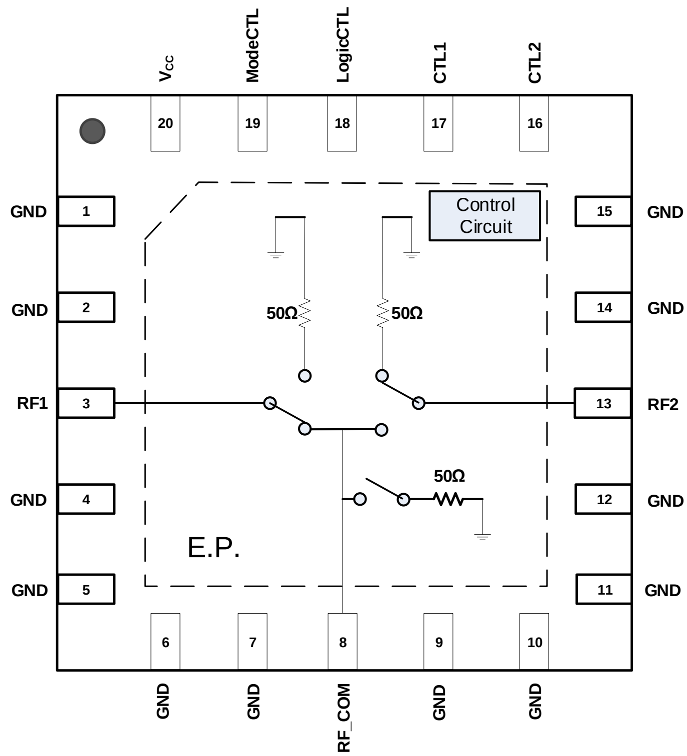


RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

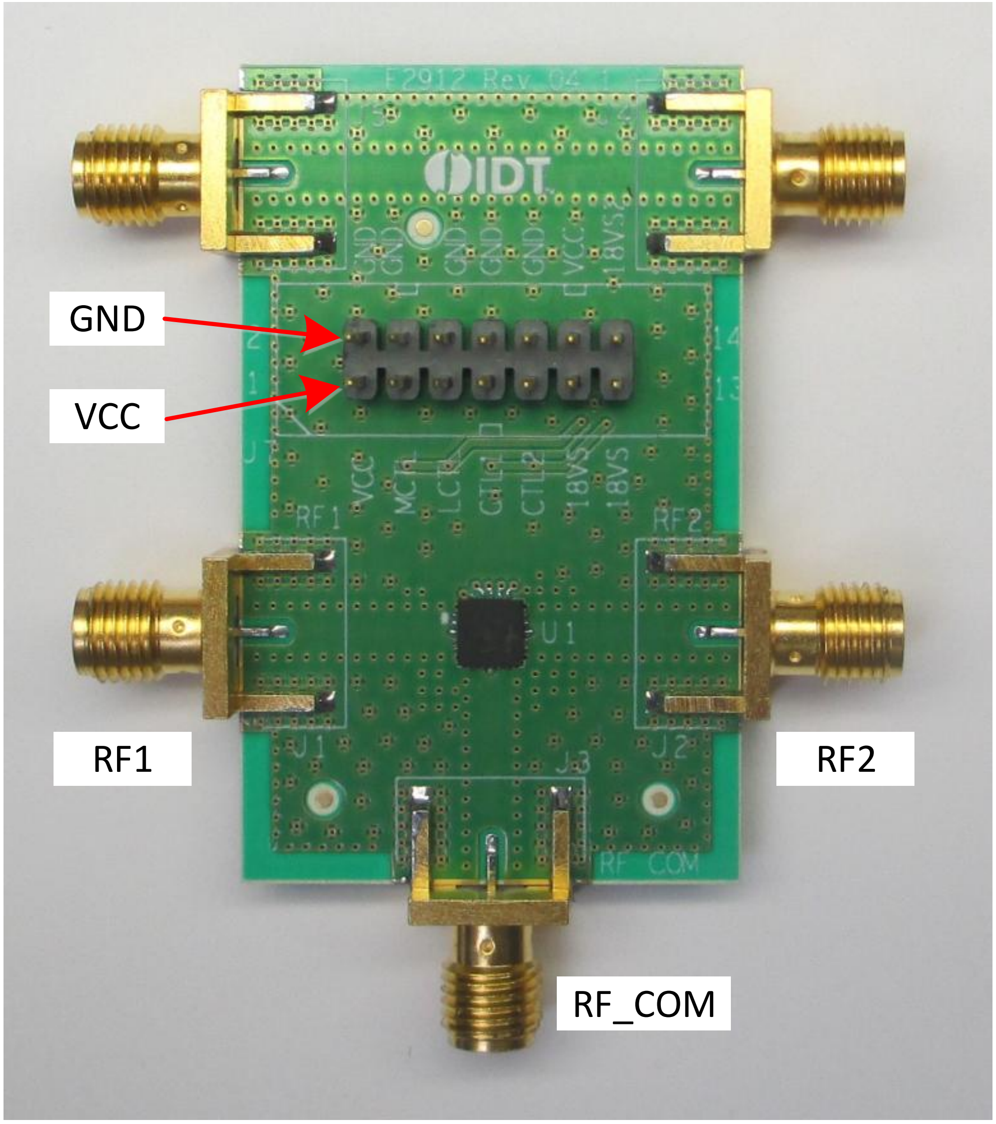
PIN DIAGRAM



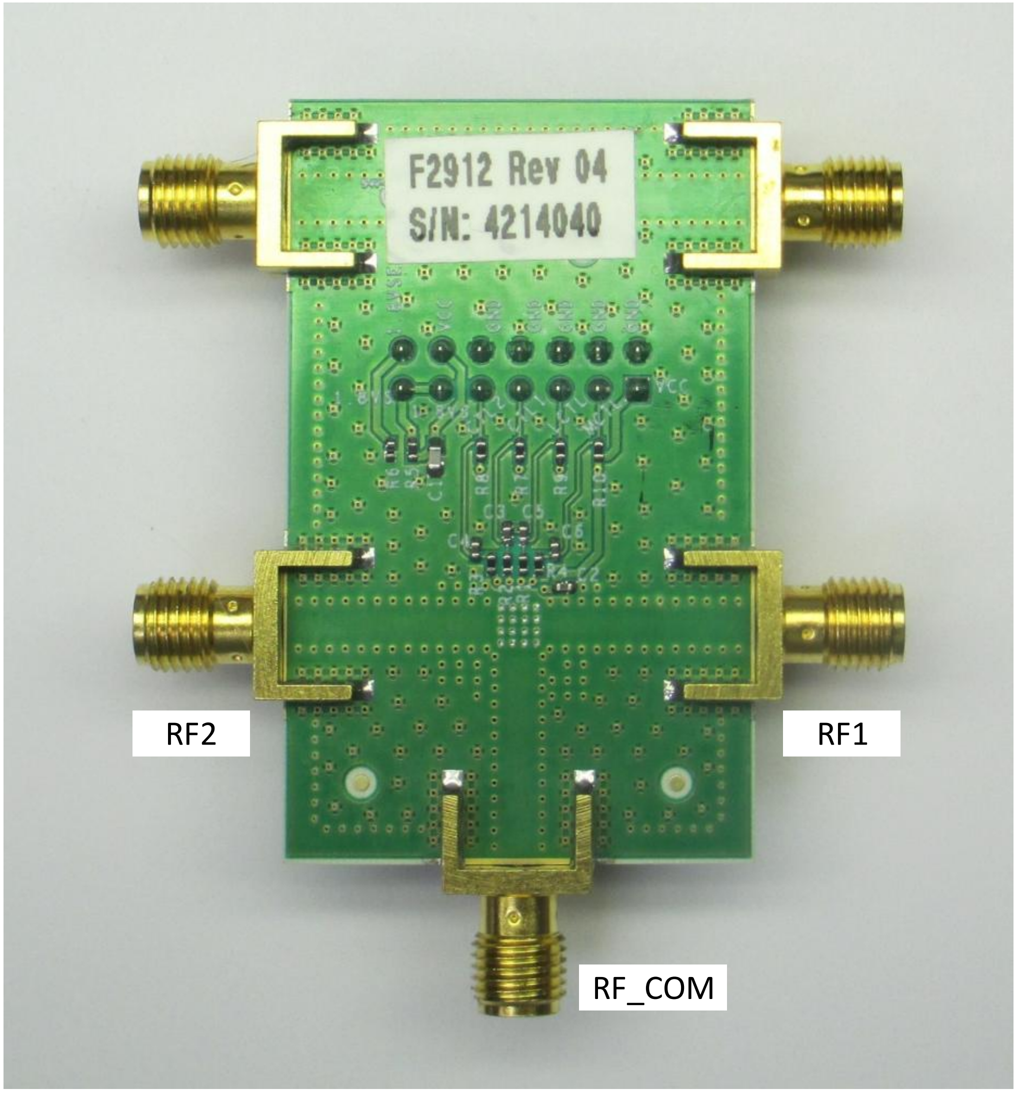
PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15	GND	Ground these pins as close to the device as possible.
3	RF1	RF1 Port. Matched to 50 Ω. If this pin is not 0 V DC, then an external coupling capacitor must be used.
8	RF_COM	RF Common Port. Matched to 50 Ω. If this pin is not 0 V DC, then an external coupling capacitor must be used.
13	RF2	RF2 Port. Matched to 50 Ω. If this pin is not 0 V DC, then an external coupling capacitor must be used.
16	CTL2	Control 2 – See Table 1 and Table 2 Switch Control Truth Tables for proper logic setting.
17	CTL1	Control 1 – See Table 1 and Table 2 Switch Control Truth Tables for proper logic setting.
18	LogicCTL	Logic Control – See Table 4 Logic Control Truth Table. Apply V_{CC} to select 1.8 V logic control or GND for 3.3 V logic control.
19	ModeCTL	Mode Control – See Table 3 Mode Control Truth Table. Apply V_{CC} to select 1-pin control or GND for 2-pin control.
20	V_{CC}	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
21	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the specified RF performance.

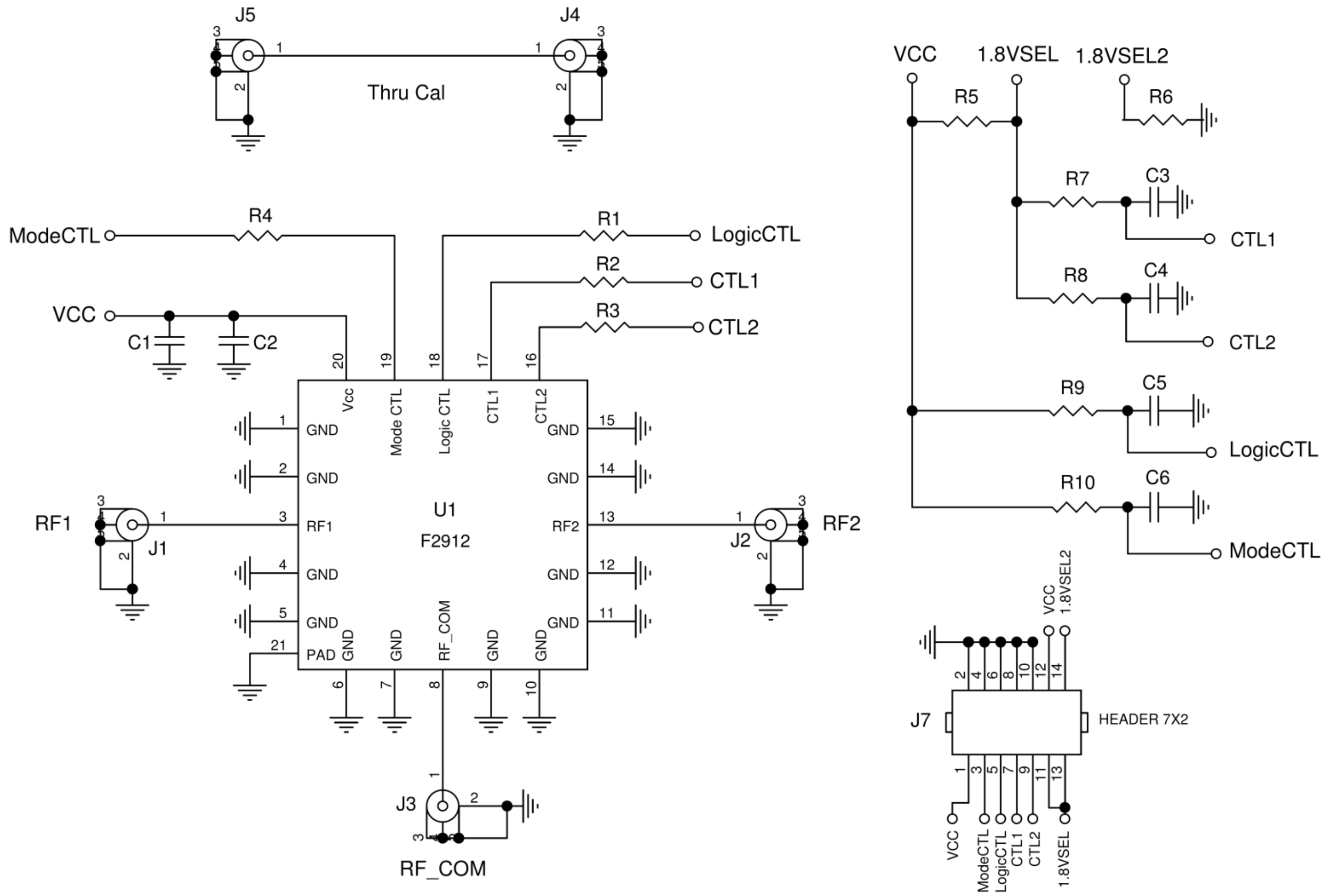
EvKit Picture (Top)



EvKit Picture (Bottom)



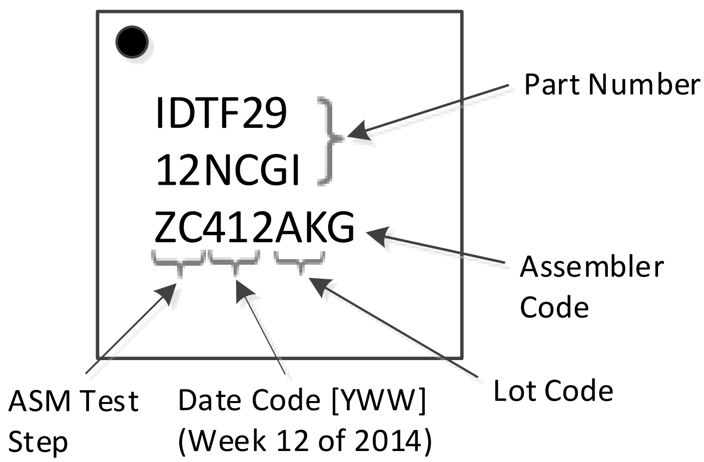
EVKIT / APPLICATIONS CIRCUIT



EVKIT BOM

Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
C1	1	1000 pF ±5%, 50V, C0G Ceramic Capacitor (0603)	GRM1885C1H102J	Murata
C2	1	0.1 µF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	Murata
C3 – C6	4	100 pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	Murata
R1 – R4	4	100 ohm ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
R5	1	15 kohm ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1502X	Panasonic
R6	1	18 kohm ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1802X	Panasonic
R7 – R10	4	100 kohm ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1003X	Panasonic
J1 – J5	5	SMA Edge Launch (0.375 inch pitch ground tabs)	142-0701-851	Emerson Johnson
J7	1	CONN HEADER VERT 7x2 POS GOLD	N2514-6002-RB	3M
U1	1	SP2T Switch 4 mm x 4 mm QFN20-EP	F2912NCGI	IDT
	1	Printed Circuit Board	F2912 EVKIT REV 4.1	IDT

TOP MARKINGS



APPLICATIONS INFORMATION

Default Start-up

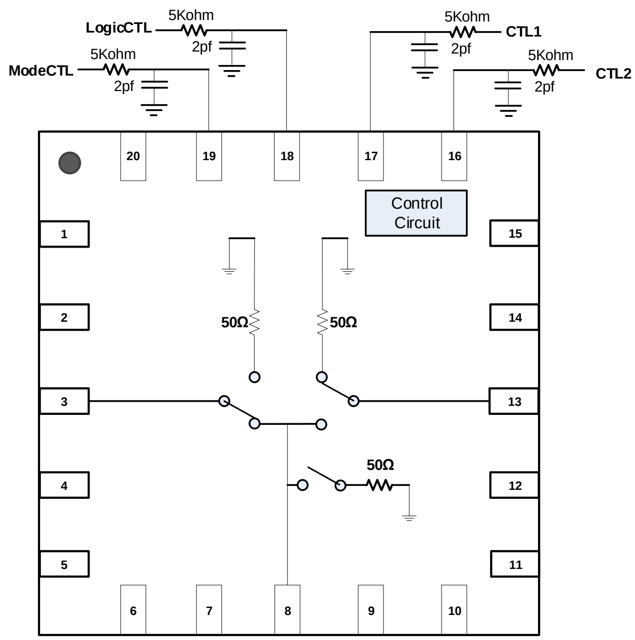
Control pins include no internal pull-down resistors to logic LOW or pull-up resistors to logic HIGH. Upon start-up, all control pins should be set to logic LOW (0) thereby enabling 2 pin switch control, opening both RF1 and RF2 paths, and setting logic control voltage to 3.3 V (see above tables for LOW logic states).

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1 V / 20 uS. In addition, all control pins should remain at 0 V (+/-0.3 V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 16, 17, 18, and 19 as shown below.



Pin Compatibility

The F2912 switch is compatible with other supplier parts which only support two wire control and 3 volt logic. Other suppliers' parts with limited functionality have pins 18 and 19 grounded. Grounding pins 18 and 19 on the F2912 will make it fully compatible with the other products.

Per Table 3 when pin 19 is grounded, the F2912 is set for 2-wire control.

Per Table 4 when pin 18 is grounded, the F2912 is set for 3.3 volt control logic. JEDEC 3.3 volt logic (JESD8C.01) allows logic high to be as low as 2.7 volts which the F2912 supports.

Contact your IDT representative for more information about compatibility with other suppliers' products.

EVKIT OPERATION

The F2912 EVkit has a number of control features available. Please refer to the EVkit Application Circuit and EVkit Picture for connections to this part. All bias and logic controls are done using J7 as an interface.

See Table 5 for the function of each pin on J7.

Table 5: EVkit J7 Interface Table

J7 PIN	PIN NAME	CONNECTIONS
1	V_{CC}	Pin to supply VCC from an external power supply.
2	GND	Pin to supply GND from an external power supply.
3	ModeCTL	Leave this pin open to select 1-pin control. A pull up resistor on the EVkit provides a logic high. If 2-pin control is desired, ground this pin by using a two pin shunt between this pin and pin 4 (GND). See Tables 1, 2, and 3 for 1-pin and 2-pin control logic.
4	GND	Pin available to shunt to pin 3 to provide a logic low.
5	LogicCTL	If using 1.8 V logic for CTL1 and CTL2, leave this pin open. A pullup resistor on the kit provides a logic high. If 3.3 V logic is used then ground this pin by using a two pin shunt between this pin and pin 6 (GND).
6	GND	Pin available to shunt to pin 5 to provide a logic low.
7	CTL1	Used to control the switch state when using the 2-pin control method. Leave this pin open to allow the EVkit pullup resistor to provide a logic high. Connect to pin 8 (GND) with a two pin shunt if a logic low is desired. Actual logic levels applied to this pin depend on the setting of LogicCTL pin. This device can be damage if the incorrect logic level is applied to this pin.
8	GND	Pin available to shunt to pin 7 to provide a logic low.
9	CTL2	Used to control the switch state when using the 1-pin or 2-pin control method. Leave this pin open to allow the EVkit pullup resistor to provide a logic high. Connect to pin 10 (GND) with a two pin shunt if a logic low is desired. Actual logic levels applied to this pin depend on the setting of LogicCTL pin. This device can be damage if the incorrect logic level is applied to this pin.
10	GND	Pin available to shunt to pin 9 to provide a logic low.
11	1.8VSEL	If using 3.3 V CTL1 and CTL2 logic, connect this pin to pin 12 (VCC) using a two pin shunt. If using 1.8 V logic then leave this pin open.*
12	V_{CC}	Internally connected on PCB to VCC on pin 1.
13	1.8VSEL	If using 1.8 V CTL1 and CTL2 logic, connect this pin to pin 14 (1.8VSEL2) using a two pin shunt. If using 3.3 V logic then leave this pin open.*
14	1.8VSEL2	If using 1.8 V CTL1 and CTL2 logic, connect this pin to pin 13 (1.8VSEL) using a two pin shunt. If using 3.3 V logic then leave this pin open.*

***** Never configure the kit to have two pin shunts for both Pin 11 to Pin 12 and Pin 13 to Pin 14.

REVISION HISTORY SHEET

Rev	Date	Page	Description of Change
0	2014-Aug-19		Initial Release
1	2014-Oct-21	17, 18, 20	Update EVKIT Photo and BOM
2	2015-Sept-4	2, 6, 12, 18	Updated to new datasheet format throughout document. Added recommended PCB land pattern information. Added pin compatible information.
3	2016-Apr-01		Added data for low frequency operation (9 kHz). Added data for higher frequency operation (9 GHz).

www.IDT.com

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.idt.com

Tech Support
www.IDT.com/go/support