

## 2:1 MULTIPLEXER CHIP FOR PCI-EXPRESS GEN1

ICS557-08

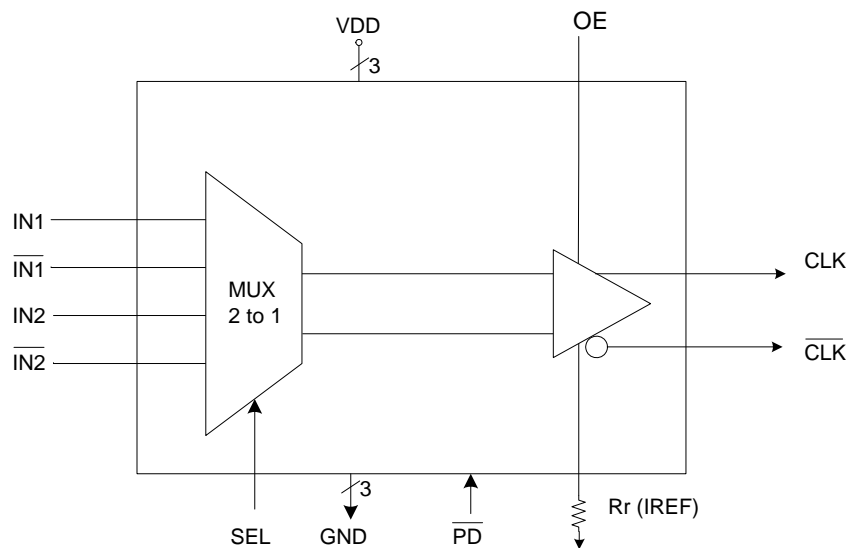
### Description

The ICS557-08 is a 2:1 multiplexer chip that allows the user to select one of the two HCSL (Host Clock Signal Level) input pairs and fans out to one pair of differential HCSL or LVDS outputs. This chip is suited especially for PCI-Express applications, where there is a need to select the PCI-Express clock either locally from the PCI-E card or from the motherboard.

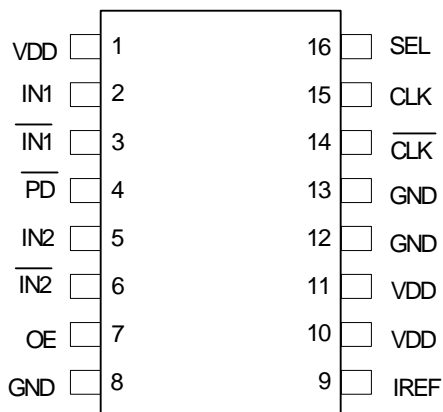
### Features

- Packaged in 16-pin TSSOP
- Pb (lead) free package
- Operating voltage of 3.3 V
- Low power consumption
- Input clock frequency of up to 200 MHz
- **For PCIe Gen2/3 applications, see the 5V41068A**

### Block Diagram



## Pin Assignment



16-pin (173 mil) TSSOP

## Select Table

| SEL | Input Pair Selected          |
|-----|------------------------------|
| 0   | IN2/ $\overline{\text{IN2}}$ |
| 1   | IN1/ $\overline{\text{IN1}}$ |

## Pin Descriptions

| Pin | Pin Name | Pin Type | Pin Description   |
|-----|----------|----------|---|
| 1   | VDD      | Power    | Connect to +3.3 V. Supply voltage for Input clocks.   |
| 2   | IN1      | Input    | HCSL true input signal 1.   |
| 3   | IN1      | Input    | HCSL complimentary input signal 1.  |
| 4   | PD       | Input    | Powers down the chip and tri-states outputs when low. Internal pull-up  |
| 5   | IN2      | Input    | HCSL true input signal 2.   |
| 6   | IN2      | Input    | HCSL complimentary input signal 2.  |
| 7   | OE       | Input    | Provides output or, tri-states output (High = enable outputs; Low = disable). Internal pull-up resistor.              |
| 8   | GND      | Power    | Connect to ground.  |
| 9   | IREF     | Output   | Precision resistor attached to this pin is connected to the internal current  |
| 10  | VDD      | Power    | Connect to +3.3 V. Supply Voltage for Output Clocks.  |
| 11  | VDD      | Power    | Connect to +3.3 V. Supply Voltage for Output Clocks.  |
| 12  | GND      | Power    | Connect to ground.  |
| 13  | GND      | Power    | Connect to ground.  |
| 14  | CLK      | Output   | HCSL/LVDS Complimentary output clock .  |
| 15  | CLK      | Output   | HCSL/LVDS True output clock.  |
| 16  | SEL      | Input    | SEL=1 selects IN1/ $\overline{\text{IN1}}$ . SEL =0 selects IN2/ $\overline{\text{IN2}}$ . Internal pull-up resistor. |

## Application Information

### Decoupling Capacitors

As with any high-performance mixed-signal IC, the ICS557-08 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01 $\mu$ F must be connected between each VDD and the PCB ground plane.

### PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

Each 0.01 $\mu$ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the ICS557-08.

This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

### External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01  $\mu$ F should be connected between VDD and GND pins as close to the device as possible.

### Current Reference Source $R_r$ ( $I_{ref}$ )

If board target trace impedance ( $Z$ ) is 50 $\Omega$ , then  $R_r = 475\Omega$  (1%), providing IREF of 2.32 mA, output current ( $I_{OH}$ ) is equal to 6\*IREF.

### Load Resistors $R_L$

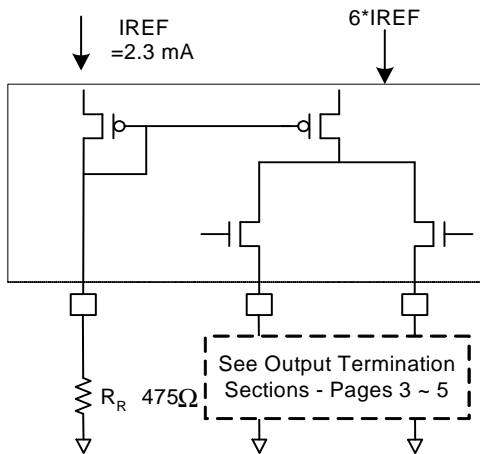
Since the clock outputs are open source outputs, 50 $\Omega$  external resistors to ground are to be connected at each clock output.

### Output Termination

The PCI-Express differential clock outputs of the ICS557-08 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The ICS557-08 can also be configured for LVDS compatible voltage levels. See the **LVDS Compatible Layout Guidelines** section.

## Output Structures



### General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each  $0.01\mu\text{F}$  decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.
2. No vias should be used between decoupling capacitor and VDD pin.
3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.
4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the ICS557-08. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

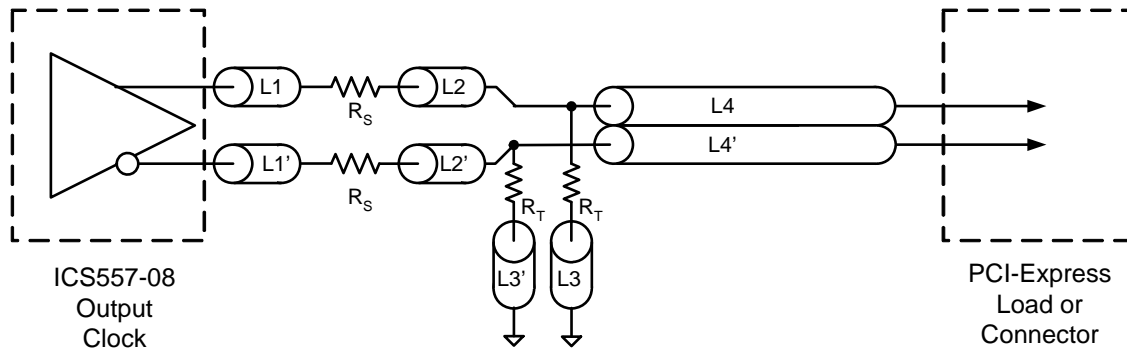
## PCI-Express Layout Guidelines

| Common Recommendations for Differential Routing | Dimension or Value | Unit |
|---|--------------------|------|
| L1 length, Route as non-coupled 50 ohm trace.   | 0.5 max            | inch |
| L2 length, Route as non-coupled 50 ohm trace.   | 0.2 max            | inch |
| L3 length, Route as non-coupled 50 ohm trace.   | 0.2 max            | inch |
| $R_S$   | 33                 | ohm  |
| $R_T$   | 49.9               | ohm  |

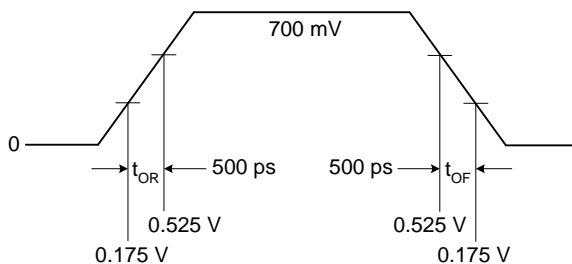
| Differential Routing on a Single PCB                                      | Dimension or Value  | Unit |
|---|---------------------|------|
| L4 length, Route as coupled <b>microstrip</b> 100 ohm differential trace. | 2 min to 16 max     | inch |
| L4 length, Route as coupled <b>stripline</b> 100 ohm differential trace.  | 1.8 min to 14.4 max | inch |

| Differential Routing to a PCI Express Connector                           | Dimension or Value    | Unit |
|---|-----------------------|------|
| L4 length, Route as coupled <b>microstrip</b> 100 ohm differential trace. | 0.25 to 14 max        | inch |
| L4 length, Route as coupled <b>stripline</b> 100 ohm differential trace.  | 0.225 min to 12.6 max | inch |

### PCI-Express Device Routing



### Typical PCI-Express (HCSL) Waveform



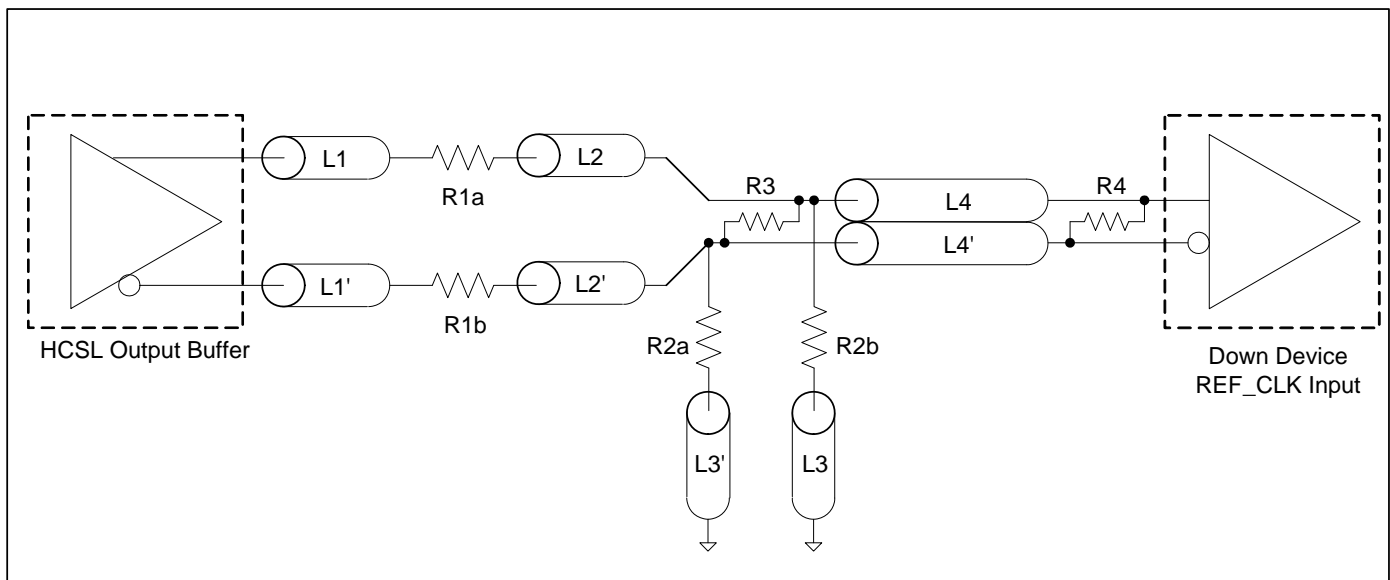
## LVDS Compatible Layout Guidelines

| Alternative Termination for LVDS and other Common Differential Signals |                  |                 |    |      |      |     |                                |
|--|------------------|-----------------|----|------|------|-----|--------------------------------|
| V <sub>diff</sub>  | V <sub>p-p</sub> | V <sub>cm</sub> | R1 | R2   | R3   | R4  | Note                           |
| 0.45v  | 0.22v            | 1.08            | 33 | 150  | 100  | 100 |                                |
| 0.58   | 0.28             | 0.6             | 33 | 78.7 | 137  | 100 |                                |
| 0.80   | 0.40             | 0.6             | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60   | 0.3              | 1.2             | 33 | 174  | 140  | 100 | Standard LVDS                  |

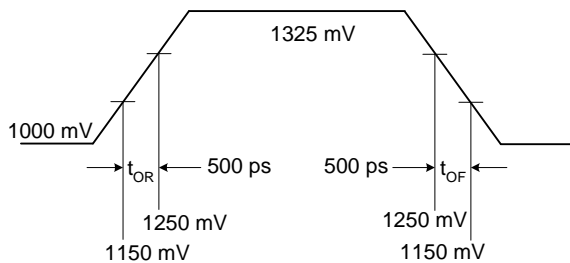
R1a = R1b = R1

R2a = R2b = R2

## LVDS Device Routing



## Typical LVDS Waveform



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS557-08. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                          | Rating              |
|-------------------------------|---------------------|
| Supply Voltage, VDD           | 7 V                 |
| All Inputs and Outputs        | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | -40 to +85° C       |
| Storage Temperature           | -65 to +150° C      |
| Junction Temperature          | 125° C              |
| Soldering Temperature         | 260° C              |
| ESD Protection (Input)        | 2000 V min. (HBM)   |

## DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V ±5%, Ambient Temperature -40 to +85° C

| Parameter                          | Symbol            | Conditions                    | Min.    | Typ. | Max.     | Units |
|------------------------------------|-------------------|-------------------------------|---------|------|----------|-------|
| Supply Voltage                     | V                 |                               | 3.135   |      | 3.465    | V     |
| Input High Voltage <sup>1</sup>    | V <sub>IH</sub>   | OE, SEL, $\overline{PD}$      | 2.0     |      | VDD +0.3 | V     |
| Input Low Voltage <sup>1</sup>     | V <sub>IL</sub>   | OE, SEL, $\overline{PD}$      | VSS-0.3 |      | 0.8      | V     |
| Input Leakage Current <sup>2</sup> | I <sub>IL</sub>   | 0 < V <sub>in</sub> < VDD     | -5      |      | 5        | μA    |
| Operating Supply Current           | I <sub>DD</sub>   | 50Ω, 2 pF                     |         |      | 40       | mA    |
|                                    | I <sub>DDOE</sub> | OE =Low                       |         |      | 20       | mA    |
|                                    | I <sub>DDPD</sub> | No load, $\overline{PD}$ =Low |         |      | 400      | μA    |
| Input Capacitance                  | C <sub>IN</sub>   | Input pin capacitance         |         |      | 7        | pF    |
| Output Capacitance                 | C <sub>OUT</sub>  | Output pin capacitance        |         |      | 6        | pF    |
| Pin Inductance                     | L <sub>PIN</sub>  |                               |         |      | 5        | nH    |
| Output Resistance                  | R <sub>OUT</sub>  | CLK outputs                   | 3.0     |      |          | kΩ    |
| Pull-up Resistor                   | R <sub>PUP</sub>  | OE, SEL, $\overline{PD}$      |         | 110  |          | kΩ    |

1. Single edge is monotonic when transitioning through region.
2. Inputs with pull-ups/-downs are not included.

## AC Electrical Characteristics

Unless stated otherwise, VDD=3.3 V ±5%, Ambient Temperature -40 to +85° C

| Parameter                               | Symbol              | Conditions  | Min.  | Typ. | Max.  | Units |
|---|---------------------|---|-------|------|-------|-------|
| Operating Frequency                     |                     | HCSL termination  |       |      | 200   | MHz   |
|   |                     | LVDS termination  |       |      | 100   | MHz   |
| Input High Voltage <sup>1,2</sup>       | V <sub>IH</sub>     | HCSL  | 660   | 700  | 850   | mV    |
| Input Low Voltage <sup>1,2</sup>        | V <sub>IL</sub>     | HCSL  | -150  | 0    |       | mV    |
| Differential Input Voltages             | V <sub>ID</sub>     | LVDS  | 250   | 350  | 450   | mV    |
| Input Offset Voltage                    | (V <sub>IS</sub> )  | LVDS  | 1.125 | 1.25 | 1.375 | V     |
| Output High Voltage <sup>1,2</sup>      | V <sub>OH</sub>     | HCSL  | 660   | 700  | 850   | mV    |
| Output Low Voltage <sup>1,2</sup>       | V <sub>OL</sub>     | HCSL  | -150  | 0    | 27    | mV    |
| Crossing Point Voltage <sup>1,2</sup>   |                     | Absolute  | 250   | 350  | 550   | mV    |
| Crossing Point Voltage <sup>1,2,4</sup> |                     | Variation over all edges  |       |      | 140   | mV    |
| Rise Time <sup>1,2</sup>                | t <sub>OR</sub>     | From 0.175 V to 0.525 V   | 175   | 332  | 700   | ps    |
| Fall Time <sup>1,2</sup>                | t <sub>OF</sub>     | From 0.525 V to 0.175 V   | 175   | 344  | 700   | ps    |
| Rise/Fall Time Variation <sup>1,2</sup> |                     |   |       |      | 125   | ps    |
| Duty Cycle <sup>1,3</sup>               |                     |   | 45    |      | 55    | %     |
| Output Enable Time <sup>5</sup>         |                     | All outputs   |       | 10   |       | μs    |
| Output Disable Time <sup>5</sup>        |                     | All outputs   |       | 10   |       | μs    |
| Stabilization Time                      | t <sub>STABLE</sub> | From power-up VDD=3.3 V   |       | 3.0  |       | ms    |
| Input to Output Delay                   |                     | Input differential clock to output differential clock delay measured at crossing point of input levels to crossing point of output levels | 2     | 4    | 6     | ns    |

<sup>1</sup> Test setup is R<sub>L</sub>=50 ohms with 2 pF, R<sub>r</sub> = 475Ω (1%).

<sup>2</sup> Measurement taken from a single-ended waveform.

<sup>3</sup> Measurement taken from a differential waveform.

<sup>4</sup> Measured at the crossing point where instantaneous voltages of both CLK and  $\overline{\text{CLK}}$  are equal.

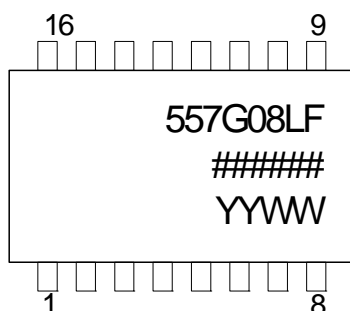
<sup>5</sup> CLK and  $\overline{\text{CLK}}$  pins are tri-stated when OE is Low asserted. CLK and  $\overline{\text{CLK}}$  are driven differential when OE is High unless its  $\overline{\text{PD}}$  = low.



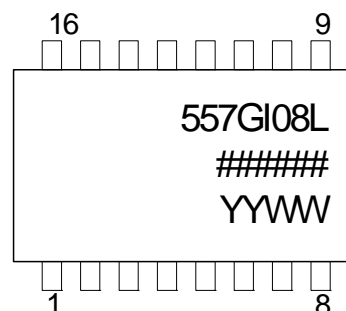
## Thermal Characteristics

| Parameter                              | Symbol        | Conditions     | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air      |      | 93   |      | °C/W  |
|  | $\theta_{JA}$ | 1 m/s air flow |      | 78   |      | °C/W  |
|  | $\theta_{JA}$ | 3 m/s air flow |      | 65   |      | °C/W  |
| Thermal Resistance Junction to Case    | $\theta_{JC}$ |                |      | 20   |      | °C/W  |

### Marking Diagram (ICS557G-08LF)



### Marking Diagram (ICS557GI-08LF)

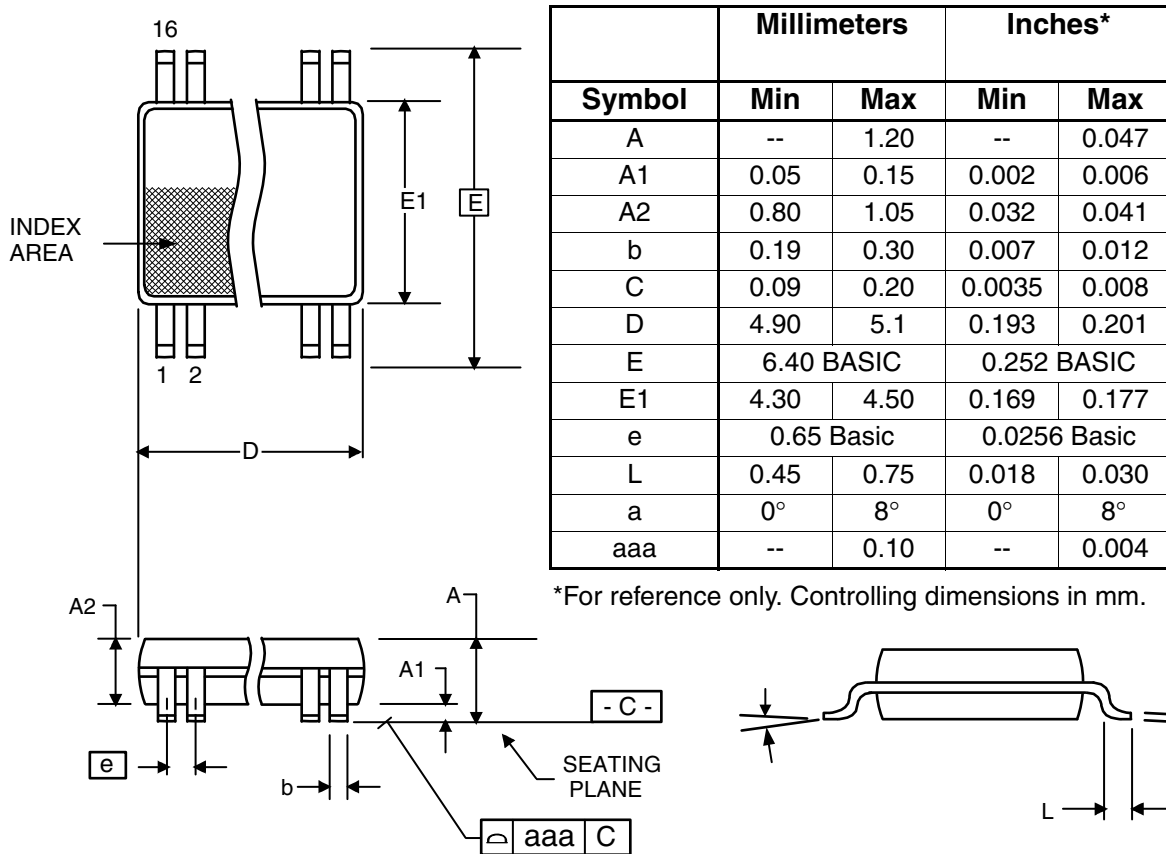


#### Notes:

- ##### is the lot code.
- YYWW is the last two digits of the year, and the week number that the part was assembled.
- “LF” denotes Pb free package.
- “I” denotes industrial temperature device
- Bottom marking: (origin). Origin = country of origin if not USA.

## Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



## Ordering Information

| Part / Order Number | Marking    | Shipping Packaging | Package      | Temperature   |
|---------------------|------------|--------------------|--------------|---------------|
| 557G-08LF           | see page 9 | Tubes              | 16-pin TSSOP | 0 to +70° C   |
| 557G-08LFT          |            | Tape and Reel      | 16-pin TSSOP | 0 to +70° C   |
| 557GI-08LF          |            | Tubes              | 16-pin TSSOP | -40 to +85° C |
| 557GI-08LFT         |            | Tape and Reel      | 16-pin TSSOP | -40 to +85° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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## Revision History

| Rev. | Originator | Date     | Description of Change  |
|------|------------|----------|--|
| C    | D.Chan     | 02/16/06 | Added industrial temp range; updated PCI-Express Waveform diagram to include 0.525 V; changed "Supply Voltage, VDD" spec in Absolute Max. Ratings from 5.5 V to 7 V; changed CLKOUT to CLK and $\overline{\text{CLK}}$ ; added marking diagrams for I-temp device. |
| D    | Arvind     | 05/17/07 | Removed Cycle-to-cycle jitter spec.  |
| E    |            | 06/26/07 | Added 27mV to VOL max. spec  |
| F    |            | 09/24/09 | Added EOL note for non-green parts.  |
| G    |            | 10/05/09 | Updated "Input to Output Delay" parameter.   |
| H    |            | 05/13/10 | Removed EOL note for non-green parts.  |
| J    | A.T.       | 12/15/10 | Updated LVDS termination table and diagram   |
| K    | LPL        | 08/02/11 | Updates to product description and Features bullets on pg.1  |
| L    | K.B.       | 11/21/11 | 1. Added "Gen1" to title<br>2. Added note in Features section, "For PCIe Gen2/3 applications, see the 5V41068A"  |

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