



2.5V ZERO DELAY CLOCK BUFFER, SPREAD SPECTRUM COMPATIBLE

IDT23S09T

FEATURES:

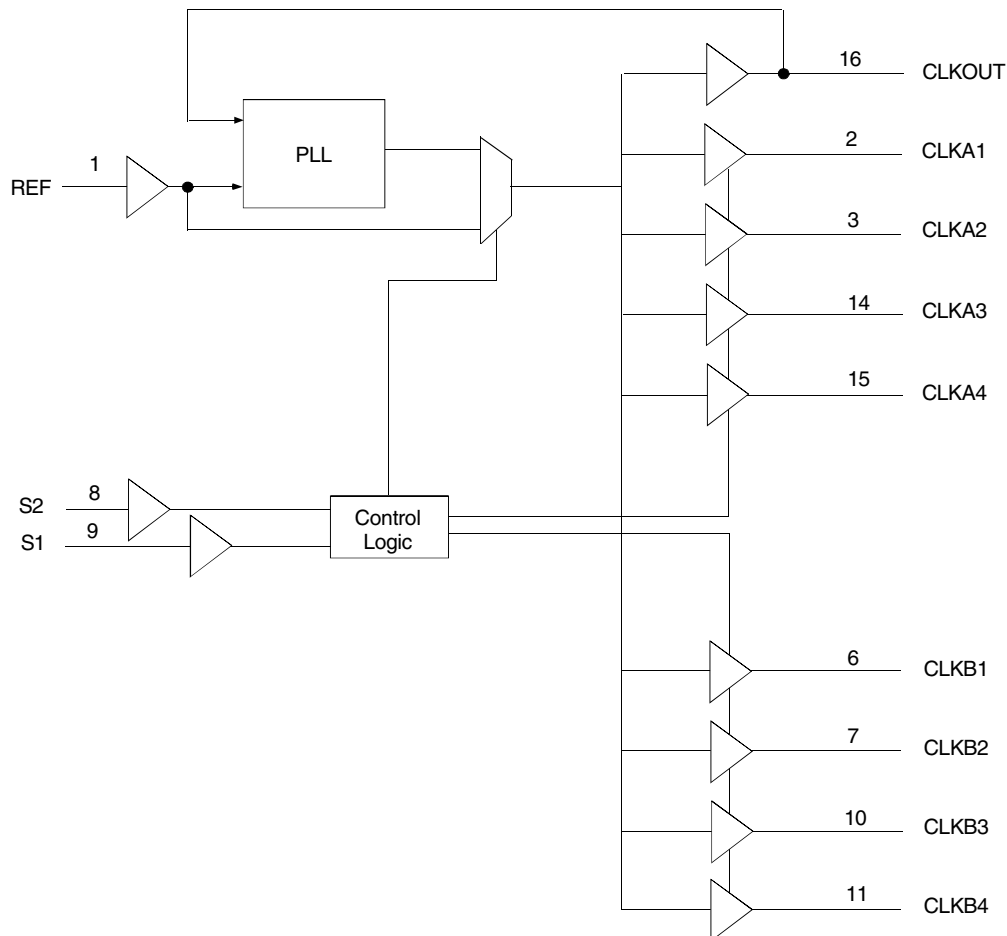
- Phase-Lock Loop Clock Distribution
- 10MHz to 133MHz operating frequency
- Distributes one clock input to one bank of five and one bank of four outputs
- Separate output enable for each output bank
- Output Skew < 250ps
- Low jitter <200 ps cycle-to-cycle
- No external RC network required
- Operates at 2.5V V_{DD}
- Spread spectrum compatible
- Available in SOIC package

DESCRIPTION:

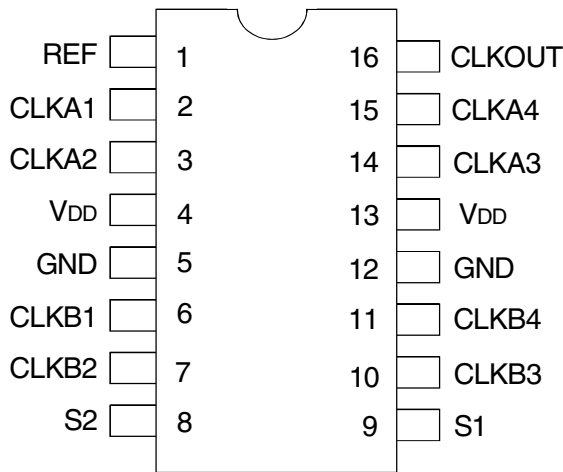
The IDT23S09T is a high-speed phase-lock loop (PLL) clock buffer, designed to address high-speed clock distribution applications. The zero delay is achieved by aligning the phase between the incoming clock and the output clock, operable within the range of 10 to 133MHz.

The IDT23S09T is a 16-pin version of the IDT23S05T. The IDT23S09T accepts one reference input, and drives two banks of four low skew clocks. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad. In the absence of an input clock, the IDT23S09T enters power down, and the outputs are tri-stated. In this mode, the device will draw less than 12µA.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC
TOP VIEW

APPLICATIONS:

- SDRAM
- Telecom
- Datacom
- PC Motherboards/Workstations
- Critical Path Delay Designs

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Max. | Unit |
|---|----------------------------------|------------------------------|------|
| V _{DD} | Supply Voltage Range | -0.5 to +4.6 | V |
| V _I ⁽²⁾ | Input Voltage Range (REF) | -0.5 to +5.5 | V |
| V _I | Input Voltage Range (except REF) | -0.5 to V _{DD} +0.5 | V |
| I _{IK} (V _I < 0) | Input Clamp Current | -50 | mA |
| I _O (V _O = 0 to V _{DD}) | Continuous Output Current | ±50 | mA |
| V _{DD} or GND | Continuous Current | ±100 | mA |
| T _A = 55°C (in still air) ⁽³⁾ | Maximum Power Dissipation | 0.7 | W |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| Operating Temperature | Commercial Temperature Range | 0 to +70 | °C |

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PIN DESCRIPTION

| Pin Name | Pin Number | Type | Functional Description |
|-----------------------|------------|------|---|
| REF ⁽¹⁾ | 1 | IN | Input reference clock, 3.3V tolerant input |
| CLKA1 ⁽²⁾ | 2 | Out | Output clock for bank A |
| CLKA2 ⁽²⁾ | 3 | Out | Output clock for bank A |
| V _{DD} | 4, 13 | PWR | 2.5V Supply |
| GND | 5, 12 | GND | Ground |
| CLKB1 ⁽²⁾ | 6 | Out | Output clock for bank B |
| CLKB2 ⁽²⁾ | 7 | Out | Output clock for bank B |
| S2 ⁽³⁾ | 8 | IN | Select input Bit 2 |
| S1 ⁽³⁾ | 9 | IN | Select input Bit 1 |
| CLKB3 ⁽²⁾ | 10 | Out | Output clock for bank B |
| CLKB4 ⁽²⁾ | 11 | Out | Output clock for bank B |
| CLKA3 ⁽²⁾ | 14 | Out | Output clock for bank A |
| CLKA4 ⁽²⁾ | 15 | Out | Output clock for bank A |
| CLKOUT ⁽²⁾ | 16 | Out | Output clock, internal feedback on this pin |

NOTES:

1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs.

FUNCTION TABLE⁽¹⁾

| S2 | S1 | CLKA | CLKB | CLKOUT ⁽²⁾ | Output Source | PLL Shut Down |
|----|----|-----------|-----------|-----------------------|---------------|---------------|
| L | L | Tri-State | Tri-State | Driven | PLL | N |
| L | H | Driven | Tri-State | Driven | PLL | N |
| H | L | Driven | Driven | Driven | REF | Y |
| H | H | Driven | Driven | Driven | PLL | N |

NOTES:

- H = HIGH Voltage Level.
L = LOW Voltage Level
- This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the REF and the output.

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|--------------------|--------------------------|--|------|------|------|
| V _{IL} | Input LOW Voltage Level | | — | 0.7 | V |
| V _{IH} | Input HIGH Voltage Level | | 1.7 | — | V |
| I _{IL} | Input LOW Current | V _{IN} = 0V | — | 50 | μA |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | — | 100 | μA |
| V _{OL} | Output LOW Voltage | Standard Drive, I _{OL} = 8mA | — | 0.3 | V |
| V _{OH} | Output HIGH Voltage | Standard Drive, I _{OH} = -8mA | 2 | — | V |
| I _{DD_PD} | Power Down Current | REF = 0MHz (S2 = S1 = H) | — | 12 | μA |
| I _{DD} | Supply Current | Unloaded Outputs at 66.66MHz, SEL inputs at V _{DD} or GND | — | 32 | mA |

OPERATING CONDITIONS

| Symbol | Parameter | Min. | Max. | Unit |
|-----------------|---|------|------|------|
| V _{DD} | Supply Voltage | 2.3 | 2.7 | V |
| T _A | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| C _L | Load Capacitance 10MHz - 133MHz | — | 15 | pF |
| C _{IN} | Input Capacitance | — | 7 | pF |

SWITCHING CHARACTERISTICS^(1,2)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-------------------|---|--|------|------|------|------|
| t ₁ | Output Frequency | 15pF Load | 10 | — | 133 | MHz |
| | Duty Cycle = t ₂ ÷ t ₁ | Measured at V _{DD} /2, F _{OUT} = 66.66MHz | 40 | 50 | 60 | % |
| t ₃ | Rise Time | Measured between 0.7V and 1.7V | — | — | 2.5 | ns |
| t ₄ | Fall Time | Measured between 0.7V and 1.7V | — | — | 2.5 | ns |
| t ₅ | Output to Output Skew | All outputs equally loaded | — | — | 250 | ps |
| t _{6A} | Delay, REF Rising Edge to CLKOUT Rising Edge ⁽²⁾ | Measured at V _{DD} /2 | — | 0 | ±350 | ps |
| t _{6B} | Delay, REF Rising Edge to CLKOUT Rising Edge ⁽²⁾ | Measured at V _{DD} /2 in PLL bypass mode | 1 | 5 | 8.7 | ns |
| t ₇ | Device-to-Device Skew | Measured at V _{DD} /2 on the CLKOUT pins of devices | — | 0 | 700 | ps |
| t _J | Cycle-to-Cycle Jitter | Measured at 66.66MHz, loaded outputs | — | — | 200 | ps |
| t _{LOCK} | PLL Lock Time | Stable power supply, valid clock presented on REF pin | — | — | 1 | ms |

NOTES:

- REF Input has a threshold voltage of V_{DD}/2.
- All parameters specified with loaded outputs.

ZERO DELAY AND SKEW CONTROL

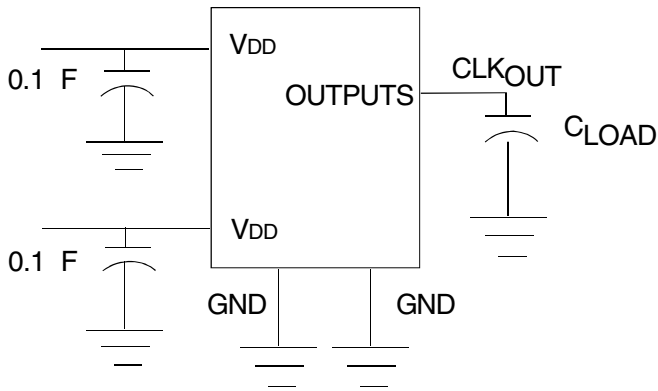
All outputs should be uniformly loaded in order to achieve Zero I/O Delay. Since the CLKOUT pin is the internal feedback for the PLL, its relative loading can affect and adjust the input/output delay.

For designs utilizing zero I/O Delay, all outputs including CLKOUT must be equally loaded. Even if the output is not used, it must have a capacitive load equal to that on the other outputs in order to obtain true zero I/O Delay. For zero output-to-output skew, all outputs must be loaded equally.

SPREAD SPECTRUM COMPATIBLE

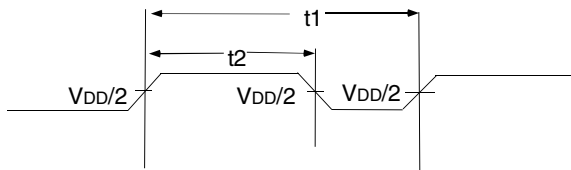
Many systems being designed now use a technology called Spread Spectrum Frequency Timing Generation. This product is designed not to filter off the Spread Spectrum feature of the reference input, assuming it exists. When a zero delay buffer is not designed to pass the Spread Spectrum feature through, the result is a significant amount of tracking skew, which may cause problems in systems requiring synchronization.

TEST CIRCUIT

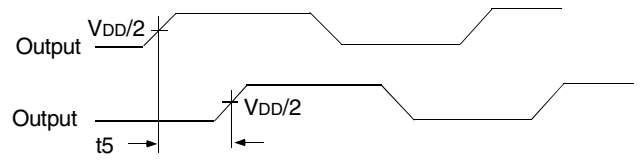


Test Circuit for All Parameters

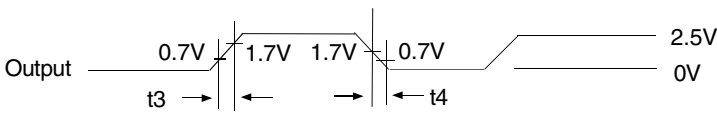
SWITCHING WAVEFORMS



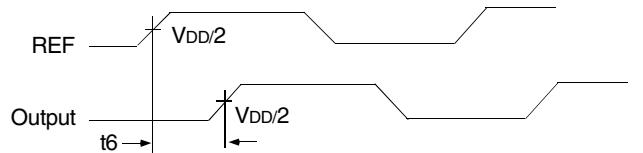
Duty Cycle Timing



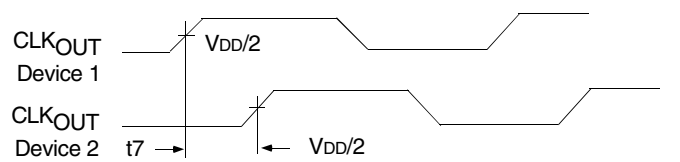
Output to Output Skew



All Outputs Rise/Fall Time

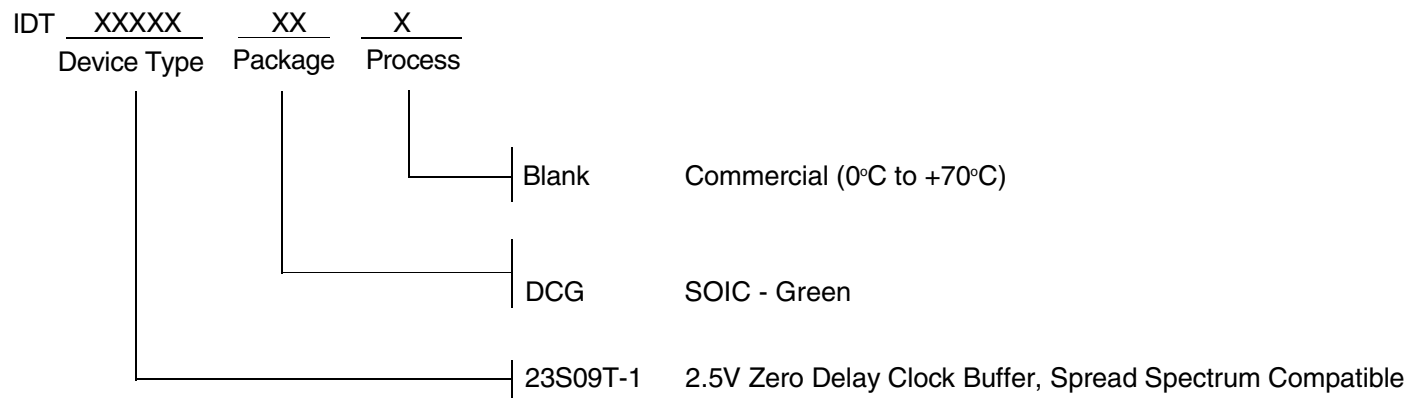


Input to Output Propagation Delay



Device to Device Skew

ORDERING INFORMATION



| Part / Order Number | Shipping Packaging | Package | Temperature |
|----------------------------|---------------------------|----------------|--------------------|
| 23S09T-1DCG | Tubes | 16-pin SOIC | 0° to +70° C |
| 23S09T-1DCG8 | Tape and Reel | 16-pin SOIC | 0° to +70° C |



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