

DATA SHEET

SURFACE-MOUNT CERAMIC MULTILAYER CAPACITORS

C-Array NPO/X7R/Y5V 16 V TO 50 V sizes 0508 (4 x 0402) / 0612 (4 x 0603)

RoHS compliant & Halogen Free



YAGEO Phícomp

Surface-Mount Ceramic Multilayer Capacitors 4C-Arroy NP0/X7R/Y5V

Product specification $\frac{2}{17}$

<u>SCOPE</u>

This specification describes NP0/X7R/Y5V 4-capacitor Array with lead-free terminations.

APPLICATIONS

- Professional electronics
- High density consumer electronics

FEATURES

- Supplied in tape on reel
- Nickel-barrier end termination
- 0508 (4x0402) / 0612 (4x0603) capacitors (of the same capacitance value) per array
- Less than 50% board space of an equivalent discrete component
- High volumetric efficiency
- Increased throughout, by time saved in mounting
- RoHS compliant
- Halogen Free compliant

ORDERING INFORMATION - GLOBAL PART NUMBER, PHYCOMP

CTC & 12NC

All part numbers are identified by the series, size, tolerance, TC material, packing style, voltage, process code, termination and capacitance value. Please note that 12 digits ordering code will expire at the end of 2010.

YAGEO BRAND ordering code

GLOBAL PART NUMBER (PREFERRED)

CA <u>xxxx</u> <u>x</u> <u>x</u> <u>xxx</u> <u>x</u> B <u>x</u> <u>xxx</u> (1) (2) (3) (4) (5) (6) (7)

(I) SIZE – INCH BASED (METRIC)

0508	(1220)

0612 (1632)

(2) TOLERANCE

 $J = \pm 5\%$ $K = \pm 10\%$ $M = \pm 20\%$ Z = -20% to $\pm 80\%$

(3) PACKING STYLE

- R = Paper/PE taping reel; Reel 7 inch
- P = Paper/PE taping reel; Reel 13 inch

(4) TC MATERIAL

- NPO
- X7R
- Y5V

(5) RATED VOLTAGE

7	=	16	V
1			•

 $8 = 25 \lor$ $9 = 50 \lor$

(6) PROCESS

- N = NP0
- B = class 2 material

(7) CAPACITANCE VALUE

2 significant digits+number of zeros

The 3rd digit signifies the multiplying factor, and letter R is decimal point

Example: $|2| = |2 \times 10| = |20 \text{ pF}$



YAGEO	Phícomp			Product specification 3
	Surface-Mount Ceramic Multilayer Capacitors	4C-Array	NP0/X7R/Y5V	16 V to 50 V

CONSTRUCTION

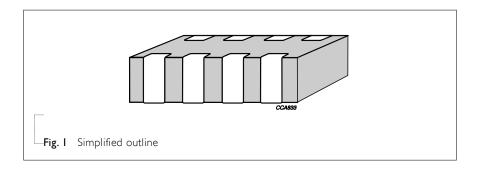
The capacitor consists of a rectangular block of ceramic dielectric in which a number of interleaved metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two end terminations and finally covered with a layer of plated tin (NiSn).

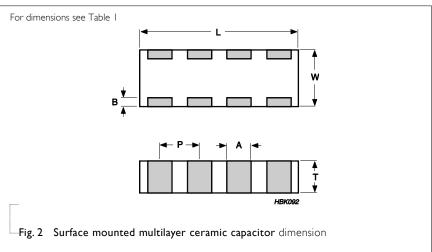
The terminations are lead-free. An outline of the structure is shown in Fig. I.

DIMENSIONS

Table I TYPE	0508 (4 X 0402)	0612 (4 X 0603)
L (mm)	2.0 ±0.15	3.2 ±0.15
W (mm)	1.25 ±0.15	1.60 ±0.15
T _{min.} (mm)	0.50	0.70
T _{max.} (mm)	0.70	0.90
A (mm)	0.28 ±0.10	0.4 ±0.10
B (mm)	0.2 ±0.10	0.3 ±0.20
P (mm)	0.5 ±0.10	0.8 ±0.10



OUTLINES





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	Surface-Mount Ceramic Multilayer Capacitors	4C-Array	NP0/X7R/Y5V	16 V to 50 V	17

		characteristic material from NP0	1
100V	0612 (4 × 0603) 50 V	0508 (4 × 0402) 50 ∨	CAPACITANCE
1001	50 V	50 V	
			IO pF
			I5 pF
			18 pF
			22 pF
			33 pF
			39 pF
			47 pF
		0.6±0.1	56 pF
			68 pF
0.8±0.1	0.8±0.1		82 pF
			100 pF
			120 pF
			150 pF
			180 pF
			220 pF
			270 pF
			330 pF
			390 pF
			470 pF
			560 pF
			680 pF
			820 pF
			I.0 nF

CAPACITANCE RANGE & THICKNESS FOR 4C-ARRAY

ΝΟΤΕ

Values in shaded cells indicate thickness class in mm



YAGEO Phicomp			Product specification	5
Surface-Mount Ceramic Multilayer Capacitors	4C-Array	NP0/X7R/Y5V	16 V to 50 V	17

CAPACITANCE RANGE & THICKNESS FOR 4C-ARRAY

 Table 3
 Temperature characteristic material from X7R
 CAPACITANCE 0508 (4 x 0402) 0612 (4 x 0603) 16 V 25 V 50 V 16 V 25 V 50 V 180 pF 220 pF 270 pF 330 pF 390 pF 470 pF 560 pF 680 pF 820 pF 0.6±0.1 1.0 nF 1.2 nF 0.8±0.1 1.5 nF 1.8 nF 2.2 nF 2.7 nF 0.8±0.1 3.3 nF 0.6±0.1 3.9 nF 0.8±0.1 4.7 nF 5.6 nF 6.8 nF 8.2 nF 0.6±0.1 10 nF 12 nF 15 nF 18 nF 22 nF 27 nF 33 nF 47 nF 56 nF 68 nF 82 nF 100 nF

ΝΟΤΕ

Values in shaded cells indicate thickness class in mm

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CAPACITANCE RANGE & THICKNESS FOR 4C-ARRAY

Table 4 Temperature characteristic material from Y5V

0612 (4 × 0603)	CAPACITANCE
25 V	
F	10 nF
	22 nF
0.6±0.1	47 nF
F	100 nF

ΝΟΤΕ

Values in shaded cells indicate thickness class in mm

THICKNESS CLASSES AND PACKING QUANTITY

Table 5				
SIZE	THICKNESS	TAPE WIDTH QUANTITY	Ø180 MM / 7 INCH	Ø180 MM / 13 INCH
CODE	CLASSIFICATION	PER REEL	Paper	Paper
0508	0.6 ±0.1 mm	8 mm	4,000	20,000
0612	0.8 ±0.1 mm	8 mm	4,000	5,000



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ELECTRICAL CHARACTERISTICS

4C-ARRAY DIELECTRIC CAPACITORS; NISN TERMINATIONS

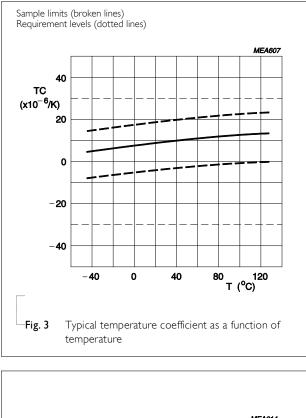
Unless otherwise stated all electrical values apply at an ambient temperature of 20 ± 1 °C, an atmospheric pressure of 86 to 106 kPa, and a relative humidity of 63 to 67%.

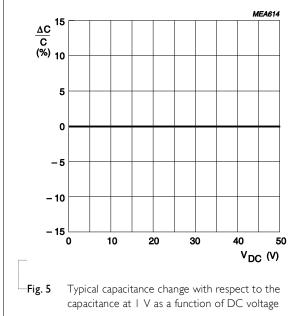
		Table 6
VAL		DESCRIPTION
10 pF to 100		Capacitance range
		Rated voltage
50	NP0	
0508: 16 V, 0612: 16 V to 50	X7R	
0612: 25	Y5V	
		Capacitance tolerance
±5%, ±10	NP0	
±10%, ±20	X7R	
-20% to +80	Y5∨	
		Dissipation factor (D.F.)
≤ 0.	NP0	
I6 V ≤ 3.5%, 25V ≤ 2.5%, 50V ≤ 2.	X7R	
2nF~ 00nF, Df ≤		
0508 ≤ 9%, 0612 ≤ ⁻	Y5∨	
$R_{ins} \geq$ 10 GQ or R_{ins} × $C_r \geq$ 500 seconds whichever is le		Insulation resistance after I minute at U _r (DC)
	ture	Maximum capacitance change as a function of temperature (temperature characteristic/coefficient):
±30 ppm/	NP0	
±1!	X7R	
+22% to -82	Y5V	
		Operating temperature range:
−55 °C to +125	NP0	
−55 °C to +125	X7R	
−30 °C to +85	Y5∨	

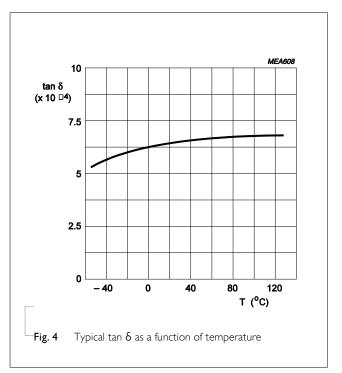


YAGEO	Phícomp		Product specification 8
	Surface-Mount Ceramic Multilayer Capacitors 4C-Array	NP0/X7R/Y5V	16 V to 50 V

NP0 0508/0612 50 V

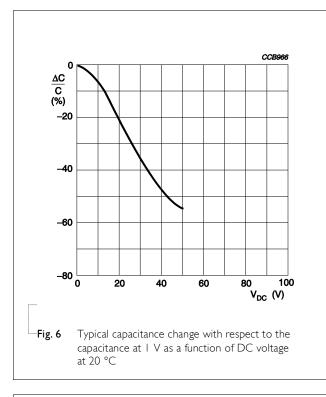


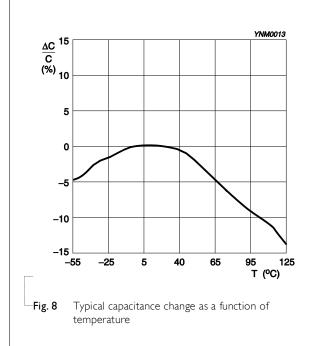


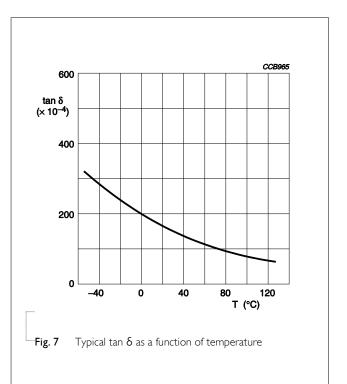


YAGEO	Phícomp			Product specification	9
	Surface-Mount Ceramic Multilayer Capacitors	4C-Array	NP0/X7R/Y5V	16 V to 50 V	17

X7R 0508 | 6 V

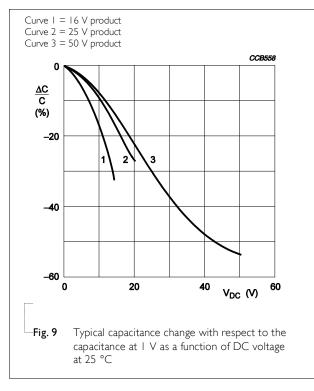


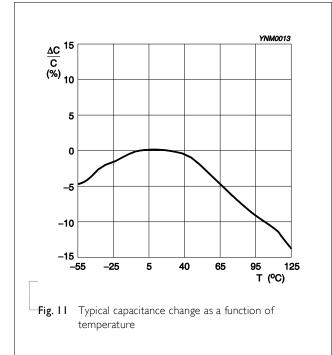


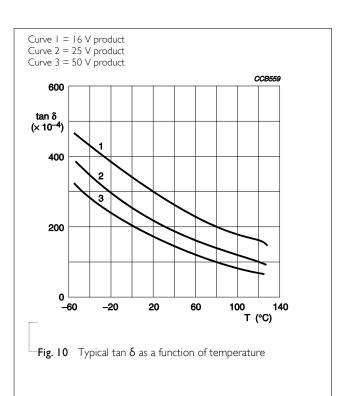


YAGEO	Phícomp			Product specification	10
	Surface-Mount Ceramic Multilayer Capacitors	4C-Array	NP0/X7R/Y5V	16 V to 50 V	17

X7R 0612 | 6 V to 50 V



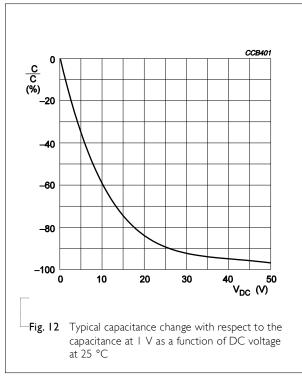


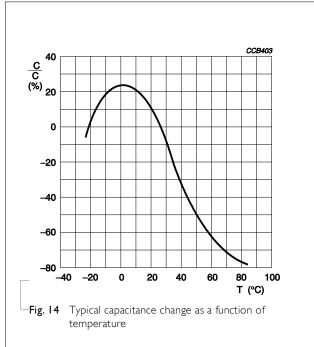


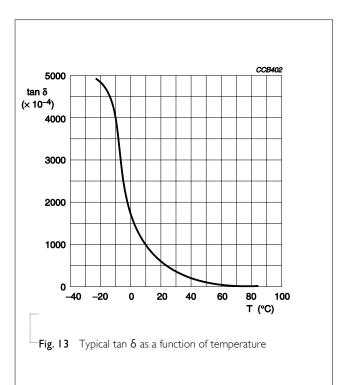


	Phicomp			Product specification	11
ę	Surface-Mount Ceramic Multilayer Capacitors	4C-Array	NP0/X7R/Y5V	16 V to 50 V	17

Y5V 0612 25 V







YAGEO	Phícomp			Product specification	12
	Surface-Mount Ceramic Multilayer Capacitors	4C-Array	NP0/X7R/Y5V	16 V to 50 V	17

TESTS AND REQUIREMENTS

TEST	TEST MET	HOD	PROCEDURE	REQUIREMENTS
Mounting	IEC 60384- 21/22	4.3	The capacitors may be mounted on printed-circuit boards or ceramic substrates	No visible damage
Visual Inspection and Dimension Check		4.4	Any applicable method using × 10 magnification	In accordance with specification
Capacitance		4.5.I	Class I: $f = 1 \text{ MHz}$ for $C \le 1 \text{ nF}$, measuring at voltage 1 V_{rms} at 20 °C $f = 1 \text{ KHz}$ for $C \ge 1 \text{ nF}$, measuring at voltage 1 V_{rms} at 20 °C Class 2: $f = 1 \text{ KHz}$ for $C \le 10 \mu$ F, measuring at voltage 1 V_{rms} at 20 °C $f = 120 \text{ Hz}$ for $C \ge 10 \mu$ F, measuring at voltage 0.5 V _{rms} at 20 °C	Within specified tolerance
Dissipation Factor (D.F.)		4.5.2	Class I: $f = 1 \text{ MHz}$ for $C \le 1 \text{ nF}$, measuring at voltage 1 V _{rms} at 20 °C f = 1 KHz for $C > 1 nF$, measuring at voltage 1 V _{rms} at 20 °C Class 2: $f = 1 \text{ KHz}$ for $C \le 10 \mu\text{F}$, measuring at voltage 1 V _{rms} at 20 °C $f = 120 \text{ Hz}$ for $C > 10 \mu\text{F}$, measuring at voltage 0.5 V _{rms} at 20 °C	In accordance with specification
Insulation Resistance		4.5.3	At U _r (DC) for I minute	In accordance with specification



Surface-Mount Ceramic Multilayer Capacitors 4C-Array NP0/X7R/Y5V

16 V to 50 V

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
Temperature Coefficient	4.6	Capacitance shall be measured by the steps shown in the following table. The capacitance change should be measured after 5 min at each	<general purpose="" series=""> Class1: Δ C/C: ±30ppm Class2:</general>
		specified temperature stage.	Class2: X7R: Δ C/C: ±15%
		Step Temperature(°C)	Y5V: Δ C/C: 22~-82%
		a 25±2	<high capacitance="" series=""></high>
		b Lower temperature±3°C	Class2: X7R/X5R: Δ C/C: ±15%
		c 25±2	Y5V: Δ C/C: 22~-82%
		d Upper Temperature±2°C	
		e 25±2	
		(1) Class I	
		Temperature Coefficient shall be calculated from the formula as below	
		Temp, Coefficient = $\frac{C2 - CI}{CI \times \Delta T} \times 10^6 \text{ [ppm/°C]}$	
		CI: Capacitance at step c	
		C2: Capacitance at 125°C	
		ΔT: 100°C(=125°C-25°C)	
		(2) Class II	
		Capacitance Change shall be calculated from the formula as below	
		$\Delta C = \frac{C2 - C1}{C1} \times 100\%$	
		CI: Capacitance at step c	
		C2: Capacitance at step b or d	
Adhesion	4.7	A force applied for 10 seconds to the line joining the terminations and in a plane parallel to the substrate	Force size ≥ 0603: 5N size = 0402: 2.5N size = 0201: 1N



Surface-Mount Ceramic Multilayer Capacitors 4C-Array NP0/X7R/Y5V

Product specification $\frac{14}{17}$ 16 V to 50 V

TEST	TEST MET	HOD	PROCEDURE	REQUIREMENTS
Bond Strength of	IEC 60384- 21/22	4.8	Mounting in accordance with IEC 60384-22 paragraph 4.3	No visible damage
Plating on End Face			Conditions: bending I mm at a rate of I mm/s,	<general purpose="" series=""></general>
			radius jig 340 mm	$\Delta C/C$
			,	Class I:
				NP0: within $\pm 1\%$ or 0.5 pF, whichever is greater
				Class2:
				X5R/X7R/Y5V: ±10%
				<high capacitance="" series=""></high>
				$\Delta C/C$
				Class2:
				X5R/X7R/Y5V: ±10%
Resistance to		4.9	Precondition: 150 +0/–10 °C for 1 hour, then	Dissolution of the end face plating shall not
Soldering Heat			keep for 24 \pm l hours at room temperature	exceed 25% of the length of the edge
			Preheating for size \leq 1206: 120 °C to 150 °C for	concerned
			l minute	<general purpose="" series=""></general>
			Preheating: for size >1206: 100 °C to 120 °C for	$\Delta C/C$
			I minute and I70 °C to 200 °C for I minute	Class I:
			Solder bath temperature: 260 \pm 5 °C	NPO: within $\pm 0.5\%$ or 0.5 pF, whichever is greater
			Dipping time: 10 \pm 0.5 seconds	Class2:
			Recovery time: 24 ±2 hours	X5R/X7R: ±10% Y5V: ±20%
				<high capacitance="" series=""></high>
				$\Delta C/C$
				Class2:
				X5R/X7R: ±10%
				Y5V: ±20%
				D.F. within initial specified value
				R_{ins} within initial specified value
Solderability		4.10	Preheated the temperature of 80 °C to 140 °C and maintained for 30 seconds to 60 seconds.	The solder should cover over 95% of the critical area of each termination
			Test conditions for lead containing solder alloy	
			Temperature: 235 ±5 °C	
			Dipping time: 2 \pm 0.2 seconds	
			Depth of immersion: 10 mm	
			Alloy Composition: 60/40 Sn/Pb Number of immersions: 1	
			Test conditions for leadfree containing solder alloy	
			Temperature: 245 ±5 °C	
			Dipping time: 3 ±0.3 seconds	
			Depth of immersion: 10 mm	
			Alloy Composition: SAC305	
			Number of immersions: 1	



Surface-Mount Ceramic Multilayer Capacitors 4C-Array NP0/X7R/Y5V

Product specif 16 V to 50 V

ification	15
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TEST	TEST METH	IOD	PROCEDURE	REQUIREMENTS
Rapid Change	e IEC 60384- 4.11 21/22		Preconditioning	No visual damage
of T	21/22		150 +0/-10 °C for 1 hour, then keep for	<general purpose="" series=""></general>
Temperature			24 \pm 1 hours at room temperature	$\Delta C/C$
			5 cycles with following detail:	
			30 minutes at lower category temperature	Class 1: NP0: within ±1% or 1 pF, whichever is greater
			30 minutes at upper category temperature	Class2:
				Classz: X5R/X7R: \pm 15%
			Recovery time 24 \pm 2 hours	Y5V: ±20%
				<high capacitance="" series=""></high>
				$\Delta C/C$
				Class2:
				X5R/X7R: ±15%
				Y5V: ±20%
				D.F. meet initial specified value
				R _{ins} meet initial specified value
Damp Heat		4.13	1. Preconditioning, class 2 only:	No visual damage after recovery
with U _r Load			150 +0/−10 °C /1 hour, then keep for 24 ±1 hour at room temp	<general purpose="" series=""></general>
				$\Delta C/C$
			2. Initial measure:	Class I:
			Spec: refer initial spec C, D, IR	
			3. Damp heat test: 500 ± 12 hours at 40 ± 2 °C:	NP0: within $\pm 2\%$ or 1 pF, whichever is greater
			500 ±12 hours at 40 ±2 °C; 90 to 95% R.H. 1.0 U _r applied	Class2: X5R/X7R: ±15%; Y5V: ±30%
			4. Recovery: Class I: 6 to 24 hours	D.F.
			Class 2: 24 ± 2 hours	Class 1: NP0: $\leq 2 \times$ specified value
			5. Final measure: C, D, IR	Class2:
				$X5R/X7R$: $\leq 16V$: $\leq 7\%$
			P.S. If the capacitance value is less than the	$\geq 25V: \leq 5\%$
			minimum value permitted, then after the	Y5V: ≤ 15%
			other measurements have been made the	R _{ins}
			capacitor shall be precondition according to	Class I:
			<i>"IEC 60384 4.1"</i> and then the requirement	NPO: \geq 2,500 M Ω or R _{ins} x C _r \geq 25s whichever is less
			shall be met.	Class2:
				X5R/X7R/Y5V: ≥ 500 M Ω or R _{ins} × C _r ≥ 25s
				whichever is less
				<high capacitance="" series=""></high>
				ΔC/C
				Class2: X5R/X7R: ±20%; Y5V: ±30%
				D.F.
				Class2: $2 \times initial$ value max
				R _{ins}
				Class2: 500 MΩ or R _{ins} x C _r ≥ 25s, whichever is less
				Class2, 500 Fig2 of $N_{ins} \times C_r \ge 255$, while level is less
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Surface-Mount Ceramic Multilayer Capacitors 4C-Array NP0/X7R/Y5V 16 V to 50 V

Product specification  $\frac{16}{17}$ 

TEST	TEST METH	IOD	PROCEDURE	REQUIREMENTS
Endurance	IEC 60384- 21/22	4.14	<ol> <li>Preconditioning, class 2 only: 150 +0/-10 °C /1 hour, then keep for 24 ±1 hour at room temp</li> <li>Initial measure: Spec: refer initial spec C, D, IR</li> <li>Endurance test: Temperature: NP0/X7R: 125 °C X5R/Y5V: 85 °C</li> <li>Specified stress voltage applied for 1,000 hours: Applied 2.0 × U_r for general product. Applied 1.5 × U_r for high cap. product. High voltage series follows with below stress condition: Applied 1.3 × U_r for 500V series Applied 1.2 × U_r for 1KV, 2KV, 3KV series</li> <li>Recovery time: 24 ±2 hours</li> <li>Final measure: C, D, IR</li> <li>P.S. If the capacitance value is less than the minimum value permitted, then after the other measurements have been made the capacitor shall be precondition according to <i>"IEC 60384 4.1"</i> and then the requirement shall be met.</li> </ol>	No visual damage <b>General purpose series&gt;</b> $\Delta C/C$ Class 1: NP0: within ±2% or 1 pF, whichever is greater Class2: $XSR/X7R: \pm 15\%; Y5V: \pm 30\%$ D.F. Class1: NP0: $\leq 2 \times$ specified value Class2: $XSR/X7R: \leq 16V: \leq 7\%$ $\geq 25V: \leq 5\%$ Y5V: $\leq 15\%$ R _{ins} Class1: NP0: $\geq 4,000 \text{ M}\Omega \text{ or}$ R _{ins} $\times C_r \geq 40$ s whichever is less Class2: $XSR/X7R/Y5V: \geq 1,000 \text{ M}\Omega \text{ or}$ R _{ins} $\propto C_r \geq 50$ s whichever is less <b>High Capacitance series&gt;</b> $\Delta C/C$ Class 2: $XSR/X7R: \pm 20\%; Y5V: \pm 30\%$ D.F. Class 2: $2 \times \text{ initial value max}$ R _{ins} Class 2: $2 \times \text{ initial value max}$ R _{ins} Class 2: $1,000 \text{ M}\Omega \text{ or R}_{\text{ins}} \times C_r \geq 50$ s, whichever is less
Voltage Proof	IEC 60384-1	4.6	Specified stress voltage applied for 1 minute $U_r \le 100 \text{ V}$ : series applied 2.5 $U_r$ $100 \text{ V} < U_r \le 200 \text{ V}$ series applied (1.5 $U_r + 100$ ) $200 \text{ V} < U_r \le 500 \text{ V}$ series applied (1.3 $U_r + 100$ ) $U_r > 500 \text{ V}$ : 1.3 $U_r$ I: 7.5 mA	No breakdown or flashover



<b>YAGEO</b>	Phícomp			Product specification	17
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IAGEU		4C-Array	NP0/X7R/Y5V		17

# <u>REVISION HISTORY</u>

REVISION	DATE	CHANGE NOTIFICATION	DESCRIPTION
Version 3	May 21, 2014	-	- Product range updated
Version 2	Jun. 17, 2013	-	- Product range updated
Version I	Feb 05, 2010	-	- The statement of "Halogen Free" on the cover added
Version 0	Jun 22, 2009	-	- New datasheet for 4C-Array series with RoHS compliant
			- Replace from pdf files: 0508_16V to 50V_1, 0612_16V to 50V_0, C-Array_NP0_50V_0508_7, C-Array_NP0_50V_0612_7, C-Array_X7R_16V_25V_50V_0612_6, C-Array_X7R_16V_0508_5, C-Array_Y5V_25V_0508_0, C-Array_Y5V_25V_0612_5
			- Define global part number
			- Description of "Halogen Free compliant" added
			- Test method and procedure updated



# **Mouser Electronics**

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Yageo:

 CA0612JRNPO9BN101
 CA0612KRX7R7BB104
 CA0612KRX7R7BB473
 CA0612KRX7R8BB473

 CA0612JRNPO9BN220
 CA0612JRNPO9BN471
 CA0612JRNPO9BN470
 CA0612JRNPO9BN221

 CA0612JRNPO9BN331
 CA0612ZRY5V8BB104
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