

DATA SHEET

SURFACE MOUNT MULTILAYER CERAMIC CAPACITORS

High Frequency Automotive Grade

NP0

16 V TO 50 V

0.2 pF to 100 pF

RoHS compliant & Halogen Free



SCOPE

This specification describes Automotive grade NP0 series chip capacitors with lead-free terminations and used for automotive equipments.

APPLICATIONS

All general purpose applications
Entertainment applications
Comfort / security applications
Information applications

FEATURES

- AEC-Q200 qualified
- MSL class: MSL 1
- AC series soldering is compliant with J-STD-020D
- Halogen free epoxy
- RoHS compliant
- Reduce environmentally hazardous waste
- High component and equipment reliability
- The capacitors are 100% performed by automatic optical inspection prior to taping.

ORDERING INFORMATION - GLOBAL PART NUMBER

All part numbers are identified by the series, size, tolerance, TC material, packing style, voltage, process code, termination and capacitance value.

GLOBAL PART NUMBER

AQ XXXX X X XXX X **B** X XXX
(1) (2) (3) (4) (5) (6) (7)

(1) SIZE – INCH BASED (METRIC)

0603 (1608)

(2) TOLERANCE

0.2pF to 2.0pF

A = ± 0.05 pF

B = ± 0.1 pF

C = ± 0.25 pF

2.1pF to 5.0pF

A = ± 0.05 pF

B = ± 0.1 pF

C = ± 0.25 pF

D = ± 0.5 pF

5.1pF to 9.9pF

B = ± 0.1 pF

C = ± 0.25 pF

D = ± 0.5 pF

10pF and over

F = $\pm 1\%$

G = $\pm 2\%$

J = $\pm 5\%$

(3) PACKING STYLE

R = Paper/PE taping reel; Reel 7 inch

P = Paper/PE taping reel; Reel 13 inch

(4) TC MATERIAL

NP0

(5) RATED VOLTAGE

7 = 16 V

8 = 25 V

9 = 50 V

(6) PROCESS

N = NP0

(7) CAPACITANCE VALUE

2 significant digits+number of zeros

The 3rd digit signifies the multiplying factor, and letter R is decimal point

Example: 121 = $12 \times 10^1 = 120$ pF

CONSTRUCTION

The capacitor consists of a rectangular block of ceramic dielectric in which a number of interleaved metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two end terminations and finally covered with a layer of plated tin (Matte Sn). The terminations are lead-free. A cross section of the structure is shown in Fig.1.

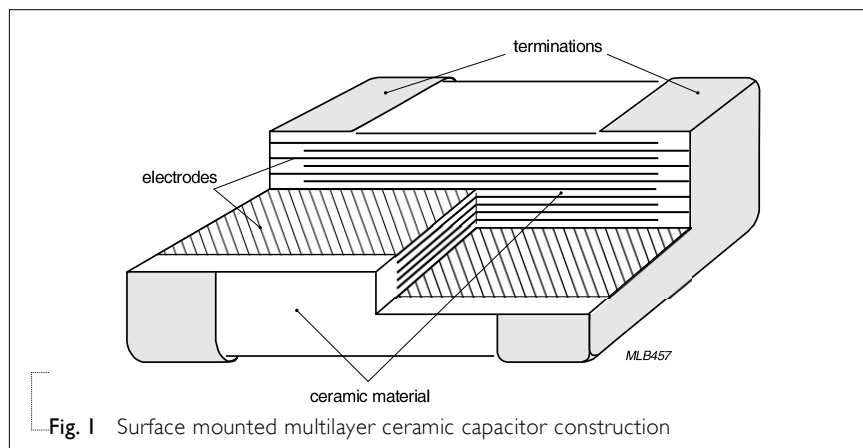


Fig. 1 Surface mounted multilayer ceramic capacitor construction

DIMENSION

Table I For outlines see fig. 2

TYPE	L ₁ (mm)	W (mm)	T (MM)	L ₂ / L ₃ (mm)		L ₄ (mm)
				min.	max.	min.
0603	1.6 ±0.10	0.8 ±0.10	0.8 ±0.10	0.20	0.60	0.40

OUTLINES

For dimension see Table I

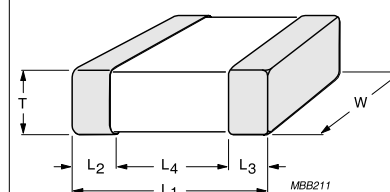


Fig. 2 Surface mounted multilayer ceramic capacitor dimension

CAPACITANCE RANGE & THICKNESS FOR NP0**Table 3** Sizes 0603

CAP.	0603			CAP.	0603		
	16 V	25 V	50 V		16 V	25 V	50 V
0.2 pF	0.8±0.1	0.8±0.1	0.8±0.1	9 pF	0.8±0.1	0.8±0.1	0.8±0.1
0.3 pF	0.8±0.1	0.8±0.1	0.8±0.1	10 pF	0.8±0.1	0.8±0.1	0.8±0.1
0.4 pF	0.8±0.1	0.8±0.1	0.8±0.1	12 pF	0.8±0.1	0.8±0.1	0.8±0.1
0.5 pF	0.8±0.1	0.8±0.1	0.8±0.1	15 pF	0.8±0.1	0.8±0.1	0.8±0.1
0.6 pF	0.8±0.1	0.8±0.1	0.8±0.1	18 pF	0.8±0.1	0.8±0.1	0.8±0.1
0.7 pF	0.8±0.1	0.8±0.1	0.8±0.1	22 pF	0.8±0.1	0.8±0.1	0.8±0.1
0.8 pF	0.8±0.1	0.8±0.1	0.8±0.1	27 pF	0.8±0.1	0.8±0.1	0.8±0.1
0.9 pF	0.8±0.1	0.8±0.1	0.8±0.1	33 pF	0.8±0.1	0.8±0.1	0.8±0.1
1.0 pF	0.8±0.1	0.8±0.1	0.8±0.1	39 pF	0.8±0.1	0.8±0.1	0.8±0.1
1.2 pF	0.8±0.1	0.8±0.1	0.8±0.1	47 pF	0.8±0.1	0.8±0.1	0.8±0.1
1.5 pF	0.8±0.1	0.8±0.1	0.8±0.1	56 pF	0.8±0.1	0.8±0.1	0.8±0.1
1.8 pF	0.8±0.1	0.8±0.1	0.8±0.1	68 pF	0.8±0.1	0.8±0.1	0.8±0.1
2.0 pF	0.8±0.1	0.8±0.1	0.8±0.1	82 pF	0.8±0.1	0.8±0.1	0.8±0.1
2.2 pF	0.8±0.1	0.8±0.1	0.8±0.1	100 pF	0.8±0.1	0.8±0.1	0.8±0.1
2.4 pF	0.8±0.1	0.8±0.1	0.8±0.1				
2.7 pF	0.8±0.1	0.8±0.1	0.8±0.1				
3.0 pF	0.8±0.1	0.8±0.1	0.8±0.1				
3.3 pF	0.8±0.1	0.8±0.1	0.8±0.1				
3.6 pF	0.8±0.1	0.8±0.1	0.8±0.1				
3.9 pF	0.8±0.1	0.8±0.1	0.8±0.1				
4.0 pF	0.8±0.1	0.8±0.1	0.8±0.1				
4.7 pF	0.8±0.1	0.8±0.1	0.8±0.1				
5.0 pF	0.8±0.1	0.8±0.1	0.8±0.1				
5.6 pF	0.8±0.1	0.8±0.1	0.8±0.1				
6.0 pF	0.8±0.1	0.8±0.1	0.8±0.1				
6.8 pF	0.8±0.1	0.8±0.1	0.8±0.1				
7.0 pF	0.8±0.1	0.8±0.1	0.8±0.1				
8.0 pF	0.8±0.1	0.8±0.1	0.8±0.1				
8.2 pF	0.8±0.1	0.8±0.1	0.8±0.1				

NOTE

1. Values in shaded cells indicate thickness class in mm
2. Capacitance value of non E-12 series is on request

THICKNESS CLASSES AND PACKING QUANTITY

Table 13

SIZE CODE	THICKNESS CLASSIFICATION	TAPE WIDTH QUANTITY PER REEL	Ø180 MM / 7 INCH		Ø330 MM / 13 INCH	
			Paper	Blister	Paper	Blister
0603	0.8 ±0.1 mm	8 mm	4,000	---	15,000	---

ELECTRICAL CHARACTERISTICS**NP0 DIELECTRIC CAPACITORS; NI/SIN TERMINATIONS**

Unless otherwise specified, all test and measurements shall be made under standard atmospheric conditions for testing as given in 5.3 of IEC 60068-1:

- Temperature: 15 °C to 35 °C
- Relative humidity: 25% to 75%
- Air pressure: 86 kPa to 106 kPa

Before the measurements are made, the capacitor shall be stored at the measuring temperature for a time sufficient to allow the entire capacitor to reach this temperature.

The period as prescribed for recovery at the end of a test is normally sufficient for this purpose.

Table I4

DESCRIPTION		VALUE
Capacitance range		0.2 pF to 100 µpF
Capacitance tolerance		
NP0	C < 10 pF	±0.05 pF, ±0.1 pF, ±0.25 pF, ±0.5 pF
	C ≥ 10 pF	±1%, ±2%, ±5%
Dissipation factor (D.F.)		
NP0	C < 30 pF	≤ 1 / (400 + 20C)
	C ≥ 30 pF	≤ 0.1 %
Insulation resistance after 1 minute at U _r (DC)		IR ≥ 10 GΩ
Maximum capacitance change as a function of temperature (temperature characteristic/coefficient):		
NP0		±30 ppm/°C
Operating temperature range:		
NP0		-55 °C to +125 °C

SOLDERING RECOMMENDATION

Table 15

SOLDERING METHOD	SIZE 0402	0603	0805	1206	≥ 1210
Reflow	≥ 0.1 μ F	≥ 1.0 μ F	≥ 2.2 μ F	≥ 4.7 μ F	Reflow only
Reflow/Wave	< 0.1 μ F	< 1.0 μ F	< 2.2 μ F	< 4.7 μ F	---

SOLDERING CONDITIONS

The lead free MLCCs are able to stand the reflow soldering conditions as below:

- Temperature: above 220 °C
- Endurance: 95 to 120 seconds
- Cycles: 3 times

The test of "soldering heat resistance" is carried out in accordance with the schedule of "MIL-STD-202F-method 210F", "The robust construction of chip capacitors allows them to be completely immersed in a solder bath of 270 °C for 10 seconds". Therefore, it is possible to mount MLCCs on one side of a PCB and other discrete components on the reverse (mixed PCBs). Surface Mount Capacitors are tested for solderability at 245 °C during 2 seconds. The test condition for no leaching is 260°C for 30 seconds.

TESTS AND REQUIREMENTS

Table 16 Test procedures and requirements

TEST	TEST METHOD		PROCEDURE	REQUIREMENTS
Mounting	IEC 60384-21/22	4.3	The capacitors may be mounted on printed-circuit boards or ceramic substrates	No visible damage
Capacitance	IEC 60384-21/22	4.5.1	Class I: At 20 °C, 24 hours after annealing $f = 1 \text{ MHz}$ for $C \leq 1 \text{ nF}$, measuring at voltage $1 V_{\text{rms}}$ at 20 °C $f = 1 \text{ KHz}$ for $C > 1 \text{ nF}$, measuring at voltage $1 V_{\text{rms}}$ at 20 °C	Within specified tolerance
Dissipation Factor (D.F.)	IEC 60384-21/22	4.5.2	Class I: At 20 °C, 24 hours after annealing $f = 1 \text{ MHz}$ for $C \leq 1 \text{ nF}$, measuring at voltage $1 V_{\text{rms}}$ at 20 °C $f = 1 \text{ KHz}$ for $C > 1 \text{ nF}$, measuring at voltage $1 V_{\text{rms}}$ at 20 °C	In accordance with specification
Insulation Resistance	IEC 60384-21/22	4.5.3	At U_r (DC) for 1 minute	In accordance with specification

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS												
Temperature coefficient	4.6	<p>Capacitance shall be measured by the steps shown in the following table.</p> <p>The capacitance change should be measured after 5 min at each specified temperature stage.</p> <table><tr><th>Step</th><th>Temperature(°C)</th></tr><tr><td>a</td><td>25±2</td></tr><tr><td>b</td><td>Lower temperature±3°C</td></tr><tr><td>c</td><td>25±2</td></tr><tr><td>d</td><td>Upper Temperature±2°C</td></tr><tr><td>e</td><td>25±2</td></tr></table> <p>(1) Class I</p> <p>Temperature Coefficient shall be calculated from the formula as below</p> <p>Temp, Coefficient = $\frac{C2 - C1}{C1 \times \Delta T} \times 10^6$ [ppm/°C]</p> <p>C1: Capacitance at step c</p> <p>C2: Capacitance at 125°C</p> <p>ΔT: 100°C(=125°C-25°C)</p> <p>(2) Class II</p> <p>Capacitance Change shall be calculated from the formula as below</p> <p>ΔC = $\frac{C2 - C1}{C1} \times 100\%$</p> <p>C1: Capacitance at step c</p> <p>C2: Capacitance at step b or d</p>	Step	Temperature(°C)	a	25±2	b	Lower temperature±3°C	c	25±2	d	Upper Temperature±2°C	e	25±2	<General purpose series> Class I: Δ C/C: ±30ppm
Step	Temperature(°C)														
a	25±2														
b	Lower temperature±3°C														
c	25±2														
d	Upper Temperature±2°C														
e	25±2														
High Temperature Exposure	AEC-Q200 3	Unpowered ; 1000hours @ T=150°C Measurement at 24±2 hours after test conclusion.	No visual damage Δ C/C : Class I: NP0: within ±0.5% or 0.5 pF whichever is greater												
Temperature Cycling	AEC-Q200 4	Preconditioning: 150 +0/-10 °C for 1 hour, then keep for 24 ±1 hours at room temperature 1000 cycles with following detail: 30 minutes at lower category temperature 30 minutes at upper category temperature Recovery time 24 ±2 hours	No visual damage ΔC/C Class I: NP0: Within ±1% or 0.5pF, whichever is greater. D.F. meet initial specified value IR meet initial specified value												
Destructive Physical Analysis	AEC-Q200 5	10ea X 3 lots. Note: Only applies to SMD ceramics. Electrical test not required.													

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
Moisture Resistance	AEC-Q200 6	T=24 hrs/per cycle; 10 continuous cycles unpowered. Measurement at 24 ±2 hours after test condition.	No visual damage
			$\Delta C/C$ NP0: Within ±3% or 3 pF, whichever is greater
			D.F. Within initial specified value
			IR NP0: ≥ 10,000 MΩ

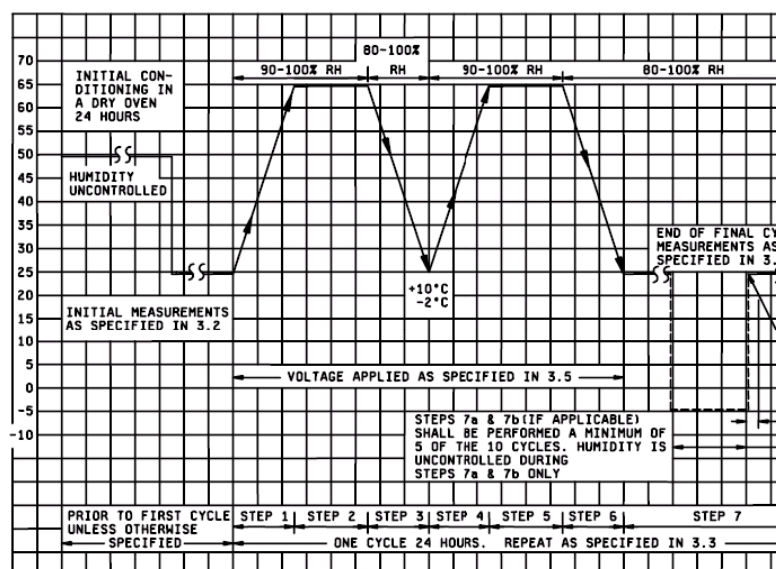
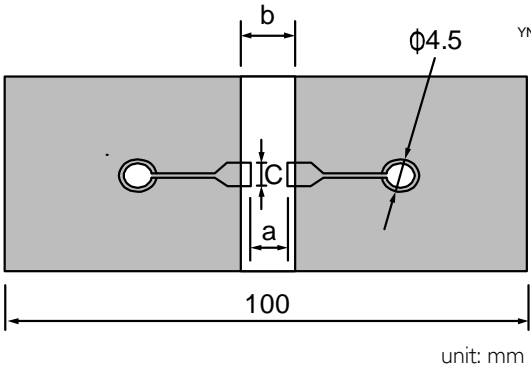


Fig. 4 Moisture resistant

Biased Humidity	AEC-Q200 7	<ol style="list-style-type: none"> Preconditioning, class 2 only: 150 +0/-10 °C /1 hour, then keep for 24 ±1 hour at room temp Initial measure: Parameter: IR Measuring voltage: 1.5V ± 0.1 VDC Note: Series with 100 KΩ & 6.8 KΩ Test condition: 85 °C, 85% R.H. connected with 100 KΩ resistor, applied 1.5V/U_r for 1,000 hours. Recovery: Class I: 6 to 24 hours Class 2: 24 ±2 hours Final measure: IR 	<p>No visual damage after recovery</p> <p>Initial requirement: Class I: - Connected to 100 KΩ: C ≤ 10 nF: I.R ≥ 10,000 MΩ or C > 10 nF: (I.R-100 KΩ) × C ≥ 100s. - Connected to 6.8 KΩ: C ≤ 10 nF: I.R ≥ 10,000 MΩ or C > 10 nF: (I.R-6.8 KΩ) × C ≥ 100s.</p> <p>Final measurement: The insulation resistance shall be greater than 0.1 time initial value.</p>
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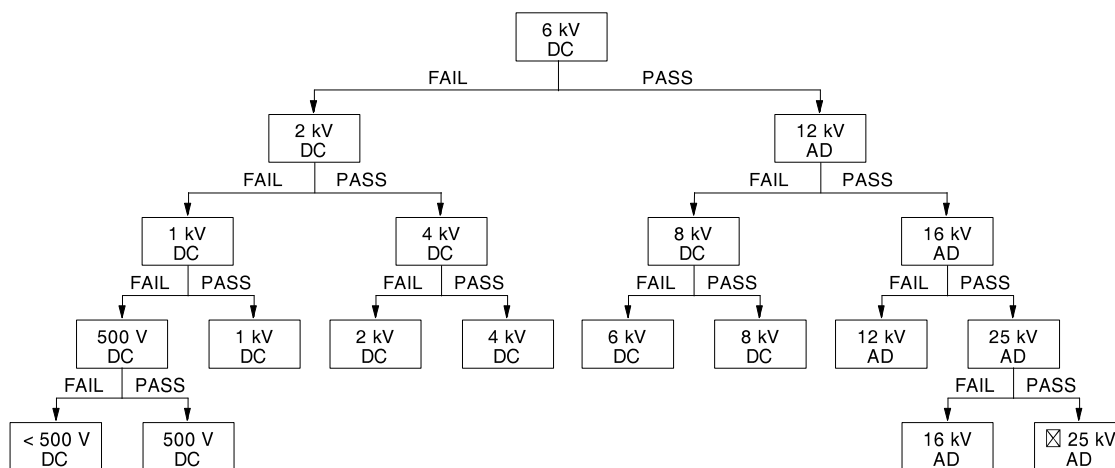
TEST	TEST METHOD		PROCEDURE	REQUIREMENTS
Operational Life	AEC-Q200	8	<p>1. Preconditioning, class 2 only: 150 +0/-10 °C /1 hour, then keep for 24 ± 1 hour at room temp</p> <p>2. Initial measure: Spec: refer to initial spec C, D, IR</p> <p>3. Endurance test: Specified stress voltage applied for 1,000 hours: Applied $2.0 \times U_r$ for general products</p> <p>4. Recovery time: 24 ± 2 hours</p> <p>5. Final measure: C, D, IR</p> <p>Note: If the capacitance value is less than the minimum value permitted, then after the other measurements have been made the capacitor shall be preconditioned according to "IEC 60384 4.1" and then the requirement shall be met.</p>	<p>No visual damage</p> <hr/> <p>$\Delta C/C$ NP0: Within ±2% or 1 pF, whichever is greater</p> <hr/> <p>D.F. NP0: $\leq 2 \times$ specified value.</p> <hr/> <p>IR NP0: $\geq 4,000 \text{ M}\Omega$ or $\text{IR} \times C_r \geq 40\text{s}$ whichever is less</p>
External Visual	AEC-Q200	9	Any applicable method using $\times 10$ magnification	In accordance with specification
Physical Dimension	AEC-Q200	10	Verify physical dimensions to the applicable device specification.	In accordance with specification
Mechanical Shock	AEC-Q200	13	<p>Three shocks in each direction shall be applied along the three mutually perpendicular axes of the test specimen (18 shocks)</p> <p>Peak value: 1,500 g's</p> <p>Duration: 0.5 ms</p> <p>Velocity change: 15.4 ft/s</p> <p>Waveform: Half-sin</p>	<p>$\Delta C/C$ NP0: Within ±0.5% or 0.5 pF, whichever is greater</p> <hr/> <p>D.F. Within initial specified value</p> <p>IR Within initial specified value</p>
Vibration	AEC-Q200	14	<p>5 g's for 20 minutes, 12 cycles each of 3 orientations.</p> <p>Note: Use 8" x 5" PCB. 0.31" thick 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point.</p> <p>Test from 10-2000 Hz.</p>	<p>$\Delta C/C$ NP0: Within ±0.5% or 0.5 pF, whichever is greater</p> <hr/> <p>D.F: meet initial specified value</p> <p>IR meet initial specified value</p>
Resistance to Soldering Heat	AEC-Q200	15	<p>Precondition: 150 +0/-10 °C for 1 hour, then keep for 24 ± 1 hours at room temperature</p> <p>Preheating: for size ≤ 1206: 120 °C to 150 °C for 1</p>	Dissolution of the end face plating shall not exceed 25% of the length of the edge concerned

TEST	TEST METHOD		PROCEDURE	REQUIREMENTS
			minute Preheating: for size >I206: 100 °C to 120 °C for 1 minute and 170 °C to 200 °C for 1 minute Solder bath temperature: 260 ±5 °C Dipping time: 10 ±0.5 seconds Recovery time: 24 ±2 hours	ΔC/C Class I: NP0: Within ±1% or 0.5 pF, whichever is greater. D.F. within initial specified value IR within initial specified value
Thermal Shock	AEC-Q200	16	1. Preconditioning, class 2 only: 150 +0/-10 °C /1 hour, then keep for 24 ±1 hour at room temp 2. Initial measure: Spec: refer to initial spec C, D, IR 3. Rapid change of temperature test: NP0: -55 °C to +125 °C; 300 cycles 15 minutes at lower category temperature; 15 minutes at upper category temperature. 4. Recovery time: Class1: 6 to 24 hours Class2: 24 ±2 hours 5. Final measure: C, D, IR	No visual damage ΔC/C NP0: Within ±1% or 1 pF, whichever is greater D.F: meet initial specified value IR meet initial specified value
ESD	AEC-Q200	17	Per AEC-Q200-002	A component passes a voltage level if all components stressed at that voltage level pass.
Solderability	AEC-Q200	18	Preheated to a temperature of 80 °C to 140 °C and maintained for 30 seconds to 60 seconds. Test conditions for lead containing solder alloy Temperature: 235 ±5 °C Dipping time: 2 ±0.2 seconds Depth of immersion: 10 mm Alloy Composition: 60/40 Sn/Pb Number of immersions: 1 Test conditions for lead-free containing solder alloy Temperature: 245 ±5 °C Dipping time: 3 ±0.3 seconds Depth of immersion: 10 mm Alloy Composition: SAC305 Number of immersions: 1	The solder should cover over 95% of the critical area of each termination.
Electrical Characterization	AEC-Q200	19	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures. Class I: NP0: -55 °C to +125 °C Normal temperature: 20 °C	ΔC/C Class I: NP0: ±30 ppm/°C

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
Board Flex	AEC-Q200 21	<p>Part mounted on a 100 mm X 40 mm FR4 PCB board, which is 1.6 ± 0.2 mm thick and has a layer-thickness $35 \mu\text{m} \pm 10 \mu\text{m}$.</p> <p>Part should be mounted using the following soldering reflow profile.</p> <p>Conditions:</p> <p>Class I:</p> <p>Bending 3 mm at a rate of 1 mm/s, radius jig 340 mm</p> <p>Test Substrate:</p> 	<p>No visible damage</p> <p>$\Delta C/C$</p> <p>Class I:</p> <p>NP0: Within $\pm 1\%$ or 0.5 pF, whichever is greater</p>
Terminal Strength	AEC-Q200 22	<p>With the component mounted on a PCB obtained with the device to be tested, apply a 17.7N (1.8Kg) force to the side of a device being tested.</p> <p>This force shall be applied for 60+1 seconds.</p> <p>Also the force shall be applied gradually as not to apply a shock to the component being tested.</p> <p>* Apply 2N force for 0402 size.</p>	<p>Magnification of 20X or greater may be employed for inspection of the mechanical integrity of the device body, terminals and body/terminal junction.</p> <p>Before, during and after the test, the device shall comply with all electrical requirements stated in this specification.</p>
Beam Load Test	AEC-Q200 23	<p>Place the part in the beam load fixture. Apply a force until the part breaks or the minimum acceptable force level required in the user specification(s) is attained.</p>	<p>≤ 0805</p> <p>Thickness $> 0.5\text{mm}$: 20N</p> <p>Thickness $\leq 0.5\text{mm}$: 8N</p> <p>≥ 1206</p> <p>Thickness $\geq 1.25\text{ mm}$: 54N</p> <p>Thickness $< 1.25\text{ mm}$: 15N</p>
Voltage Proof		<ol style="list-style-type: none"> Specified stress voltage applied for 1~5 seconds $U_r \leq 100\text{ V}$: series applied $2.5 U_r$ $100\text{ V} < U_r \leq 200\text{ V}$ series applied $(1.5 U_r + 100)$ $200\text{ V} < U_r \leq 500\text{ V}$ series applied $(1.3 U_r + 100)$ $U_r > 500\text{ V}$: $1.3 U_r$ $U_r \geq 1000\text{ V}$: $1.2 U_r$ <p>Charge/Discharge current is less than 50 mA</p>	No breakdown or flashover

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
ESR		Measuring frequency: $1 \pm 0.2\text{GHz}$ at room temperature.	$0.2\text{pF} \leq C \leq 1\text{pF} : 350\text{m}\Omega / C \text{ max}$ $1\text{pF} < C \leq 5\text{pF} : 300\text{m}\Omega \text{ max}$ $5\text{pF} < C \leq 10\text{pF} : 250\text{m}\Omega \text{ max}$ $C : \text{Nominal cap (pF)}$
		Measuring frequency: $500 \pm 50\text{MHz}$ at room temperature.	$10\text{pF} < C \leq 100\text{pF} : 400\text{m}\Omega \text{ max}$

YNM0053-1



Note: Classify the components according to the highest ESD voltage level survived during ESD testing.

Fig. 5 Passive component HBM ESD test flow diagram (DC = Direct Contact Discharge, AD = Air Discharge)

REVISION HISTORY

REVISION	DATE	CHANGE NOTIFICATION	DESCRIPTION
Version 0	Dec. 14, 2018	-	- New

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[AQ0603ARNPO9BNR70](#) [AQ0603ARNPO9BNR80](#) [AQ0603ARNPO9BNR90](#) [AQ0603BRNPO9BNR60](#)
[AQ0603BRNPO9BNR70](#) [AQ0603ARNPO9BN1R0](#)