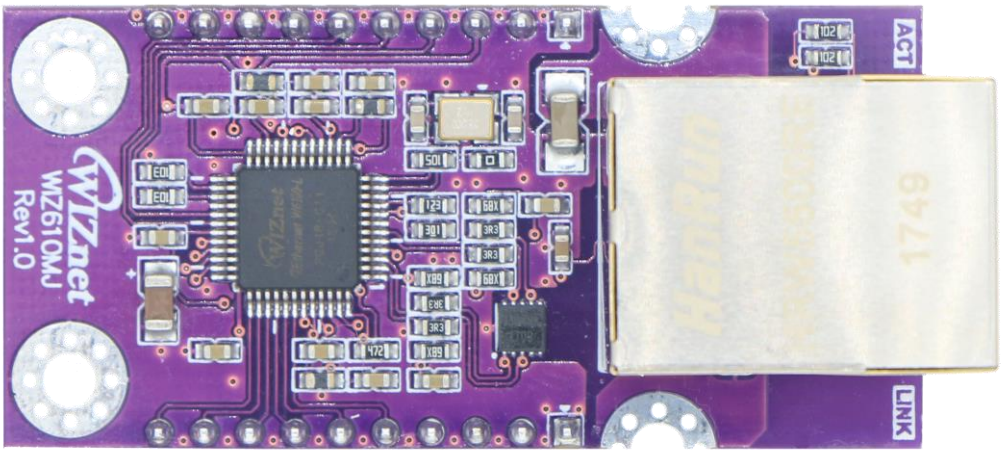
WIZ610MJ Datasheet

(Version 1.0)



☞ For more information, visit our website at http://www.wiznet.io

Document Revision History

Date	Revision	Changes
2019-2-15	V1.0	Official Release

1. Introduction

WIZ610MJ is the network module that includes W6100 (TCP/IP hardwired chip, include PHY), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W6100 and Transformer.
The WIZ610MJ is an ideal option for users who want to develop their Internet enabling systems rapidly.

For the detailed information on implementation of Hardware TCP/IP, refer to the W6100 Datasheet.

WIZ610MJ consists of W6100 and MAG-JACK.

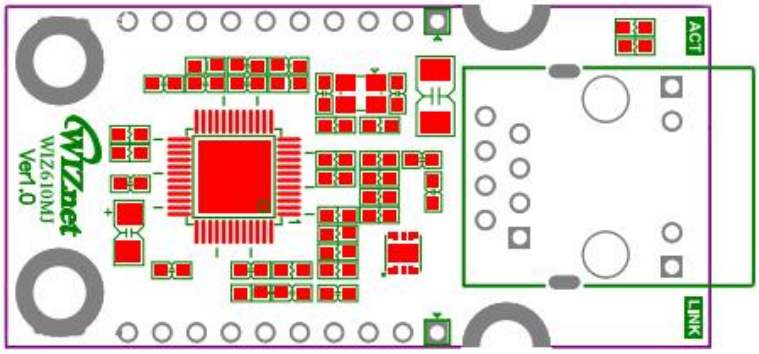
- TCP/IP, Ethernet MAC : W6100
- Ethernet PHY : Included in W6100
- Connector : MAG-JACK(RJ45 with Transformer)

1.1 Feature

- Support Hardwired TCP/IP Protocols : TCP, UDP, IPv6, IPv4, ICMPv6, ICMPv4, IGMP, MLDv1, ARP, PPPoE
- Support IPv4/IPv6 Dual Stack
- Support 8 independent SOCKETs simultaneously with 32KB Memory
- Support SOCKET-less Command:
  ARP, PING, ICMPv6(PING, ARP,DAD,NA,RS) Command for IPv6 Auto-configuration& Network Monitoring
- Support Ethernet Power Down Mode & Main Clock Switching for power save
- Support Wake on LAN over UDP
- Support Serial & Parallel Host Interface: High Speed SPI(MODE 0/3), System Bus with 2 Address signal & 8bit Data
- Internal 16Kbytes Memory for TX/ RX Buffers
- 10BaseT/100BaseTX Ethernet PHY Integrated
- Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- Support Auto-MDIX only on Auto-Negotiation Mode
- 3V operation with 5V I/O signal tolerance
- Network Indicator LEDs (Full/Half Duplex, Link, 10/100 Speed, Active)
- Interfaces with two 2.54mm pitch 1 x 10 header pin
- Temperature : -40 ~ 85℃(Operation)

2. Pin assignment & description

2.1 Pin assignment



2.2 Pin description

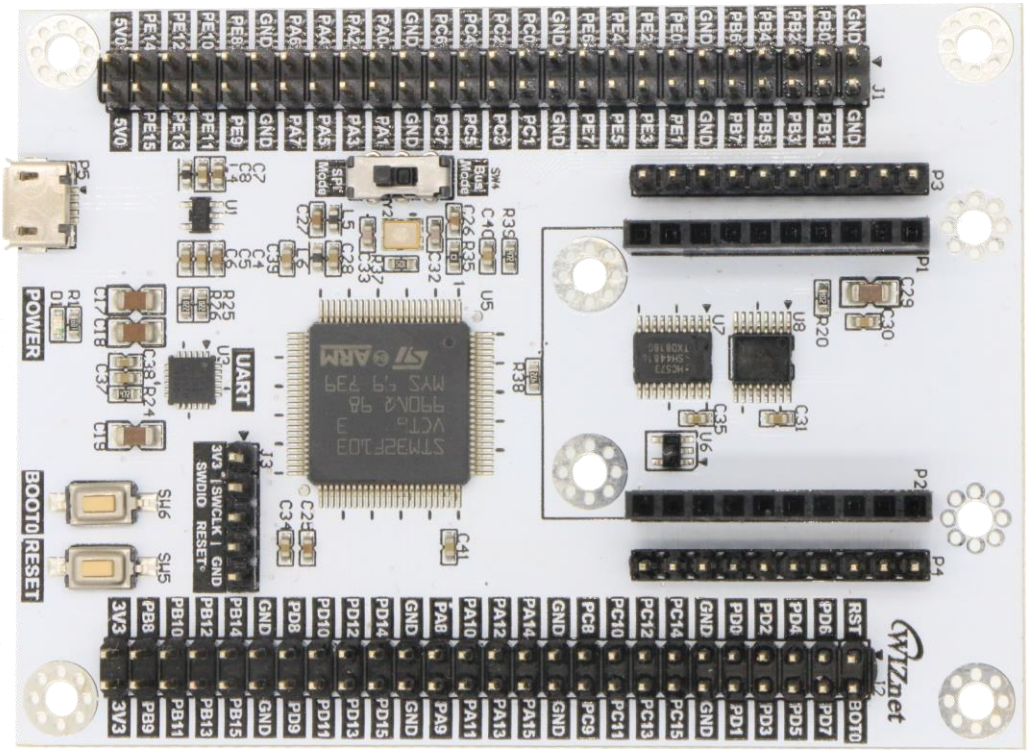
Pin Type Notation

Type	Description
I	Input
O	Output
I/O	Input / Output
P	Power & Ground

Symbol	Type	Pin No.	Description
MODE	**I**	JP2:4	**W6100 Interface Mode Selection.** Interface Mode is selected by MOD [3:0]. “0000”: SPI Mode. “010X”: Parallel Bus Mode.
CS	**I**	**JP2:5**	**W6100 Chip Select** Low : Select High : No Select
CLK	**I**	**JP2:6**	**SPI Clock** On SPI Mode, it is used to SPI Clock. But on Parallel Bus Mode, it must be connected to GND or be floated.

MOSI/ A0	**I**	**JP2:7**	**SPI Master Output Slave Input / Address 0** MOSI: On SPI Mode, SPI Data is received from HOST. ADDR0: On Parallel Bus Mode, it is used to Address 0.
MISO/ A1	**I/O**	**JP2:8**	**SPI Master Input Slave Output / Address 1** MISO: On SPI Mode, SPI Data is transmitted to HOST. ADDR1: On Parallel Bus Mode, It is used to Address 1.
RDn	**I**	JP2:9	**Read Strobe** On Parallel Bus Mode, it indicates Read Operation. On SPI Mode, it must be connected to 3V3D or be floated.
WRn	**I**	JP2:10	**Write Strobe** On Parallel Bus Mode, it indicates Write Operation.
D7~D0	**I/O**	JP1:10 JP1:9 JP1:8 JP1:7 JP1:6 JP1:5 JP1:4 JP1:3	**8 Bits Data Bus** On Parallel Bus Mode, DAT [7:0] receives Data from HOST or W6100. On SPI Mode, DAT [7:0] must be floated.
INTn	**O**	JP1:2	**Interrupt** When the event occurs during W6100 Ethernet Communication, INTn notices to HOST. Low : Interrupt Occurred High : No Interrupt Refer to IEN (Interrupt pin Enable) in MR2 (Mode Register 2), INTPTMR (Interrupt Pending Time Register), IMR (Interrupt Mask Register), IMR2 (Interrupt Mask Register 2), SLIMR (SOCKET-less Interrupt Mask Register)
RSTn	**I**	JP1:1	**Reset** RSTn initializes W6100. RSTn must be asserted to Low longer than 500ns. After asserted RSTn, W6100 spends 60.3ms for initialization. Low : W6100 initialized. High : Normal Operation.

2.2.1 WIZ810SMJ-EVB Pin assignment



***COMMENT**: P1/P2/P3/P4 have the same function, both arduino compatible with WIZ610MJ, J1,J2 expansion 80 GPIOs (Include analog Peripheral using 12bit ADC).

2.2.2 WIZ810SMJ-EVB Pin description

Symbol	Type	Pin No.	Description
3V3	**p**	J2:0-J2:1	**3.3v power**
PB8-PB15	**I/O**	J2:2-J2:9	**GPIO**
GND	**P**	J2:10-J2:11	**Ground**
PD8-PD15	**I/O**	J2:12-J2:19	**GPIO**
GND	**P**	J2:20-J2:21	**Ground**
PA8-PA15	**I/O**	J2:22-J2:29	**GPIO**

GND	**P**	J2:30-J2:31	**Ground**
PC8-PC15	**I/O**	J2:32-J2:39	**GPIO**
GND	**P**	J2:40-J2:41	**Ground**
PD0-PD7	**I/O**	J2:42-J2:49	**GPIO**
RST	**I**	J2:50	**Reset** RSTn initializes W5100S. RSTn must be asserted to Low longer than 500ns. After asserted RSTn, W5100S spends 60.3ms for initialization. Low : W5100S initialized. High : Normal Operation.
BOOT0	**I**	J2:51	**BOOT0** Power on and enter BootLoader mode.
GND	**P**	J1:0-J1:1	**Ground**
PB0-PB7	**I/O**	J1:2-J1:9	**GPIO**
GND	**P**	J1:10-J1:11	**Ground**
PE0-PE7	**I/O**	J1:12-J1:19	**GPIO**
GND	**P**	J1:20-J1:21	**Ground**
PC0-PC7	**I/O**	J1:22-J1:29	**GPIO**
GND	**P**	J1:30-J1:31	**Ground**
PA0-PA7	**I/O**	J1:32-J1:39	**GPIO**
GND	**P**	J1:40-J1:41	**Ground**
PE8-PE15	**I/O**	J1:42-J1:49	**GPIO**

5V0	**P**	J1:50- J1:51	**5.0V Power**

2.3 Power & Ground

Symbol	Type	Pin No.	Description
VCC	P	JP2:3	Power : 3.3 V power supply
GND	P	JP2:1, JP2:2	Ground

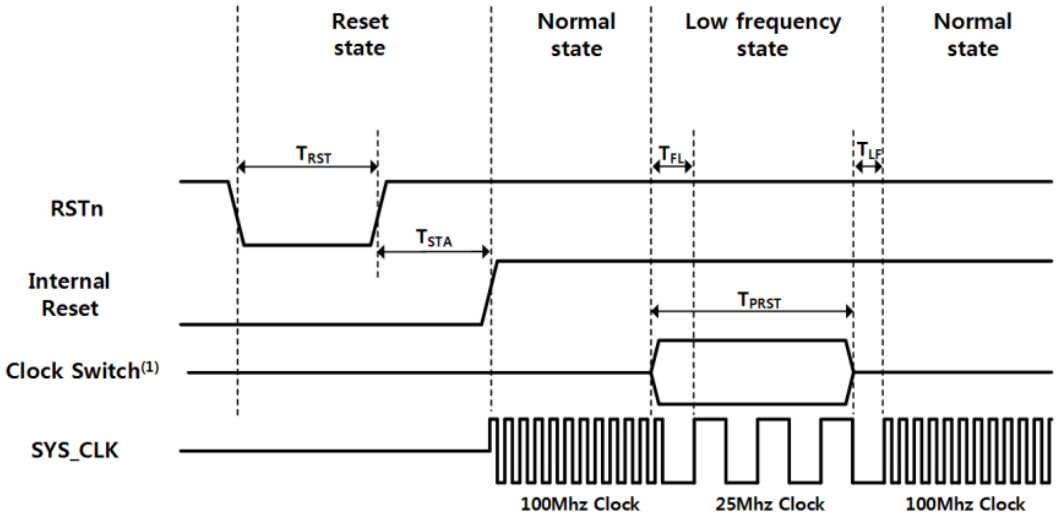
3. Timing diagram

WIZ610MJ provides following interfaces of W6100.

-. Parallel bus access

-. SPI access

3.1 Reset Timing



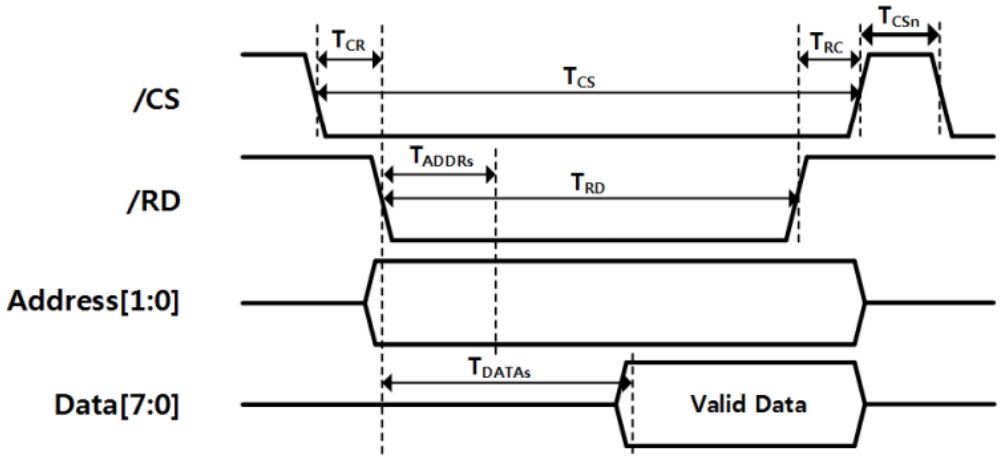
Symbol	Description	Min	Typ	Max
T_{RST}	Reset Time	210 ns	330ns	560ns-
T_{STA}	Stable Time	-		60.3 ms
T_{FI}	Fast to Low Time by MR2[CLKSEL] 1	100ns		-
T_{FI}	Fast to Low Time by PHYCR1[Reset] or PHYCR1[PWDN]	300ns		

T_{PRST}	PHY Auto Reset Time	0.6ms		-
T_{PRST}	PHY Power Down Time	200us		
T_{PRST}	Clock Switch Time	200ns		
T_{LF}	Low to Fast Time by MR2[CLKSEL]	100ns		-
T_{LF}	Low to Fast Time by PHYCR1[Reset] or PHYCR1[PWDN]	100ns		

***COMMENT**: PHY Power-down Mode has TFI and TLF (In PHY Power-down Mode, SYS_CLK switches to Low Clock. After TFI, User can be disable PHY Power-down Mode.)

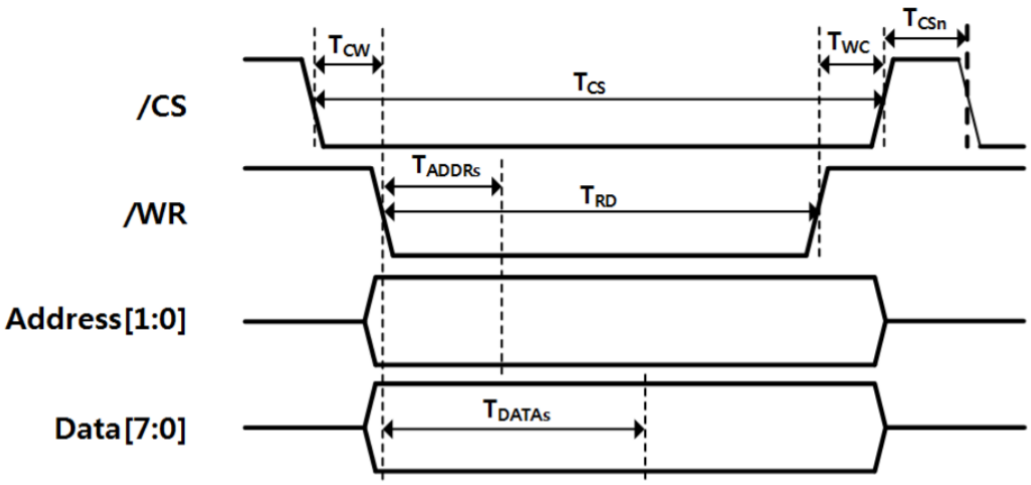
***CAUTION**: User must not set PHY Auto Reset and PHY Power-down Mode at the same time

3.2 BUS Access Read Timing



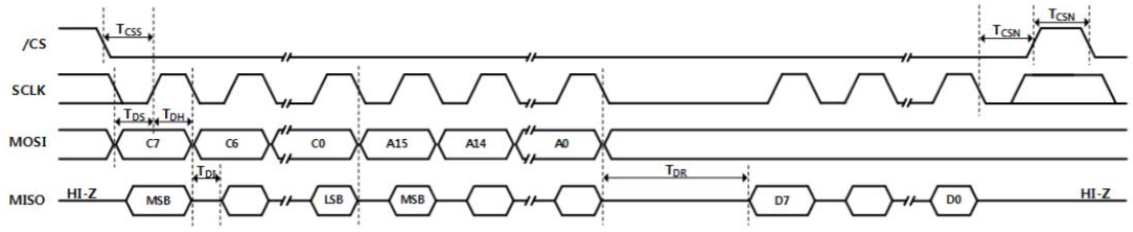
Symbol	Description	Min	Max
T_{ADDRs}	Address Setup Time	SYS_CLK	
T_{CR}	/CS Low to /RD Low Time	0 ns	
Tcs	/CS Low Time	4 SYS_CLK	
T_{RC}	/RD High to /CS High Time	0ns	
Tcsn	/CS Next Assert Time	2 SYS_CLK -	
T_{RD}	/RD Low Time	4 SYS_CLK -	
T_{DATAs}	DATA Setup Time		3 SYS_CLK

3.3 BUS Access Write Timing



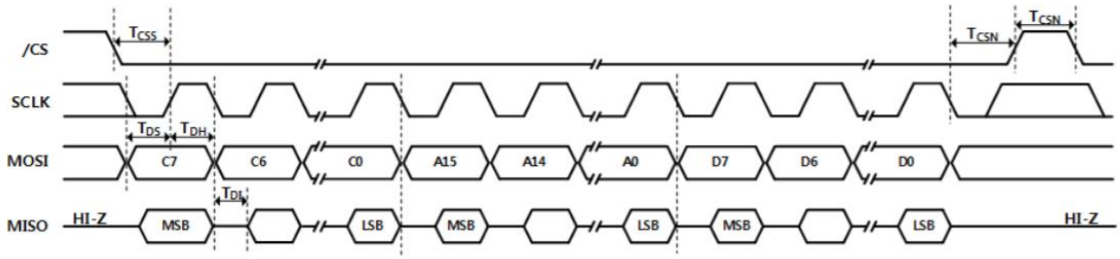
Symbol	Description	Min	Max
T_{ADDRs}	Address Setup Time	SYS_CLK	
T_{CW}	/CS Low to /WR Low Time	0 ns	
Tcs	/CS Low Time	4 SYS_CLK	
T_{WC}	/WR High to /CS High Time	0ns	
Tcsn	/CS Next Assert Time	2 SYS_CLK -	
T_{WR}	/WR Low Time	4 SYS_CLK -	
T_{DATAs}	DATA Setup Time	2 SYS_CLK	

3.4 SPI Access Read Timing



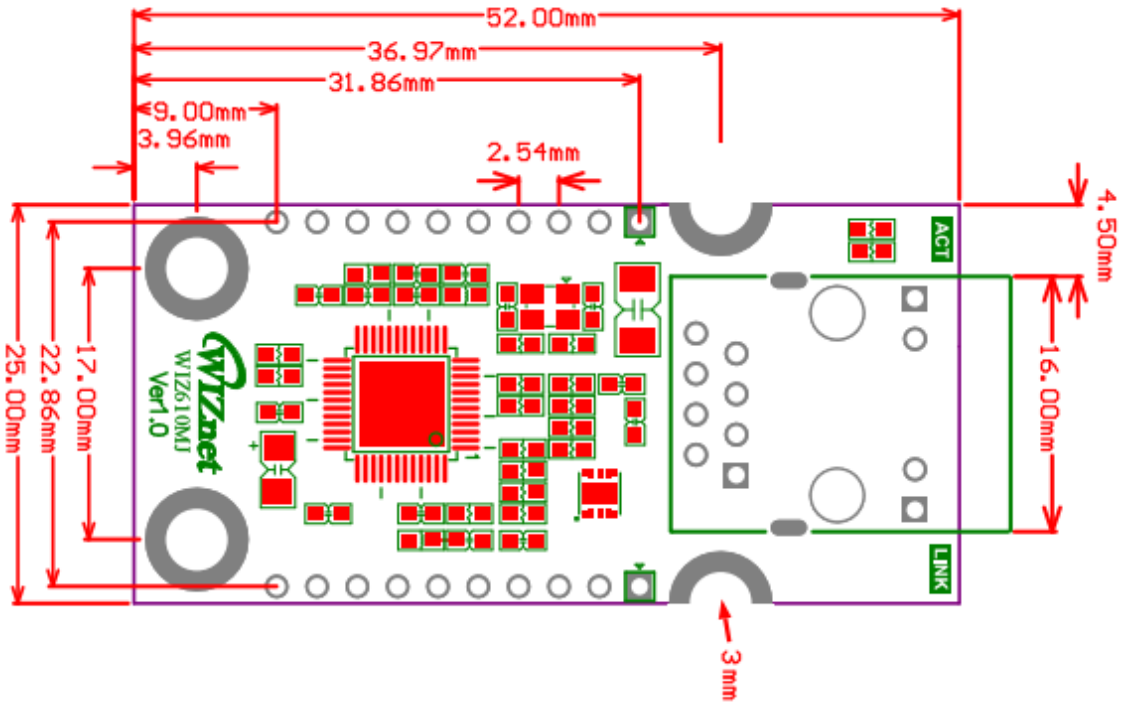
Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency		70	MHz
T_{CSS}	SCSn Setup Time	3 SYS_CLK		ns
T_{CSN}	SCSn Next Time	2 SYS_CLK		ns
T_{DS}	Data In Setup Time	3		ns
T_{DH}	Data In Hold Time	3		ns
T_{DI}	Data Invalid Time	7		ns
T_{DR}	Data Ready Time	6 SYS_CLK+30		ns

3.5 SPI Access Write Timing



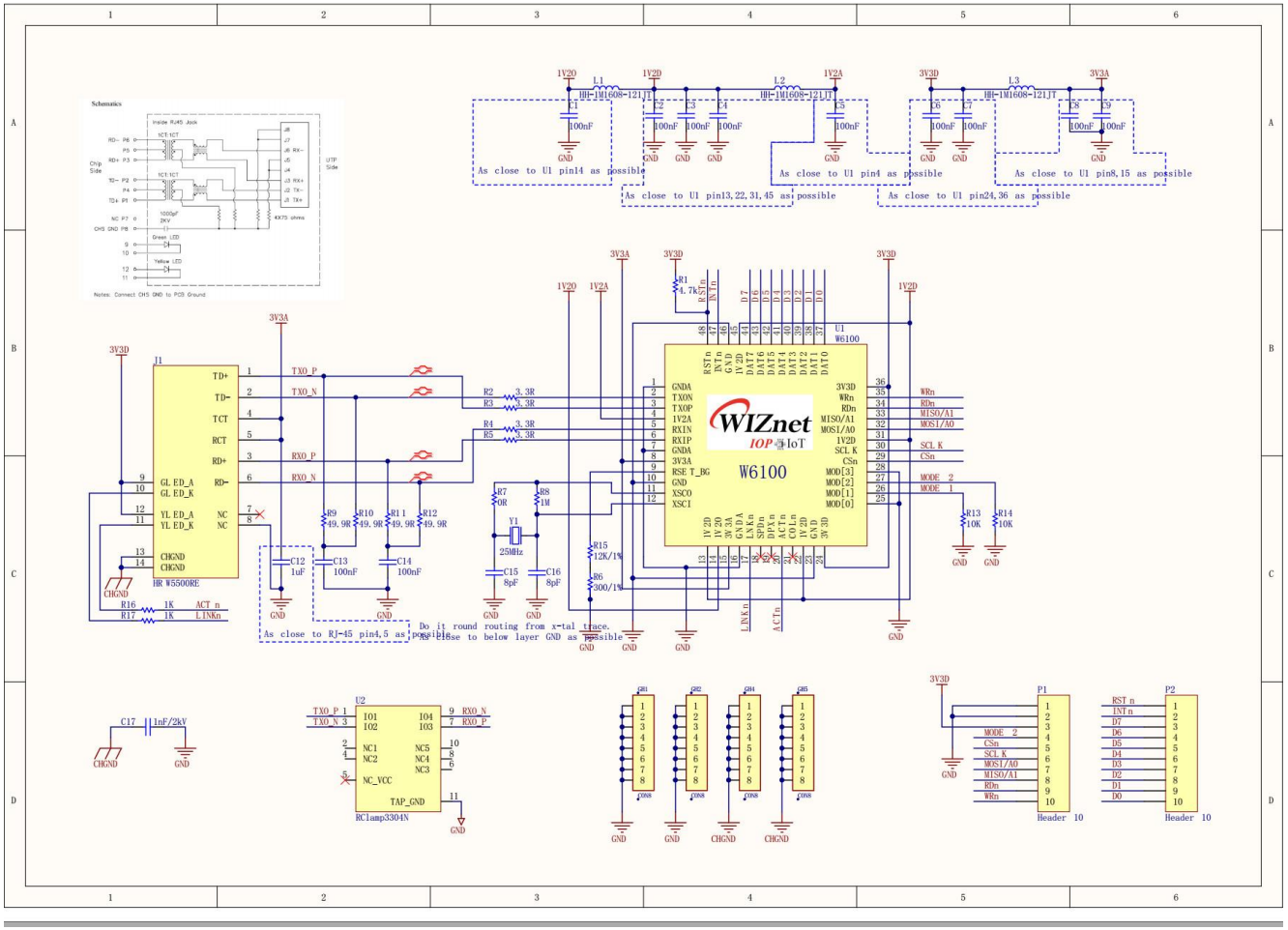
Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency		70	MHz
T_{CSS}	SCSn Setup Time	3 SYS_CLK		ns
T_{CSN}	SCSn Next Time	2 SYS_CLK		ns
T_{DS}	Data In Setup Time	3		ns
T_{DH}	Data In Hold Time	3		ns
T_{DI}	Data Invalid Time	7		ns

4. Dimensions



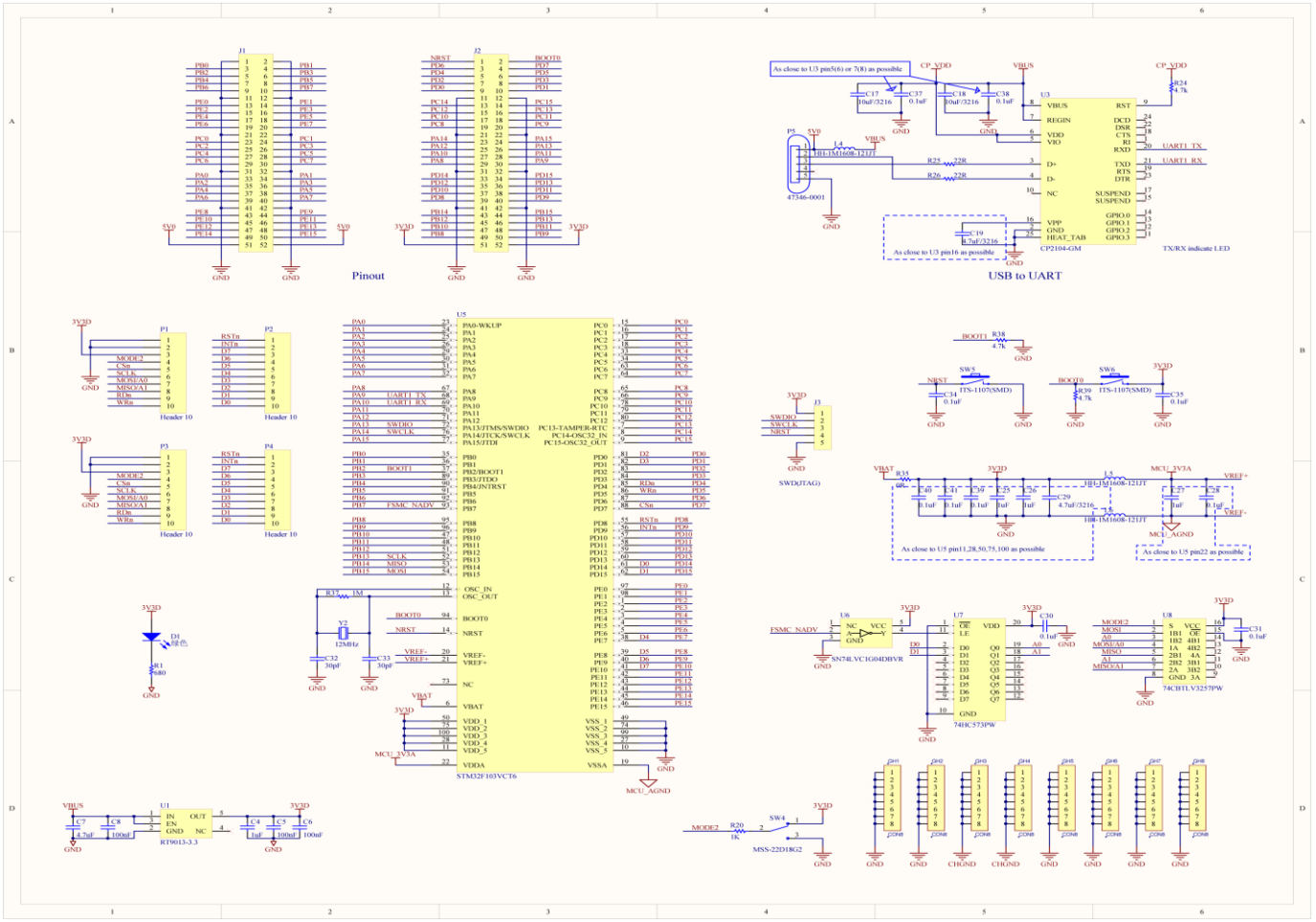
5. Reference Schematics

5.1 WIZ810SMJ Schematics



Comment	Description	Designator	Footprint	Quantity
100nF	Ceramic CAP 0603(1608)	C1, C2, C3, C4, C5, C6, C7, C8, C9, C13,C14	0603-C	11
1uF	Ceramic CAP 0603(1608)	C12	0603-C	1
8pF	Ceramic CAP 0603(1608)	C15, C16	0603-C	2
1nF/2kV	Ceramic CAP 1808(4520)	C17	CAP-1808	1
CON8		GH1, GH2,GH3,GH4	Positioning hole(with small hole)	4
HRW5500RE		J1	RJ-45(HRW5500RE)	1
120R FB	Inductor 0603(1608)	L1, L2, L3	0603-L	3
Header 10	Header,10-pin	P1, P2	HDR1X10	2
4.7k	RES0603	R1	0603-R	1
3.3R	RES0603	R2, R3, R4, R5	0603-R	4
300/1%	RES0603	R6	0603-R	1
0R	RES0603	R7	0603-R	1
1M	RES0603	R8	0603-R	1
49.9R	RES0603	R9, R10, R11, R12	0603-R	4
10K	RES0603	R13, R14	0603-R	2
12K/1%	RES0603	R15	0603-R	1
1K	RES0603	R16, R17	0603-R	2
W6100	WIZnet Hardwired TCP/IP Chip	U1	WIZNET W6100 QFN&TOFP	1
RClamp3304N	Ethernet 3.3V TVS diode, Semtech,SLP2626P10	U2	DFN-10	1

5.2 WIZ810SMJ-EVB Schematics



Comment	Description	Designator	Footprint	Quantity
Cap	Capactior	C4, C5, C6,C7, C8	CAP-0603	5
10uF/3216	Ceramic CAP 1206(3216)	C17,C18	CAP-1206	2
4.7uF/3216	Ceramic CAP 1206(3216)	C19, C29	CAP-1206	2
1uF	Ceramic CAP 0603(1608)	C25,C26,C27	CAP-0603	3
0.1uF	Ceramic CAP 0603(1608)	C28,C30,C31,C34,C35, C37,C38,C39,C40,C41	CAP-0603	10
30pF	Ceramic CAP 0603(1608)	C32,c33	CAP-0603	2
Green	Typical RED GaAs LED	D1	0603-d	1
CON8		GH1, GH2, GH3, GH4, GH5, GH6, GH7, GH8	Positioning hole (with small hole)	8
2.54mm 2x26 Pin Header DIP	2.54mm 2x26 Pin Header DIP	J1, J2	IDC-2X26	2
2.54mm 1x5 Pin Header DIP	2.54mm 1x5 Pin Header DIP	J3	IDC-1X5	1
HH-1M1608-121JT	Inductor 0603(1608)	L4, L5,L6	IND-0603	3
Header 10	Header 10-Pin	P1,P2,P3,P4	HDR1X10	4
47346-0001	Micro USB B Connector SMD	P5	USB-MOLEX-47346	1
Res1	Resitor	R1	RES-0603	1
1K	RES-0603	R20	RES-0603	1
4.7K	RES-0603	R24, R38,R39	RES-0603	3
22R	RES-0603	R25,R26	RES-0603	2
0R	RES-0603	R35	RES-0603	1
1M	RES-0603	R37	RES-0603	1
MSS-22D18G2	Slide Switch	SW4	Toggle switch, double row	1
ITS-1107(SMD)	X-tal 25MHz,3.2x2.5 SMD	SW5,SW6	IT-1107(SMD)	2
RT9013-3.3		U1	QOT-23-5	1
CP2104-GM	SINGLE-CHIP USB-TO-UART BRIDGE	U3	QFN24(0.5/4X4)	1
STM32F103VCT6	STM32 ARM-based 32-bit MCU with 64K bytes Flash,100-pin LOFP ,Industrial Temperature	U5	LQFP100(0.5/16.0)	1
SN74LVC1G04DBVR	Singal Inverter Gate	U6	SOT-23-5L	1
74HC573PW	Octal3-State Non-Inverting Transparent Latch witch Lsttl-Compatible Inputs	U7	TSSOP16(0.65/6.4)	1
74CBTLV3257PW	Quad 1-of-2 Multiplexer/demultiplexer	U8	TSSOP16(0.65/6.4)	1
12MHz	X-tal 12MHz,3.2x2.5 SMD	Y2	OSC-82J0626	1

6. Warranty

WIZnet Co., Ltd. offers the following limited warranties applicable only to the original purchaser. This offer is non-transferable.

WIZnet warrants our products and its parts against defects in materials and workmanship under normal use for period of standard ONE(1) YEAR for the WIZ610MJ module and labor warranty after the date of original retail purchase. During this period, WIZnet will repair or replace a defective products or part free of charge.

Warranty Conditions:

1. The warranty applies only to products distributed by WIZnet or our official distributors.
2. The warranty applies only to defects in material or workmanship as mentioned above in
3. Warranty. The warranty applies only to defects which occur during normal use and does not extend to damage to products or parts which results from alternation, repair, modification, faulty installation or service by anyone other than someone authorized by WIZnet ; damage to products or parts caused by accident, abuse, or misuse, poor maintenance, mishandling, misapplication, or used in violation of instructions furnished by us ; damage occurring in shipment or any damage caused by an act of God, such as lightening or line surge.

Procedure for Obtaining Warranty Service

1. Contact an authorized distributors or dealer of WIZnet for obtaining an RMA (Return Merchandise Authorization) request form within the applicable warranty period.
2. Send the products to the distributors or dealers together with the completed RMA request form. All products returned for warranty must be carefully repackaged in the original packing materials.
3. Any service issue, please contact to sales@wiznet.io

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

WIZnet:
WIZ610MJ