WIZ810Sio User Manual

(Version 1.0)

☞ For more information, visit our website at http://www.wiznet.io

Document Revision History

Date	Revision	Changes
2018-12-28	V1.0	Official Release

Contents

1. Introduction

WIZ810Sio is the internet offload network module that includes W5100S (TCP/IP hardwired chip, include PHY), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W5100S and Transformer.

The WIZ810Sio is an ideal option for users who want to develop their Internet enabling systems rapidly.

For the detailed information on implementation of Hardware TCP/IP, refer to the W5100S Datasheet.

WIZ810Sio consists of W5100S and MAG-JACK.

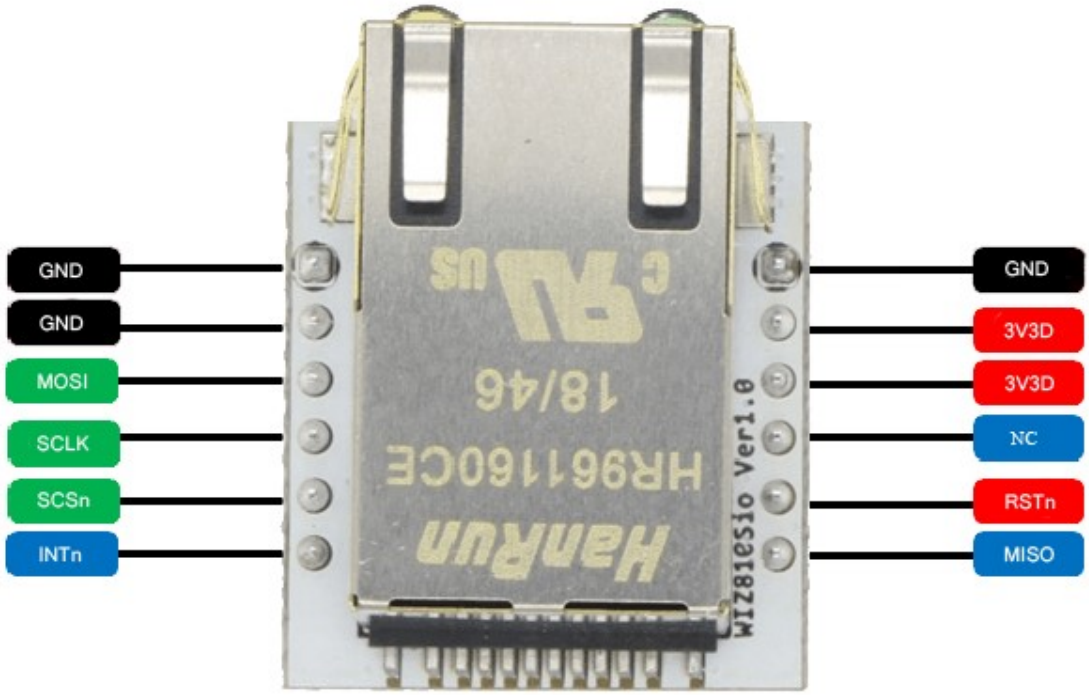
- TCP/IP, Ethernet MAC : W5100S
- Ethernet PHY : Included in W5100S
- Connector : MAG-JACK(RJ45 with Transformer)

1.1. Feature

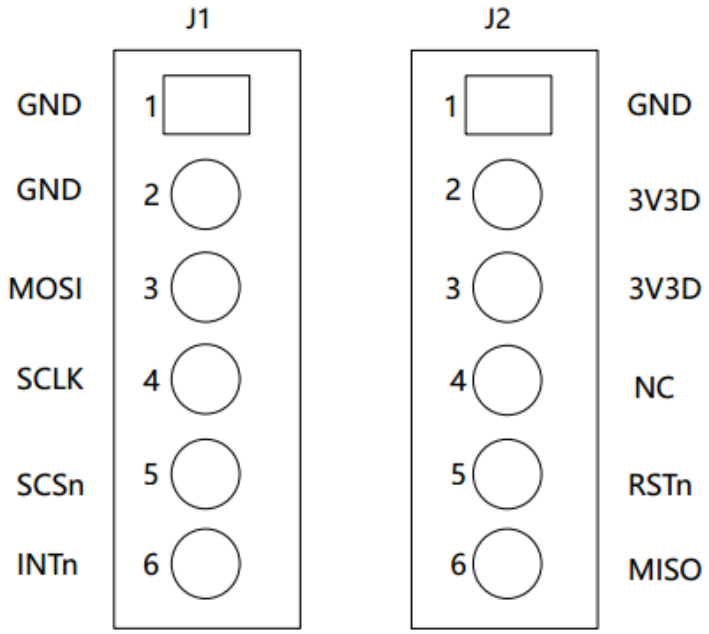
- Support Hardwired Internet protocols
  : TCP, UDP, WOL over UDP, ICMP, IGMPv1/v2, IPv4, ARP, PPPoE
- Support 4 independent SOCKETs simultaneously
- Supports half/full duplex operation
- Support SOCKET-less command
  : ARP-Request, PING-Request
- Support Ethernet Power down mode & Main Clock gating for power save
- Support Wake on LAN over UDP
- Supports high speed SPI Interface (SPI mode 0/3)
- Internal 16Kbytes Memory for TX/ RX Buffers
- 10BaseT/100BaseTX Ethernet PHY Integrated
- Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- Supports Wake On LAN
- Support Auto-MDIX only when Auto-Negotiation mode
- 3.3V operation with 5V I/O signal tolerance
- Interfaces with two 2.54mm pitch 1 x 6 header pin
- Very small form factor: 23mm x 25mm (PCB size)

2. Pin assignment & description

2.1. Pin assignment



< TOP side view >



< Pin assignment >

2.2. Pin description

Pin No.		I/O	Pin Name	Description
J1	1	P	GND	**Ground**
	2	P	GND	**Ground**
	3	I	MOSI	**SPI Master Out Slave In** This pin is used to SPI MOSI signal pin.
	4	I	SCLK	**SPI Clock** This pin is used to SPI Clock Signal pin.
	5	I	SCSn	**SPI Slave Select :** Active Low This pin is used to SPI Slave Select signal Pin when using SPI interface.
	6	O	INTn	**Interrupt** : Active low This pin indicates that W5100S requires MCU attention after socket connecting, disconnecting, data receiving timeout, and WOL (Wake on LAN). The interrupt is cleared by writing IR Register or Sn_IR (Socket n-th Interrupt Register). All interrupts are maskable.
J2	1	P	GND	**Ground**
	2	P	3V3D	**Power** : 3.3 V power supply
	3	P	3V3D	**Power** : 3.3 V power supply
	4	I	-	-
	5	I	RSTn	**Reset :** RSTn initializes W5100S. RSTn must be asserted to Low longer than 500ns. After asserted RSTn, W5100S spends 60.3ms for initialization. Low : W5100S initialized. High : Normal Operation.
	6	O	MISO	**SPI Master In Slave Out** This pin is used to SPI MISO signal pin.

3. Device SPI operations

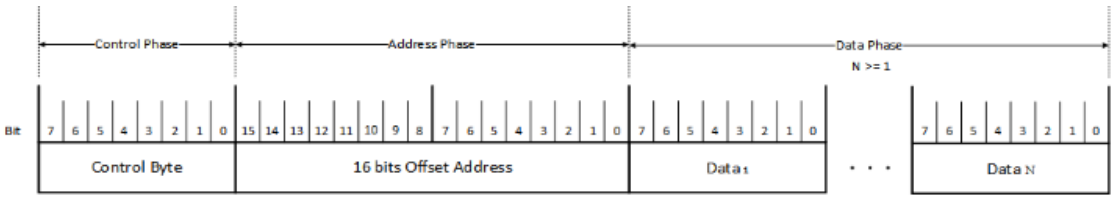
WIZ810Sio is controlled by a set of instruction that is sent from an external host, commonly referred to as the SPI Master. The SPI Master communicates with W5100S on WIZ810Sio via the SPI bus, which is composed of four signal lines: Slave Chip Select (SCSn), Serial Clock (SCLK), MOSI (Master Out Slave In) and MISO (Master In Slave Out).

The SPI protocol defines four modes for its operation (Mode 0-3). Each mode differs according to the SCLK polarity and phase - how the polarity and phase control the flow of data on the SPI bus. The W5100S operates as SPI Slave device and supports the most common modes - SPI Mode 0 and 3.

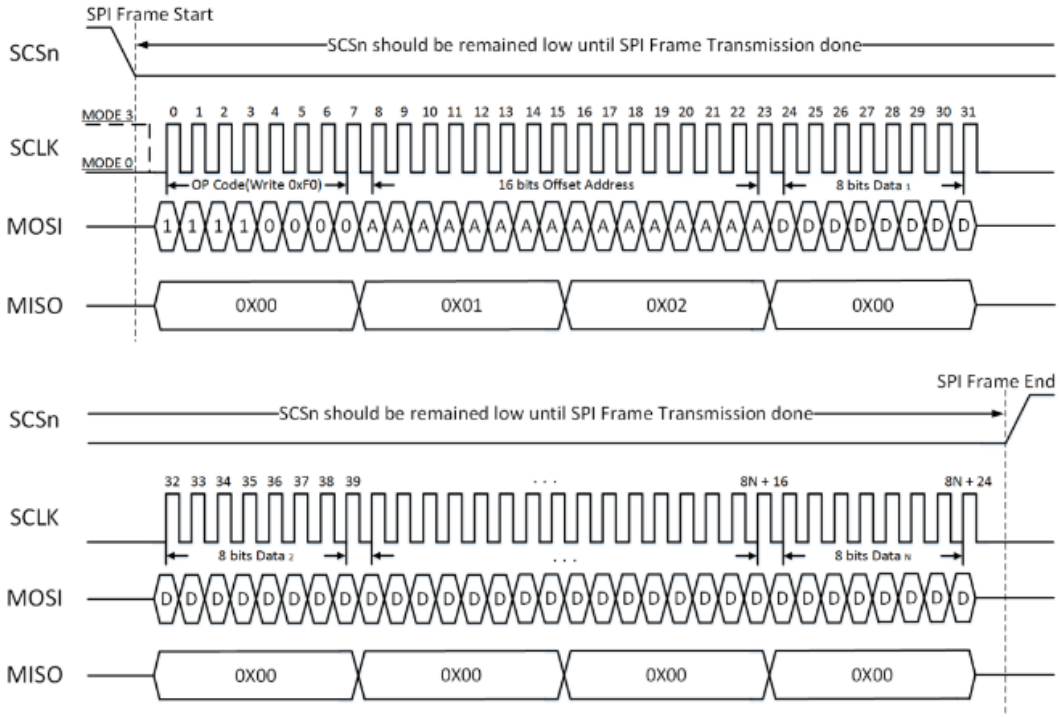
The only difference between SPI Mode 0 and 3 is the polarity of the SCLK signal at the inactive state. With SPI Mode 0 and 3, data is always latched in on the rising edge of SCLK and always output on the falling edge of SCLK.

3.1. Process of using general SPI Master device

1. Configure Input/Output direction on SPI Master Device pins.
2. Configure SCSn as 'High' on inactive
3. Configure SCSn as 'Low' (data transfer start)
4. Write Control Byte for transmission on SPDR register.
5. Write target address for transmission on SPDR register (SPI Data Register).
6. Write desired data for transmission on SPDR register.
7. Wait for reception complete
8. If all data transmission ends, configure SCSn as 'High'



< W5100S SPI Frame Format >

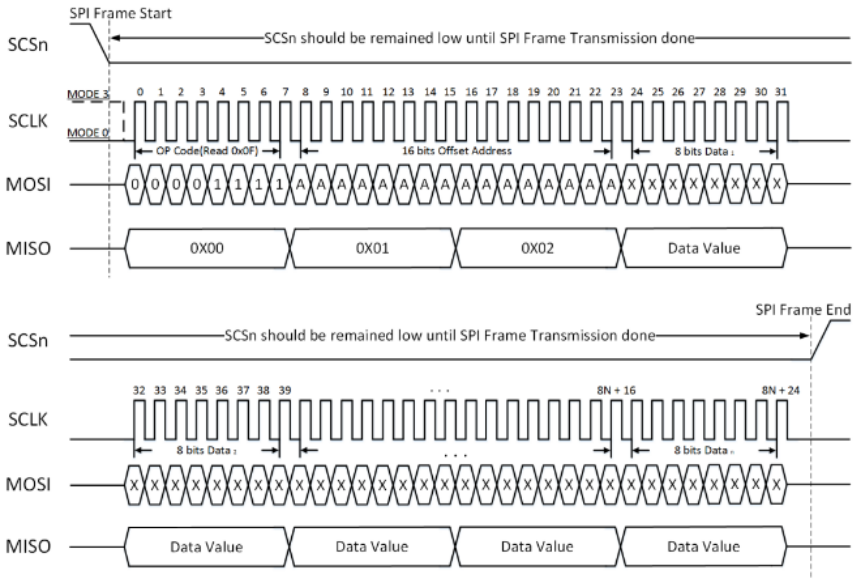


< Control, Address and DATA Sequence Diagram >

3.2. Read processing

The READ processing is entered by driving SCSn low, followed by the Address, the OP code, the Data Length and the Data byte on MOSI. The OP code (OP) is defined type of the READ OP and WIRTE OP. On OP = 0x0F, the read operation is selected. On OP = 0xF0, the write operation is selected.

In W5100S SPI mode, the Byte READ processing and the burst READ processing are provided. The Byte READ processing takes 3 instructions which is consist of the 8-bit OP code(0x0F),16-bit Address and 8-bit Data. Otherwise, The Burst READ processing only takes the Data instruction after the setting of the burst read processing. The MISO pin should be selected by driving MISO low after the falling edge of the SCSn.



< Read Sequence >

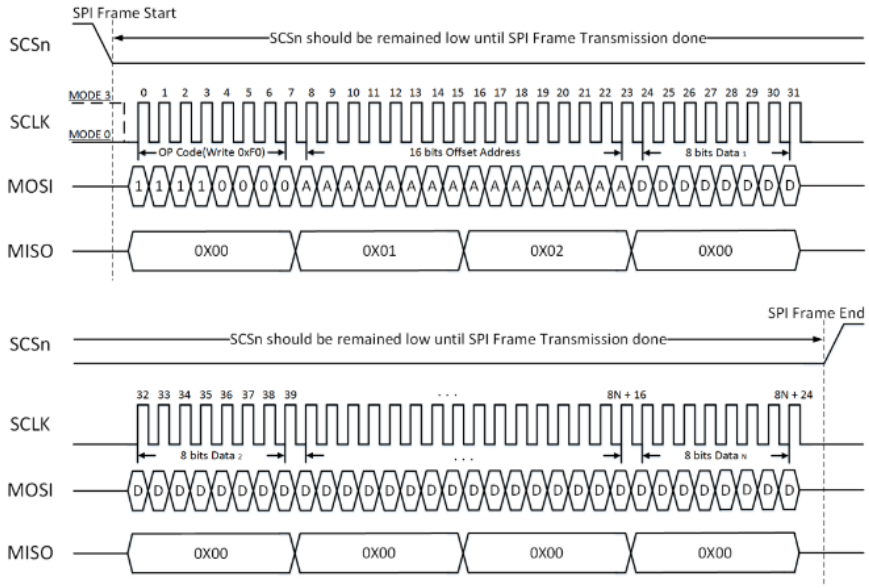
```
/* Pseudo Code for Read data of 8bit per packet */
#define data_read_command      0x00
uint16 addr;        // Address : 16bits
int16 data_len;     // Data length :15bits
uint8 data_buf[];   // Array for data
SpiSendData();      // Send data from MCU to W5100S
SpiRecvData();      // Receive data from   W5100S to MCU

{
ISR_DISABLE();   // Interrupt Service Routine disable
CSoff();   // CS=0, SPI start

// OP Read command
SpiSendData (0x0F);

// SpiSendData
SpiSendData(((addr+idx) & 0xFF00) >> 8);     // Address byte 1
SpiSendData((addr+idx) & 0x00FF);       // Address byte 2


// Read data:On data_len> 1, Burst Read Processing Mode.
for(int idx = 0; idx<data_len; idx++)
```

```
{
    SpiSendData(0);   // Dummy data
    data_buf[idx] = SpiRecvData(idx);   // Read data
}
CSon();   // CS=1, SPI end
ISR_ENABLE();   // Interrupt Service Routine disable
}
```

3.3. Write processing

The WRITE processing is entered by driving SCSn low, followed by the Address, the OP code, the Data Length, and the Data byte on MISO.

In W5100S SPI mode, the Byte WRITE processing and the Burst WRITE processing are provided. The Byte WRITE processing takes 3 instructions which is consist of the 8-bit OP code(0xF0), the 16-bit Address and 8-bit Data. Otherwise, The Burst WRITE processing only takes the Data instruction after the setting of the Burst WRITE processing. The MOSI pin should be selected by driving MOSI low after the falling edge of the SCSn.



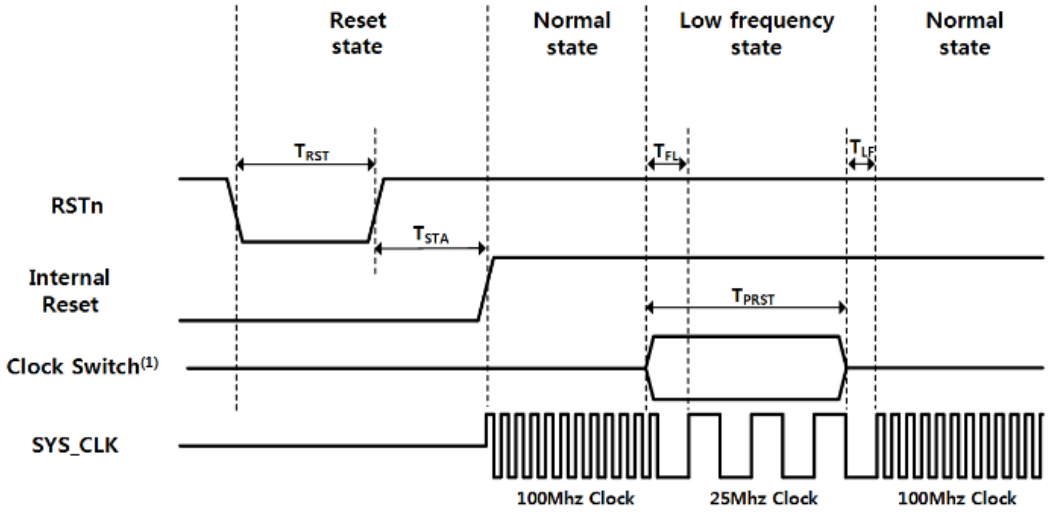
< Write Sequence >

```
/* Pseudo Code for Write data of 8bit per packet */
#define data_write_command      0x80
uint16 addr;      // Address : 16bits
```

```
int16 data_len;       // Data length :15bits
uint8 data_buf[];    // Array for data

{
SpiSendData();     //Send data from MCU to   W5100S

ISR_DISABLE();// Interrupt Service Routine disable
CSoff();// CS=0, SPI start
//OP Write command
SpiSendData(0xF0);

SpiSendData(((addr+idx) & 0xFF00) >> 8);    // Address byte 1
SpiSendData((addr+idx) & 0x00FF);    // Address byte 2


// Write data: On data_len> 1, Burst Write Processing Mode.
for(int idx = 0; idx<data_len; idx++)
    SpiSendData(data_buf[idx]);

CSon();    // CS=1, SPI end
IINCHIP_ISR_ENABLE();    // Interrupt Service Routine disable
}
```

4. Timing diagram

4.1. Reset Timing

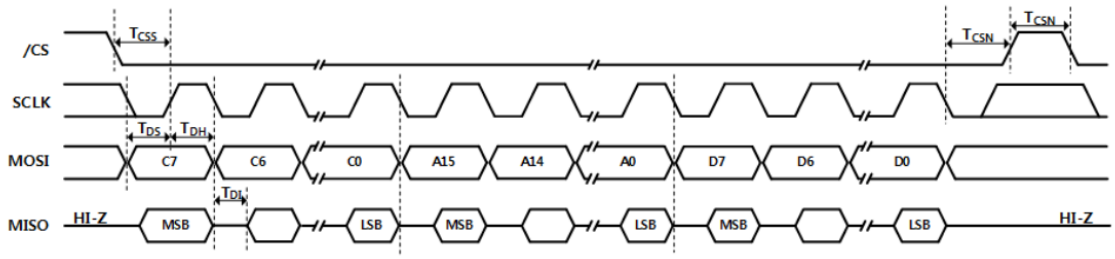


Symbol	Description	Min	Typ	Max
T_{RST}	Reset Time	210 ns	330 ns	560 ns-
T_{STA}	Stable Time	-		60.3 ms
T_{FI}	Fast to Low Time by MR2[CLKSEL]	100 ns		-
T_{FI}	Fast to Low Time by PHYCR1[Reset] or PHYCR1[PWDN]	300 ns		
T_{PRST}	PHY Auto Reset Time	0.6 ms		-
T_{PRST}	PHY Power Down Time	200 us		
T_{PRST}	Clock Switch Time	200 ns		
T_{LF}	Low to Fast Time by MR2[CLKSEL]	100 ns		-
T_{LF}	Low to Fast Time by PHYCR1[Reset] or PHYCR1[PWDN]	100 ns		

**COMMENT*: *PHY Power-down Mode has T_{FI} and T_{LF} (In PHY Power-down Mode, SYS_CLK switches to Low Clock. After T_{FI}, User can be disable PHY Power-down Mode.)*

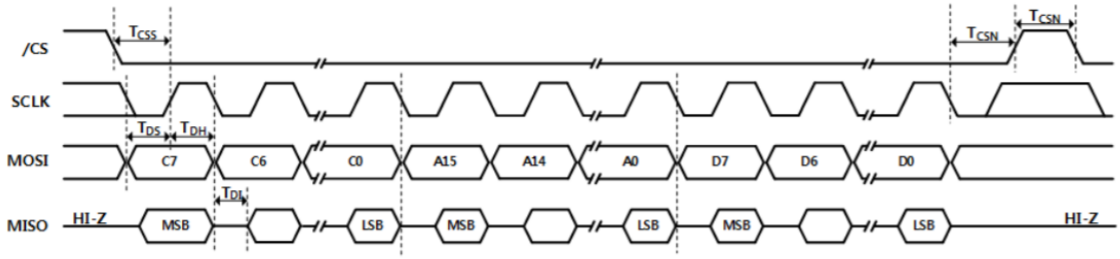
**CAUTION*: *User must not set PHY Auto Reset and PHY Power-down Mode at the same time*

4.2. SPI Access Read Timing



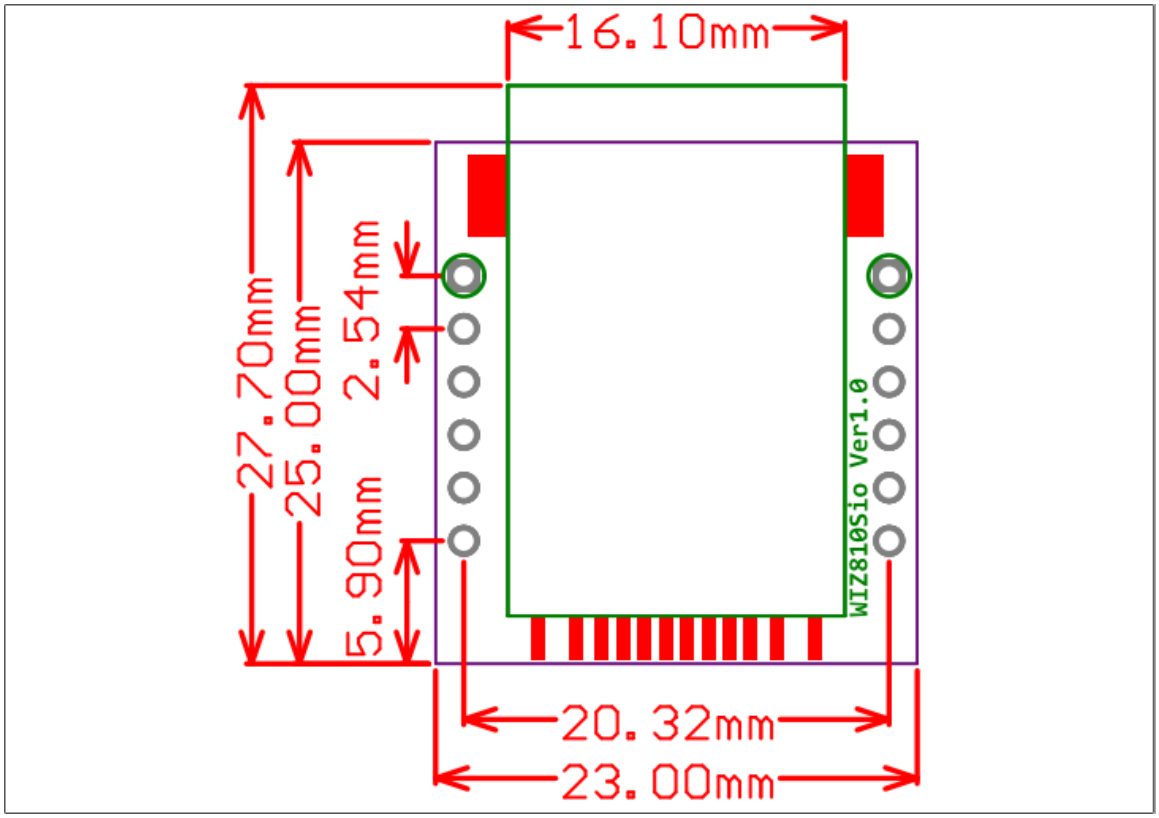
Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency		70	MHz
T_{CSS}	SCSn Setup Time	3 SYS_CLK		ns
T_{CSN}	SCSn Next Time	2 SYS_CLK		ns
T_{DS}	Data In Setup Time	3		ns
T_{DH}	Data In Hold Time	3		ns
T_{DI}	Data Invalid Time	7		ns
T_{DR}	Data Ready Time	6 SYS_CLK + 30		ns

4.3. SPI Access Write Timing

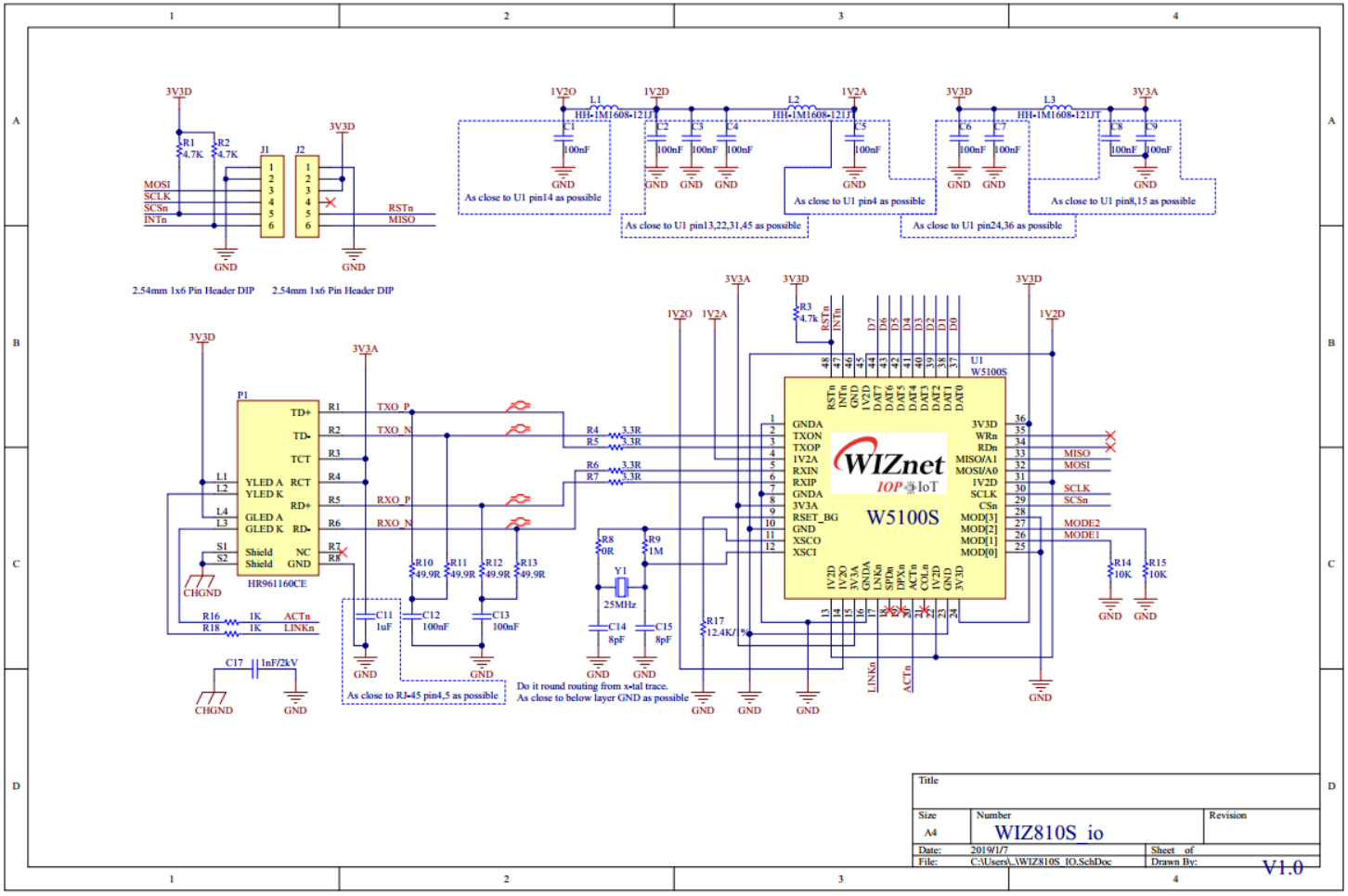


Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency		70	MHz
T_{CSS}	SCSn Setup Time	3 SYS_CLK		ns
T_{CSN}	SCSn Next Time	2 SYS_CLK		ns
T_{DS}	Data In Setup Time	3		ns
T_{DH}	Data In Hold Time	3		ns
T_{DI}	Data Invalid Time	7		ns

5. Dimensions



6. Reference Schematics



7. Warranty

WIZnet Co., Ltd. offers the following limited warranties applicable only to the original purchaser. This offer is non-transferable.

WIZnet warrants our products and its parts against defects in materials and workmanship under normal use for period of standard ONE(1) YEAR for the WIZ810Sio module and labor warranty after the date of original retail purchase. During this period, WIZnet will repair or replace a defective products or part free of charge.

Warranty Conditions:

1. The warranty applies only to products distributed by WIZnet or our official distributors.
2. The warranty applies only to defects in material or workmanship as mentioned above in 3.Warranty. The warranty applies only to defects which occur during normal use and does not extend to damage to products or parts which results from alternation, repair, modification, faulty installation or service by anyone other than someone authorized by WIZnet ; damage to products or parts caused by accident, abuse, or misuse, poor maintenance, mishandling, misapplication, or used in violation of instructions furnished by us ; damage occurring in shipment or any damage caused by an act of God, such as lightening or line surge.

Procedure for Obtaining Warranty Service

1. Contact an authorized distributors or dealer of WIZnet for obtaining an RMA (Return Merchandise Authorization) request form within the applicable warranty period.
2. Send the products to the distributors or dealers together with the completed RMA request form. All products returned for warranty must be carefully repackaged in the original packing materials.
3. Any service issue, please contact to sales@wiznet.co.kr

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

WIZnet:
WIZ810SIO