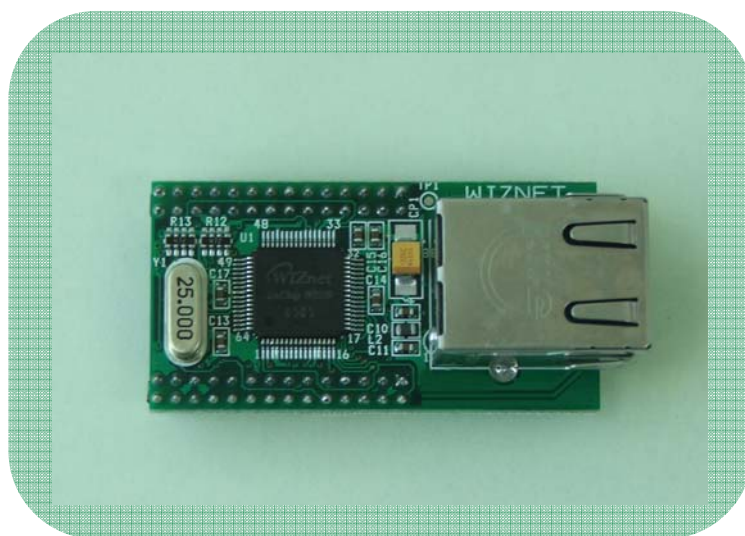


NM7010B⁺ Datasheet

(Ver. 1.3)



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Document History Information

Revision	Date	Description
Ver. 1.0	OCTOBER , 2006	Release with NM7010B ⁺ Launching
Ver. 1.1	June 29, 2007	Add SPI signal Pin description(A14-A11)
Ver.1.2	July 24, 2007	PHY Chip Change (RTL8201CP -> IP101A) For more information, refer to NM7010B+ schematic.
Ver.1.3	January 9, 2008	Add power consumption in Feature

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The screenshot shows the WIZnet website with the following sections:

- Header:** WIZnet logo, navigation links (Home, Sitemap, Contact us, 한국어), and a menu bar (Products, Technology, Technical Q & A, Library, Where to buy, Value Chain, About us).
- Main Banner:** Promoting the W5100 chip as a '3 in 1' solution for embedded Internet (TCP/IP Core + MAC + PHY).
- New Products:** WIZ Series with W5100, specifically the Serial-to-Ethernet WIZ100SR.
- Application Reference:**
 - [038] Solar Cell Inverter [2007.07.23]
 - [037] Mobile Base Station [2007.07.09]
 - [036] Individual Screens in TGV [2007.06.05]
- Solution Provider:**
 - NET7026: Single Board Computer plus Ethernet [2007.07.23]
 - LPC2106 goes network [2007.07.23]
 - EV8-3150/8051 Evaluation Board [2007.07.13]
- WIZnet News:**
 - [EDN China] W5100 release news [2007.07.11]
 - [ET Platform] Fabless Ecosystem in Channel 2.0 Era [2007.07.02]
 - [CIRCUIT CELLAR July 2007] New Product News [2007.07.02]
- Technical Support:** A link highlighted by a blue box and a large green arrow pointing to it from the text 'Click !!'.
- Footer:** WIZnet logo, copyright information, and logos for NEC, AMEL, and MICROCHIP.

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1. Introduction

NM7010B⁺ is the network module that includes W3150A⁺ (TCP/IP hardwired chip), Ethernet PHY (IP101A), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W3150A⁺ and PHY chip. The NM7010B⁺ is an ideal option for users who want to develop their Internet enabling systems rapidly.

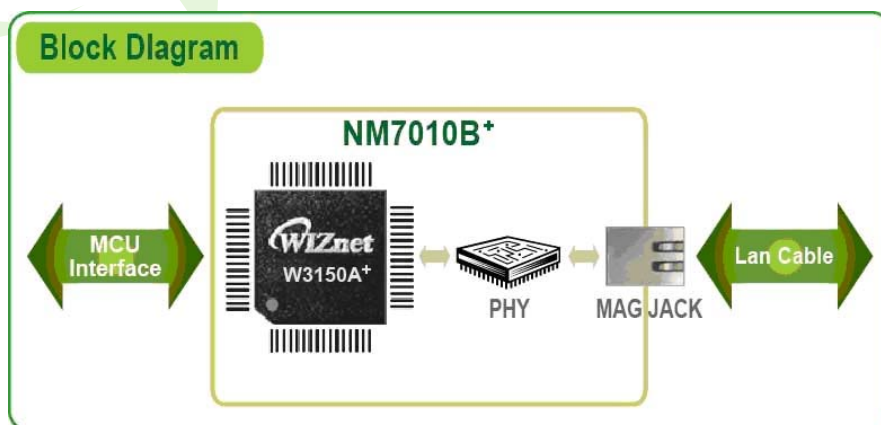
NM7010B⁺ consists of W3150A⁺, Ethernet PHY and MAG-JACK.

- TCP/IP, MAC protocol layer: W3150A⁺
- Physical layer: Ethernet PHY
- Connector: MAG-JACK

1.1. Features

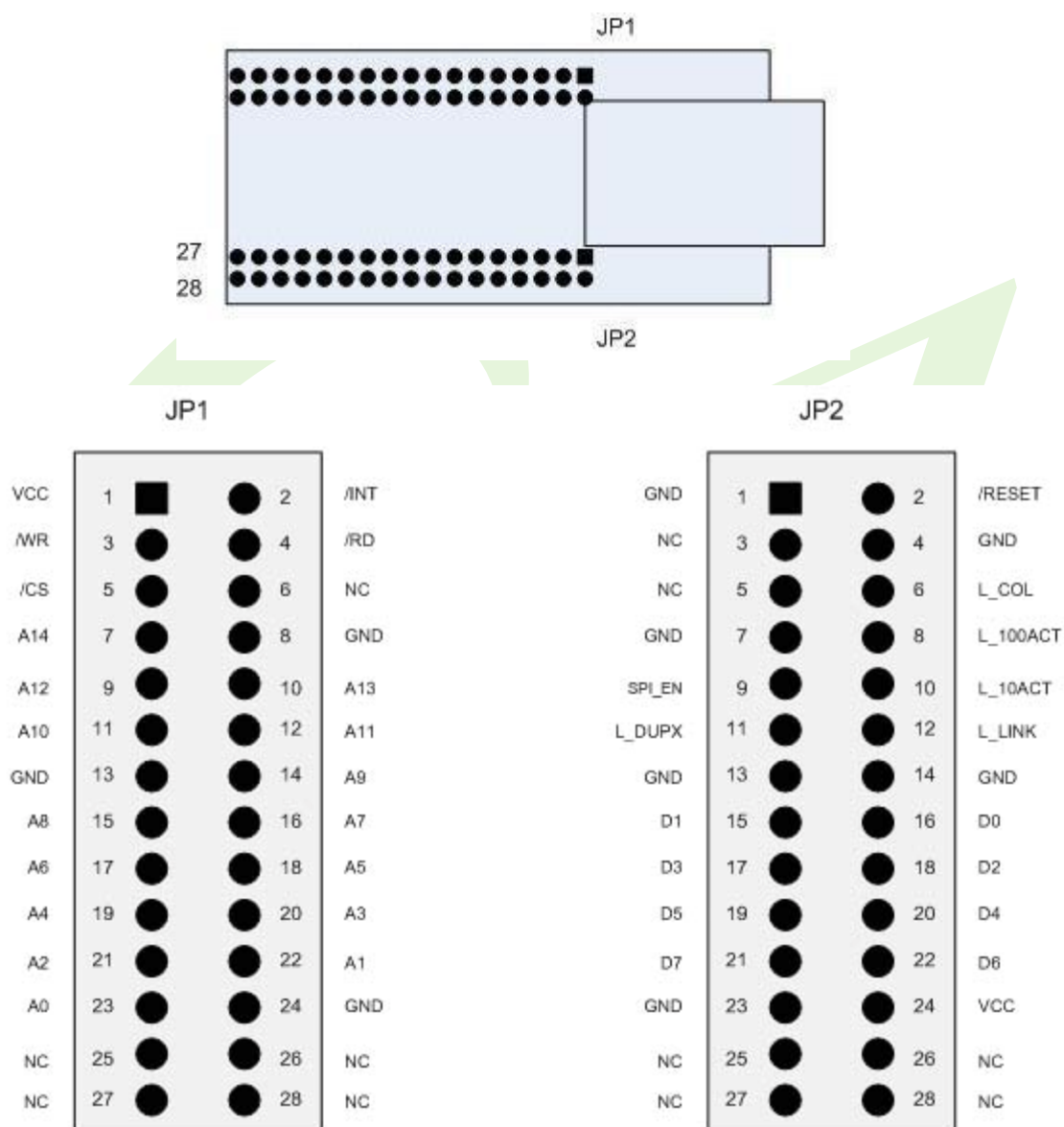
- Supports 10/100 Base TX
- Supports half/full duplex operation
- Supports auto-negotiation and auto crossover detection
- IEEE 802.3/802.3u Complaints
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP, PPPoE, IGMP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 4 independent connections simultaneously
- Supports MCU bus Interface and SPI Interface
- Supports Direct/Indirect mode bus access
- Supports Socket API for easy application programming
- Interfaces with Two 2.0mm pitch 2 * 14 header pin
- Maximum Power Consumption is 160mA at 3.3V

1.2. Block Diagram



2. Pin Assignments & descriptions

2.1. Pin Assignments



I : Input

O : Output

I/O : Bi-directional Input and output

P : Power

2.2. Power & Ground

Symbol	Type	Pin No.	Description
VCC	P	JP1 : 1 , JP2 : 24	Power : 3.3 V power supply
GND	P	JP1 : 8, JP1 : 13, JP1 : 24, JP2 : 1 JP2 : 4, JP2 : 7 JP2 : 13, JP2 : 14 JP2 : 23	Ground

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2.3. MCU Interfaces

Symbol	Type	Pin No.	Description
A14	I	JP1 : 7	ADDRESS PIN OR SCLK(Serial Clock) This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI Clock signal Pin.
A13	I	JP1 : 10	ADDRESS PIN or /SS (Slave Select) * This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI Slave Select signal Pin. In only SPI Mode, this pin is active low
A12	I	JP1 : 9	ADDRESS PIN or MOSI (Master Out Slave In) * This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI MOSI signal pin.
A11	I/O	JP1 : 12	ADDRESS PIN or MISO (Master In Slave Out) * This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI MISO signal pin.
A10~A8	I	JP1 : 11, JP1 : 14 JP1 : 15	Address Used as Address[10-8] pin
A7~A0	I	JP1 : 16 ~ JP1 : 23	Address Used as Address[7-0] pin
D7~D0	I/O	JP2 : 21, JP2 : 22 JP2 : 19, JP2 : 20 JP2 : 17, JP2 : 18 JP2 : 15, JP2 : 16	Data 8 bit-wide data bus
/CS	I	JP1 : 5	Module Select : Active low. /CS of W3150A ⁺
/RD	I	JP1 : 4	Read Enable : Active low. /RD of W3150A ⁺
/WR	I	JP1 : 3	Write Enable : Active low /WR of W3150A ⁺

/INT	O	JP1 : 2	Interrupt : Active low After reception or transmission it indicates that the W3150A⁺ requires MCU attention. By writing values to the Interrupt Status Register of W3150A⁺ the interrupt will be cleared. All interrupts can be masked by writing values to the IMR of W3150A⁺ (Interrupt Mask Register). For more details refer to the W3150A⁺ Datasheet
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2.4. Network status & LEDs

You can observe the network status using MAC-JACK LEDs. LED interface can be extended to the LED of the main board.

Symbol	Type	Pin No.	Description
L_COL	O	JP2 : 6	Collision LED : Active low when collisions occur.
L_100ACT	O	JP2 : 8	Link 100/ACT LED : Active low when linked by 100 Base TX, and blinking when transmitting or receiving data.
L_10ACT	O	JP2 : 10	Link 10/ACT LED : Active low when linked by 10 Base T, and blinking when transmitting or receiving data.
L_DUPX	O	JP2 : 11	Full Duplex LED : Active low when in full duplex operation. Active high when in half duplex operation.
L_LINK	O	JP2 : 12	Link LED : Active low when linked

2.5. Miscellaneous Signals

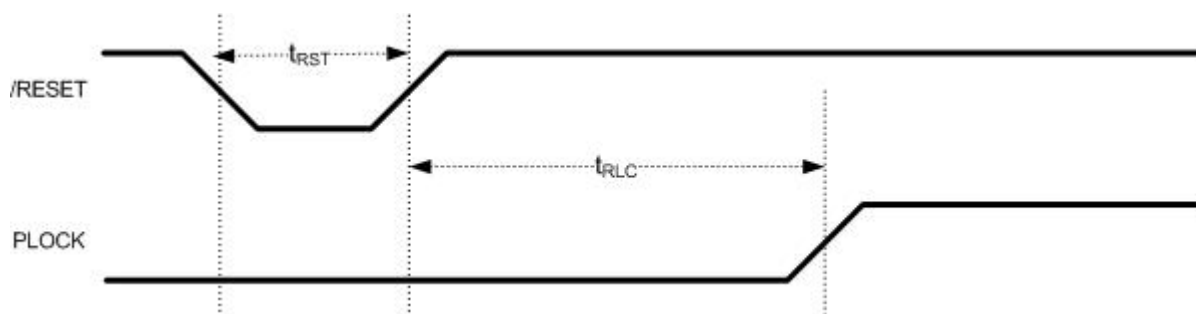
Symbol	Type	Pin No.	Description
/RESET	I	JP2 : 2	Reset : Active low Reset W3150A, RTL8201BL chip. For complete reset function this pin must be asserted low for at least 10ms.
SPI_EN	I	JP2 : 9	SPI Enable This pin selects Enable/disable W3150A ⁺ SPI Mode This pin is internally pulled low for previous W3150A users. Even if there is no signal connection to this pin, it asserts low internally. So change to new version W3150A ⁺ including SPI interface, there is no effort to change previous board design. Low = Disable W3150A ⁺ SPI Mode High = Enable W3150A ⁺ SPI Mode
NC	-	JP1 : 6, 25, 26, 27, 28 JP2 : 3, 5, 9, 25, 26, 27, 28	Not Connect

3. Timing Diagrams

NM7010B⁺ provides following interfaces of W3150A⁺

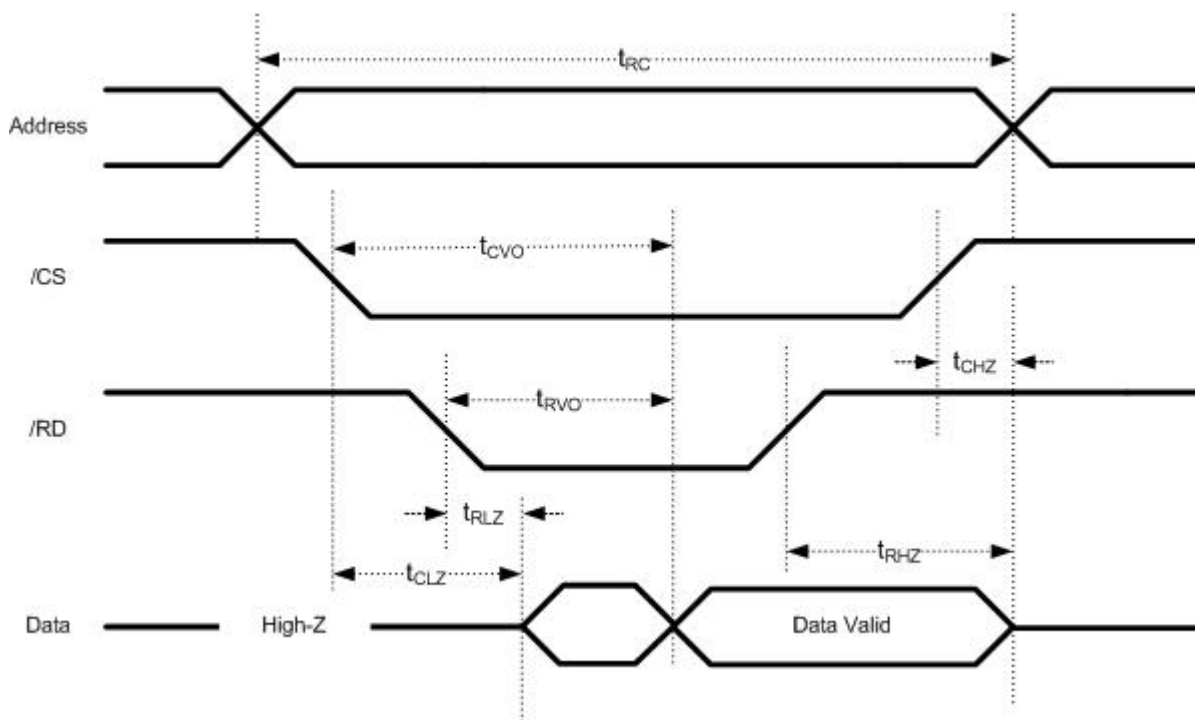
- Direct/Indirect mode bus access
- SPI access

3.1. Reset Timing



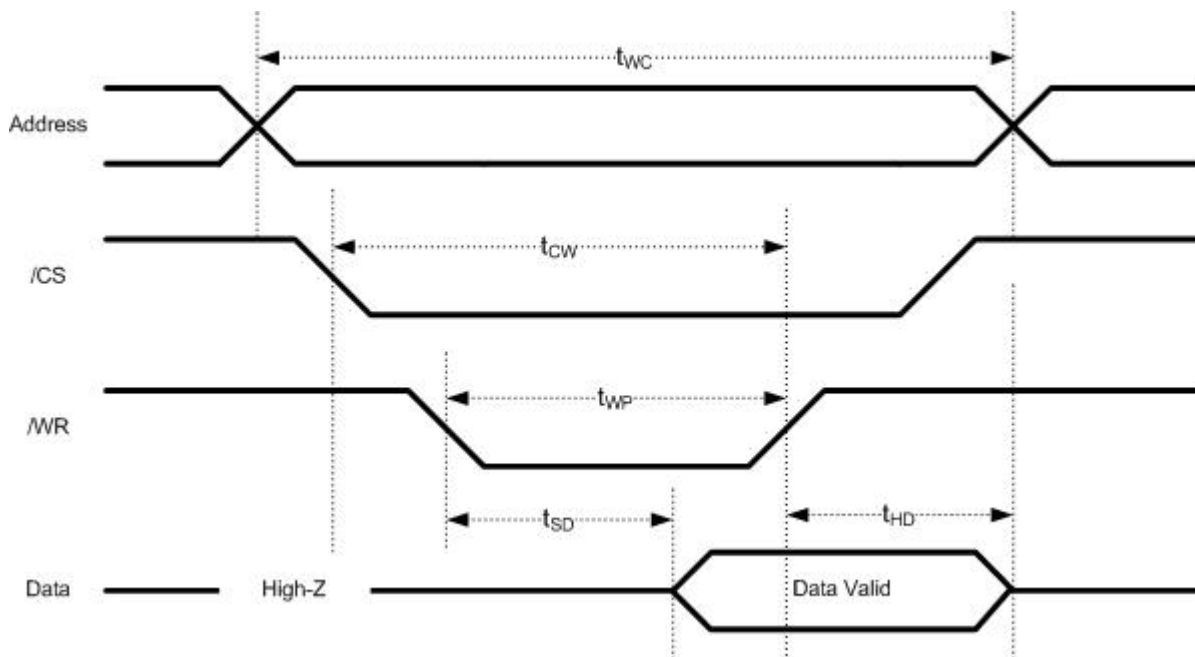
Symbol	Parameter	Min	Max
t_{RST}	Reset Cycle Time	2 μs	-
t_{RLC}	$\overline{\text{RESET}}$ to internal PLOCK	-	10 ms

3.2. Register/Memory READ Timing



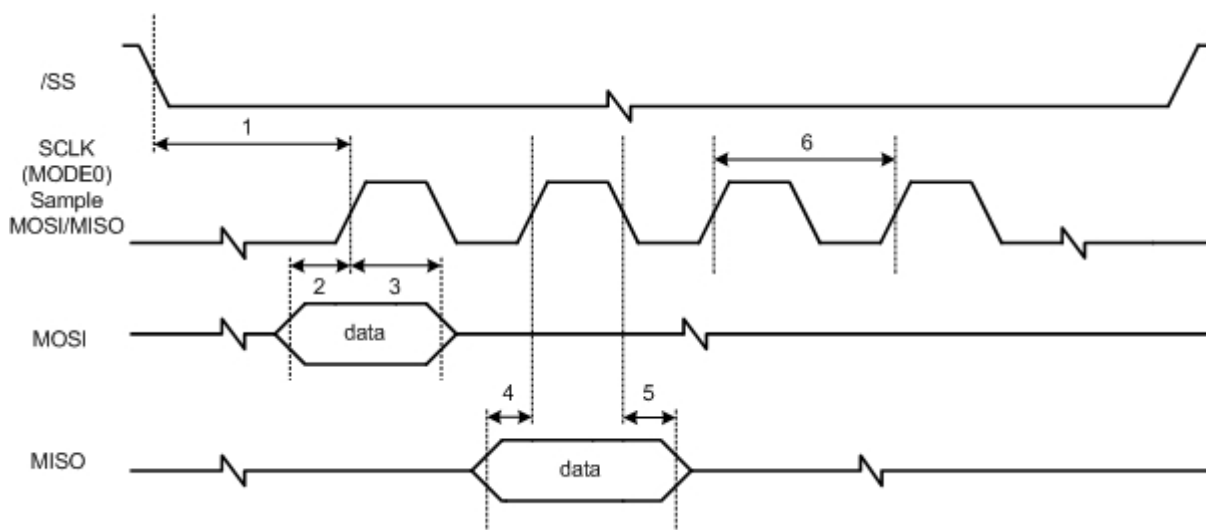
Symbol	Parameter	Min	Max
t_{RC}	Read Cycle Time	80 ns	-
t_{CVO}	/CS to Valid Output	-	80 ns
t_{RVO}	/RD to Valid Output	-	80 ns
t_{CLZ}	/CS to Low-Z Output	0 ns	-
t_{RLZ}	/RD to Low-Z Output	0 ns	-
t_{CHZ}	/CS to High-Z Output	-	1 ns
t_{RHZ}	/RD to High-Z Output	-	1 ns

3.3. Register/Memory WRITE Timing



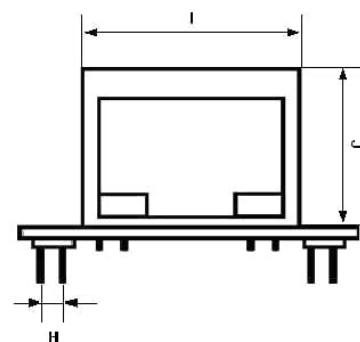
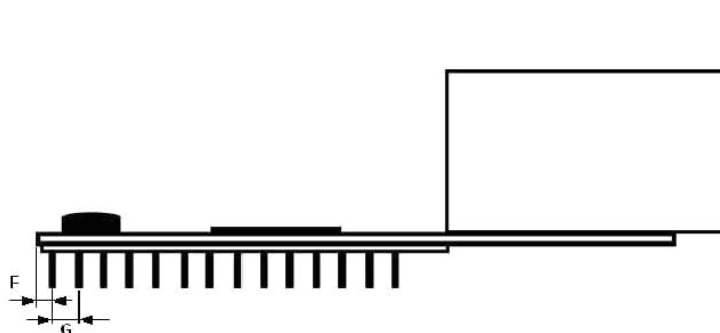
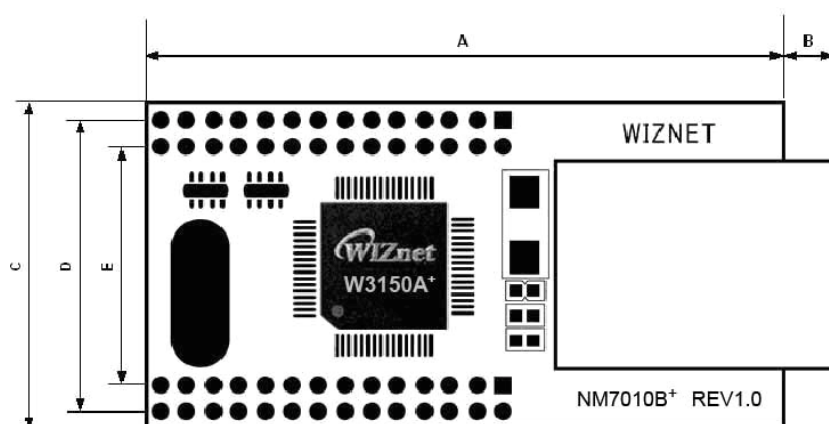
Symbol	Parameter	Min	Max
t_{WC}	Write Cycle Time	70 ns	-
t_{CW}	/CS to Write End	70 ns	-
t_{WP}	/WR Pulse width	63 ns	-
t_{SD}	/WR low to SD valid	-	14 ns
t_{HD}	Data Hold from Write End	0 ns	-

3.4. SPI Timing



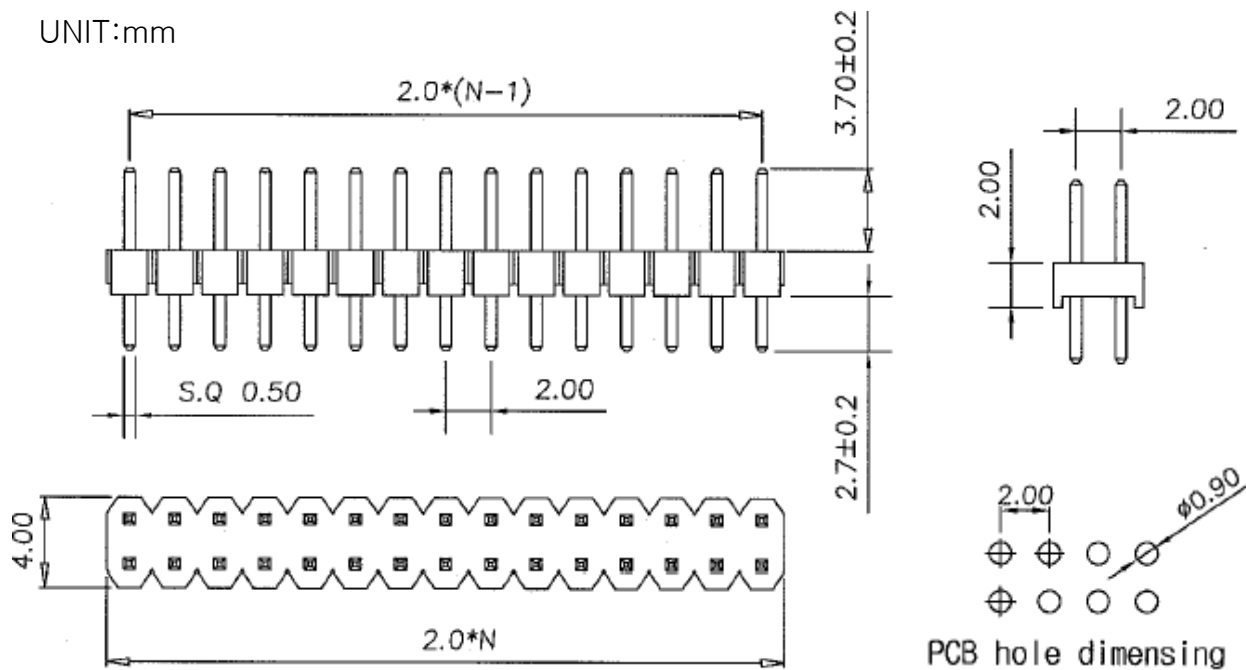
	Description	Mode	Min	Max
1	/SS low to SCLK	Slave	21 ns	-
2	Input setup time	Slave	7 ns	-
3	Input hold time	Slave	28 ns	-
4	Output setup time	Slave	7 ns	14 ns
5	Output hold time	Slave	21 ns	-
6	SLKC time	Slave	70 ns	

4. Dimensions

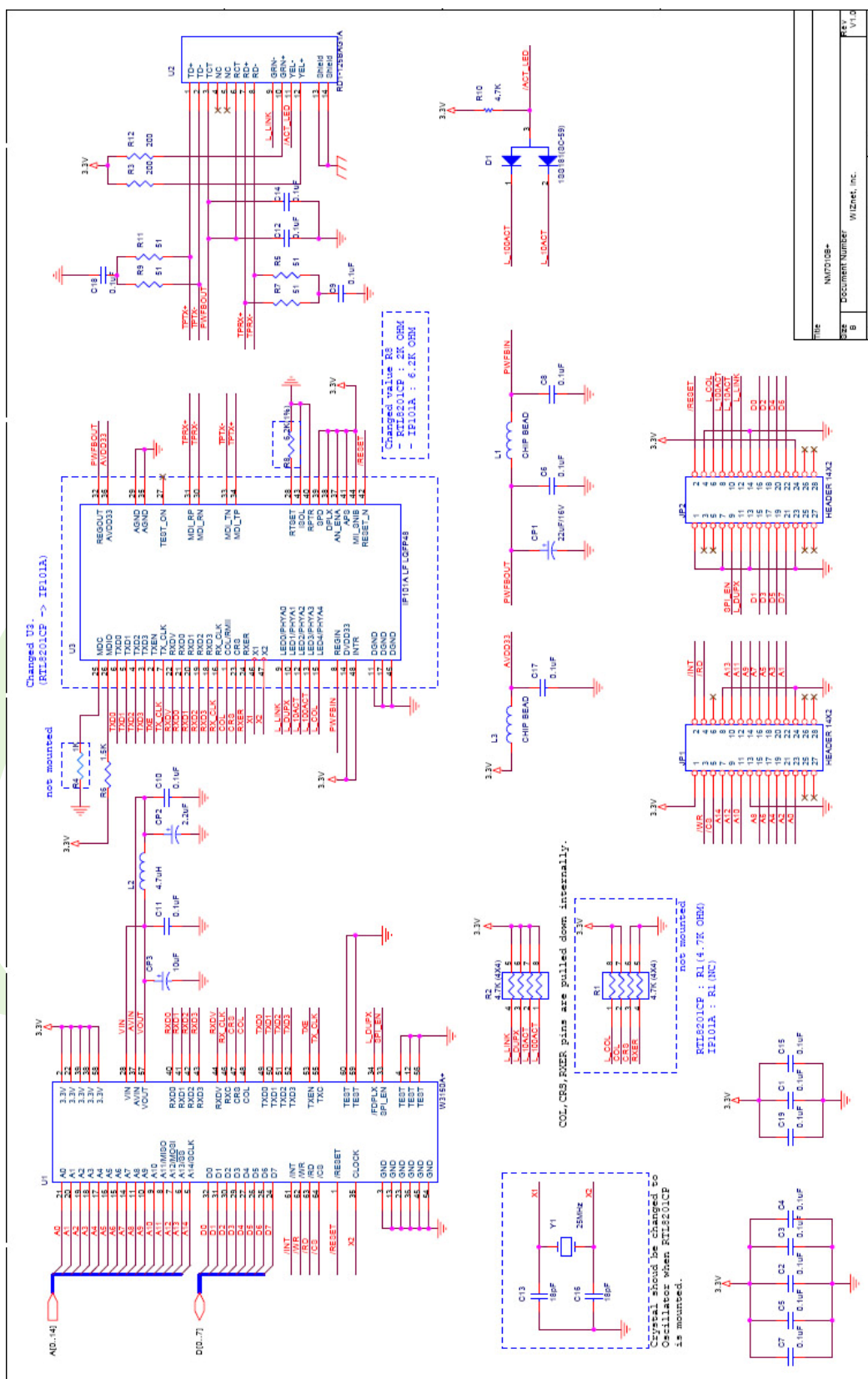


Symbols	Dimensions (mm)
A	48.0
B	4.0
C	25.0
D	22.4
E	18.4
F	1.0
G	2.0
H	2.0
I	16.0
J	13.4

5. Connector Specification



6. Schematic



[Parts Revision History]

	Description	Parts
Before	W3150A ⁺ + RTL8201CP	R1 : 4.7K OHM ARRAY R4 : 1K OHM R8 : 2K OHM 1% U3 : RTL8201CP
After	W3150A ⁺ + IP101A-LF	R1 : Not mounted R4 : Not mounted R8 : 6.2K OHM 1% U3 : IP101A-LF

※ If you have the hardware having previous parts, refer to the NM7010B⁺ datasheet V1.1 for the usage. For more stable operation, we recommend using the part revised hardware.

7. Partlists

Item	Q.ty	Reference	Part	Tech. Characteristics	Package
1	1	CP1	22uF	16Vmin 10%	EIA/IECQ 3528
2	1	CP2	2.2uF	10Vmin 10%	EIA/IECQ 3216
3	1	CP3	10uF	10Vmin 10%	EIA/IECQ 3216
4	17	C1,C2,C3,C4,C5, C6,C7,C8,C9,C10, C11,C12,C14,C15, C17,C18,C19	0.1uF	50V-20% Ceramic	CASE 0603
5	2	C13,C16	18pF	50V-20% Ceramic	CASE 0603
6	1	D1	1SS181 Switching Diode		SC-59
7	2	JP2,JP1	2X14 28PIN 2mm DIP STRAIGHT Header	2 X 14 2mm pitch	
8	2	L3,L1	120R Chip Ferrite Bead	120R@100MHz 300mA	CASE 0603
9	1	L2	4.7uH Chip Ferrite Inductor	4.7uH, 50mA	CASE 0805
10	0	R4	1K	NOT MOUNTED	
11	1	R6	1.5K	1/10W-5% SMD	CASE 0603
12	1	R8	6.2K 1%	1/10W-1% SMD	CASE 0603
13	2	R12,R3	200	1/10W-5% SMD	CASE 0603
14	4	R5,R7,R9,R11	51 1%	1/10W-1% SMD	CASE 0603
15	1	R10	4.7K	1/10W-5% SMD	CASE 0603
16	1	R2	4.7K Chip Array(0603 X 4)	50V-5% SMD Chip-Array	CASE 1206
17	0	R1	4.7K Chip Array(0603 X 4)	NOT MOUNTED	
18	1	U1	W3150A ⁺		LQFP64
19	1	U3	IP101A		LQFP48
20	1	U2	RD1-125BAG1A MAG- JACK	Transformer + RJ45	
21	1	Y1	25MHz Crystal	Holder Type, CL=18pF	ATS-25U
22	1		NM7010B+ REV1.0 FR4 1.6T 4LAYER	PRINTED CIRCUIT BOARD	

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