



WM825B00 Datasheet

Single-Band (2.4 GHz) Wi-Fi IEEE 802.11 b/g/n
Module with integrated antenna

Revision 1.1
Nov 21, 2017

Copyright © 2017 Wi2Wi, Inc.
2107 N. 1st Street, Ste. 680, San Jose, CA 95131, United States
Email: sales@wi2wi.com | Phone: 1-408-416-4200 | Fax: 1-608-831-3343

Disclaimers

Wi2Wi, Inc. PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE MANAGING DIRECTOR OF Wi2Wi, Inc.

The definitions used herein are:

a) Life support devices or systems are devices which (1) are intended for surgical implant into the body, or (2) support or sustain life and whose failure to perform when properly used in accordance with the instructions for use provided in the labeling can reasonably be expected to result in a significant injury to the user. b) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Wi2Wi does not assume responsibility for use of any of the circuitry described, no circuit patent licenses are implied and Wi2Wi reserves the right at any time to change without notice said circuitry and specifications.

The content of this document is to be treated as strictly confidential and is not to be disclosed, reproduced or used, except as authorized in writing by Wi2Wi, Inc.

Table of Contents

1. Overview	6
1.1 Features	6
1.2 IEEE 802.11 Standards.....	7
1.3 Packaging.....	7
1.4 Memory	7
1.5 WLAN MAC	7
1.6 WLAN Radio.....	8
1.7 Peripheral Bus Interfaces.....	8
2. System Description.....	9
2.1 Block Diagram	9
2.2 Pin Diagram and Description	10
2.3 Physical Dimensions and Pad Locations	13
3. Electrical Characteristics.....	14
4. Voltage Domains	15
5. External Connections	16
5.1 Power supply.....	16
5.2 Reset.....	16
5.2.1 Internal Reset.....	16
5.2.2 External PDn Assertion	16
5.3 Host Configuration	17
5.4 Host interfaces	17
5.4.1 SDIO interface.....	17
5.4.2 USB interface	18
5.4.3 Clock	19
5.4.4 Antenna / RF path	19
5.4.5 GPIO	19
6. WLAN External Host Interface.....	20
6.1 SDIO Timing Diagrams	20
7. WLAN Power-Save Modes	22
7.1 Full Power-Down Mode ²	22
7.2 IEEE Power Save.....	22
7.3 Deep Sleep.....	22
8. Software Specifications	23
8.1 Host Processor.....	24
9. Reference Schematics	25
10. Manufacturing Notes.....	26
10.1 Shield Marking.....	26
10.2 Storage and Baking Instructions	26
10.3 Recommended Reflow Profile.....	26
11. Ordering Information	28
12. Data Sheet Status.....	28
13. Certifications	29
14. References.....	31
14.1 Specifications	31
14.2 Trademarks, Patents and Licenses	31
14.3 Disclosures.....	31

List of Figures

Figure 1: Block Diagram	9
Figure 2 : WM825B00 Module Pin Diagram – Top View	10
Figure 3: SDIO FS Timing	20
Figure 4: SDIO HS Timing.....	20
Figure 5: Stack Diagram	24
Figure 6: EVB Reference Schematics	25
Figure 7: Shield Marking – Top View	26
Figure 8: Recommended Reflow Profile	27

List of Tables

Table 1: Pin Description	11
Table 2 : Electrical Characteristics	14
Table 3 : 3.3V Voltage Domain Signal Limits	15
Table 4 : 1.8V Voltage Domain Signal Limits	15
Table 5: SDIO Timing Data	21
Table 6: Ordering Information for Modules	28
Table 7: Ordering Information for Evaluation Kits.....	28

Revision History:

Revision	Revision Date	Originator	Changes
0.4	Oct 13, 2016	SA	Initial version Datasheet
1.0	May 19, 2017	SA	Changed Datasheet format
1.1	Nov 21, 2017	SK	u.FL changed to MHF4 IPEX

1. Overview

WM825B00 is a complete wireless subsystem with industry's best integration in a small form factor, featuring full 802.11 b/g/n WLAN capabilities with excellent performance. WM825B00 is part of Wi2Wi's Maximum Performance (MX) series. It includes integrated MAC, baseband, RF front-end, PA, crystal, Tx/Rx switch, filter and OTP memory for calibration data and MAC address storage. This module also has an onboard chip antenna and MHF4 IPEX connector. This module is fully optimized to yield excellent throughput and receive sensitivity performance through careful design. It supports SDIO and USB host interfaces. This module is available in industrial, extended and commercial operating temperature variants.

1.1 Features

- Compact design for easy integration: 12.5mm x 16mm x 1.76mm
- QFN module with 32 pins
- Single-band (2.4 GHz) Wi-Fi 802.11 b/g/n
- 20 MHz channel bandwidth, 1x1 SISO operation
- Optimized RF and electrical design for better performance in co-existence with other wireless standards
- Support for SDIO and USB host interfaces
- SDIO High Speed up to 50 MHz, 4 bit
- Antenna Options: Chip Antenna, MHF4 IPEX Connector, RF Pad
- Support for Antenna Diversity
- Operating system support for Linux
- Support for Station Mode and AP Mode
- WEP, WPA, WPA2 (Wi-Fi Protected Access)
- Certifications: FCC, IC, CE
- Green/ROHS compliant
- Internal 38.4 MHz crystal clock
- Low power operation: Deep Sleep and IEEE Power Save modes
- OTP memory (eliminates need for external EEPROM)
- Single power supply of 3.3V

1.2 IEEE 802.11 Standards

- 802.11b data rates of 1, 2, 5.5 and 11 Mbps (DSSS/CCK Modulation)
- 802.11g data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps (OFDM Modulation) for multimedia content transmission
- 802.11g/b performance enhancements
- 802.11n compliant with maximum data rates up to 72.2 Mbps (20 MHz channel)
- 802.11d international roaming
- 802.11e quality of service
- 802.11h transmit power control
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11n block acknowledgement extension
- 802.11r fast hand-off for AP roaming
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode

1.3 Packaging

- 32-pins with pads on 3 sides of the module and 4 ground pads in the middle of the module on the bottom side.

1.4 Memory

- Internal SRAM for TX frame queues/RX data buffers
- Boot ROM
- OTP

1.5 WLAN MAC

- Simultaneous peer to peer and infrastructure modes
- RTS/CTS for operating under DCF
- Hardware filtering of 32 multicast addresses.
- On-chip TX and RX FIFO for maximum throughput
- Open system and shared key authentication services
- A-MPDU RX (de-aggregation) and TX (aggregation)
- Reduce Inter-Frame Spacing (RIFS) receive
- Management information base counters
- Radio resource measurement counters
- Quality of Service queues

- Block acknowledgement extension
- Multiple BSSID and multiple station operation
- Transmit rate adaption
- Long and Short preamble generation on a frame by frame basis for 802.11b frames
- Mobile Hotspot

1.6 WLAN Radio

- Integrated Direct Conversion Radio
- Integrated T/R switch, PA, and LNA
- Integrated Antenna and Antenna Connector

1.7 Peripheral Bus Interfaces

- Clocked serial unit

2. System Description

WM825B00 is a complete module, combination of the 88W8801 802.11 b/g/n, 1 x 1 SISO device and all the components needed to operate the radio. It preserves characteristics from the chipset while providing optimized system level functionality and performance.

2.1 Block Diagram

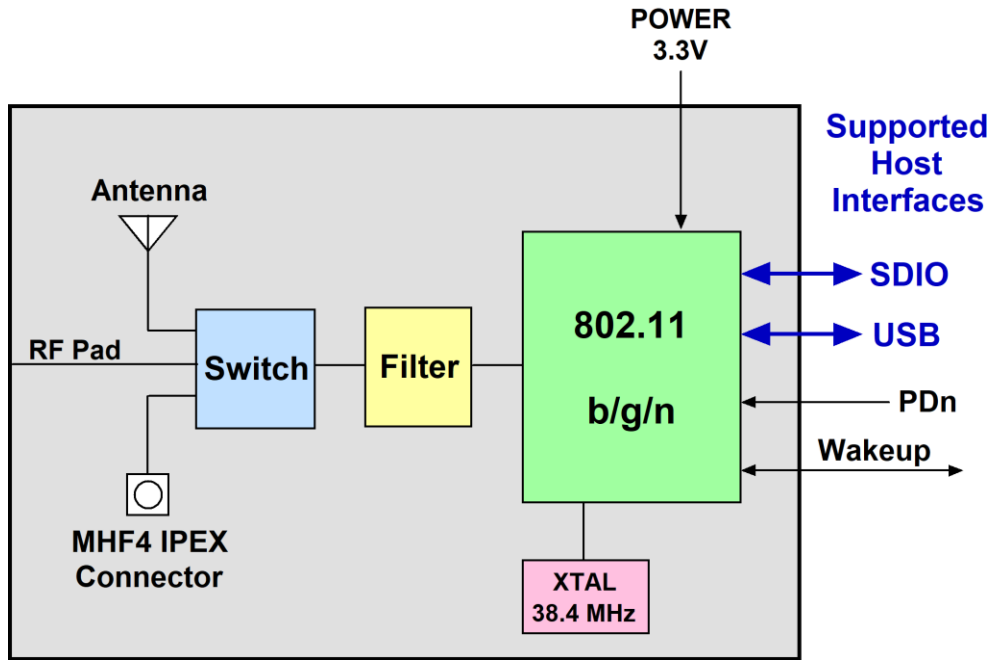


Figure 1: Block Diagram

2.2 Pin Diagram and Description

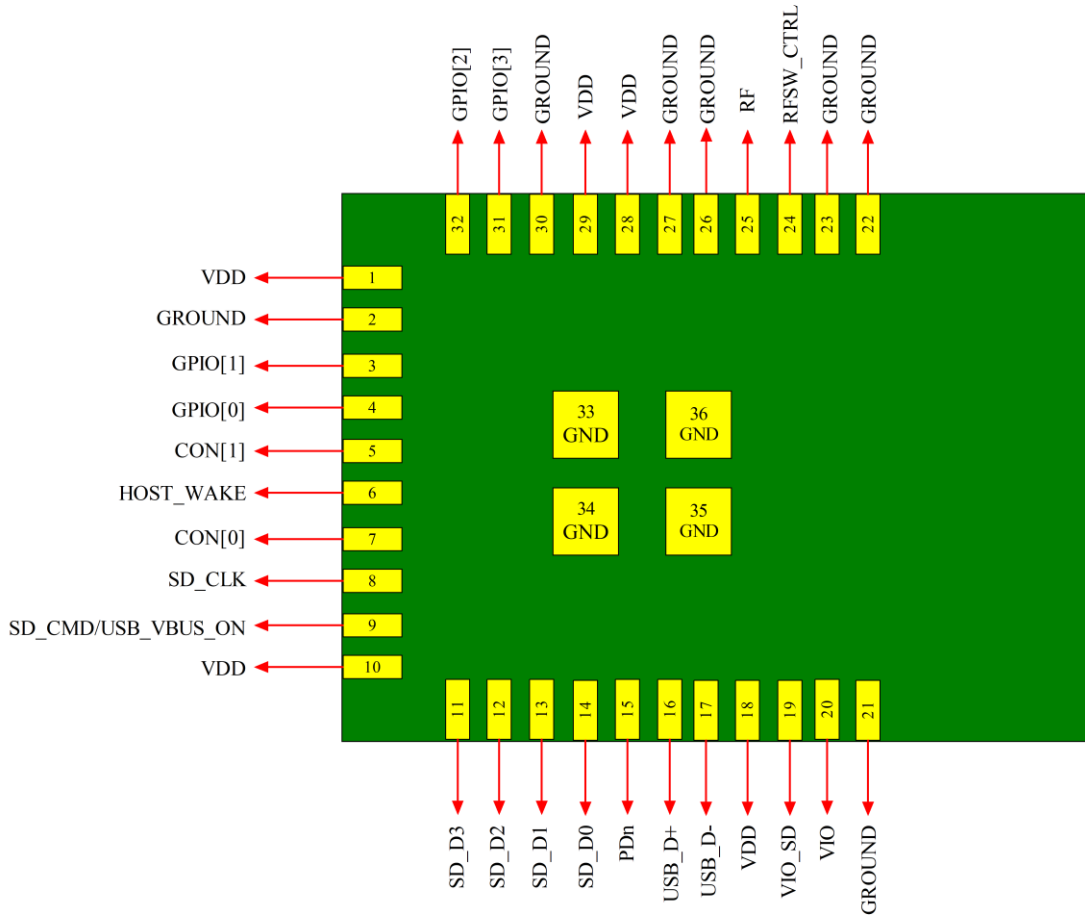


Figure 2 : WM825B00 Module Pin Diagram – Top View

Table 1: Pin Description


Pin No	Pin Name	Type	Supply	Description															
Clock, Reset and Configuration signals																			
8	SD_CLK	I	VIO_SD	SDIO 4-bit Mode: Clock input SDIO 1-bit Mode: Clock input SDIO SPI Mode: Clock input															
6	HOST_WAKE	I	AVDD18	Host-to-SoC Wakeup (input)															
5, 7	CON[1], CON[0]	I	AVDD18	Host Interface Selection <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>CON[1]</th> <th>CON[0]</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>SDIO</td> </tr> <tr> <td>1</td> <td>1</td> <td>USB (default)</td> </tr> </tbody> </table>	CON[1]	CON[0]	Mode	0	0	Reserved	0	1	Reserved	1	0	SDIO	1	1	USB (default)
CON[1]	CON[0]	Mode																	
0	0	Reserved																	
0	1	Reserved																	
1	0	SDIO																	
1	1	USB (default)																	
15	PDn	I	VDD	Full Power-Down (active low) 0 = Full power-down mode 1 = Normal mode Internally Pulled Up with 51K to VDD External host required to drive this pin low for Power-down															
Host Interface, USB (see detailed section)																			
17	USB_DMNS	I/O	VDD	USB Serial Differential Data Negative															
16	USB_DPLS	I/O	VDD	USB Serial Differential Data Positive															
9	SD_CMD/ USB_VBUS_ON	I	VIO_SD	USB Mode: USB_VBUS_ON (input) SDIO 4-bit Mode: Command/response SDIO 1-bit Mode: Command line															
Host Interface, SDIO (see detailed section)																			
8	SD_CLK	I	VIO_SD	SDIO 4-bit Mode: Clock input SDIO 1-bit Mode: Clock input SDIO SPI Mode: Clock input															
9	SD_CMD/ USB_VBUS_ON	I/O	VIO_SD	SDIO 4-bit Mode: Command/response SDIO 1-bit Mode: Command line USB Mode: USB_VBUS_ON (input)															
14	SD_D0	I/O	VIO_SD	SDIO 4-bit Mode: Data line Bit[0] SDIO 1-bit Mode: Data line															

13	SD_D1	I/O	VIO_SD	SDIO 4-bit Mode: Data line Bit[1] SDIO 1-bit Mode: Interrupt SDO is tri-state when SCSn is inactive Enables multiple devices driving SDO line
12	SD_D2	I/O	VIO_SD	SDIO 4-bit Mode: Data line Bit[2] or read wait (optional) SDIO 1-bit Mode: Read wait (optional) SDIO SPI Mode: Reserved
11	SD_D3	I/O	VIO_SD	SDIO 4-bit Mode SDIO Data Line Bit[3] SDIO 1-bit Mode: Reserved SDIO SPI Mode: Card Select (active low)
RF Antenna				
25	RF	I/O	VDD	RF PAD
24	RFSW_CTRL	I	VDD	Selects the external RF pad
GPIO Pins				
4	GPIO[0]	I/O	VIO	*UART Mode: UART_SIN (input), debug only
3	GPIO[1]	I/O	VIO	*UART Mode: UART_SOUT (output), debug only Host Wakeup: SoC-to-Host wakeup (output)
32	GPIO[2]	I/O	VIO	*TWSI EEPROM Mode: SER_CLK Serial interface clock (input/output)
31	GPIO3	I/O	VIO	*TWSI EEPROM Mode: SER_DAT Serial interface data (input/output)
POWER				
1, 10, 18, 28, 29	VDD	Power	3.3V	3.3V Power
19	VIO_SD	Power	VIO_SD	SDIO Power rail 3.3V or 1.8V
20	VIO	Power	VIO	GPIO Power rail 3.3V or 1.8V
Ground Pins				
2, 21, 22, 23,26, 27, 30	GND	Ground	GND	Ground
33, 34, 35, 36	EXPOSED PADS	Ground	GND	Ground

 **Note:** * marked is not available with the current software

2.3 Physical Dimensions and Pad Locations

- Module Physical Size: 12.5 x 16 x 1.76 mm (including shield)
- Solder Pad Size: 0.5 x 0.65 mm
- Pad to Pad Space: 0.4 mm
- Pad Pitch: 0.9 mm
- Last Pad to Module Edge: 0.375 mm
- Pad Finish: ENIG (Electro-less Nickel Immersion Gold)
- Pads: [(Three sides (10 + 11 + 11) + 4 Ground Pads in the middle)]

 For Hardware Application notes, Module dimensions and symbol library files please contact Wi2Wi Sales or send an email to sales@wi2wi.com

3. Electrical Characteristics

Parameter	Test Condition	MIN	TYP	MAX	UNITS
Absolute Maximum Ratings					
Storage Temperature		-40	-	85	°C
Supply Voltage VDD		2.7	3.3	4.2	V
Recommended Operating Conditions					
Operating Temperature	Commercial	0	-	+70	°C
	Extended	-30	-	+85	°C
	Industrial	-40	-	+85	°C
Supply Voltage VDD		3.0	3.3	3.6	V
Current Consumption USB Mode					
Transmit Mode current Consumption	Measurements during Iperf TX with 11Mbps data rate and max TX power dBm	-	369	-	mA
Receive Mode current consumption	Measurements during Iperf RX with 11Mbps data rate	-	90	-	mA
Current consumption in IEEE 802.11 Power Save Mode ¹	Deep Sleep Mode	-	238	-	uA
Current consumption in MH (Mobile Hotspot) mode	MH not beaconing and deep sleep enabled	-	711	-	uA
Current consumption in MH	External Station connected to MH	-	870	-	uA
802.11 RF System Specifications					
Transmit Power Output	Average		17.64		dBm
Transmit Power Output	Peak		24.93		dBm
Receive Sensitivity	1 Mbps	-	-94	-97	dBm
Current Consumption SDIO Mode					
Transmit Mode current Consumption	Measurements during Iperf TX with 11Mbps data rate and 17.9 dBm TX power	-	358	-	mA
Receive Mode current consumption	Measurements during Iperf RX with 11Mbps data rate	-	68	-	mA
Current consumption in IEEE 802.11 Power Save Mode ¹	Deep Sleep Mode	-	99	-	uA
Current consumption in MH (Mobile Hotspot) mode	MH not beaconing and deep sleep enabled	-	0.635	-	mA
Current consumption in MH	External Station connected to MH	-	73	-	mA

Table 2 : Electrical Characteristics

 Note ¹: VIO and VIO_SD are excluded from current measurement.

4. Voltage Domains

Voltage domains and limits of all the signal pins are listed in tables below.

	Min	Typ	Max	Units
V_{IH}	2	-	3.6	V
V_{IL}	(-) 0.3	-	1	V
V_{IHYS}	300	-	-	mV
V_{OH}	2.3	-	-	V
V_{OL}	-	-	0.4	V

Table 3 : 3.3V Voltage Domain Signal Limits

	Min	Typ	Max	Units
V_{IH}	1.2	-	2.1	V
V_{IL}	(-) 0.3	-	0.6	V
V_{IHYS}	250	-	-	mV
V_{OH}	1.22	-	-	V
V_{OL}	-	-	0.4	V

Table 4 : 1.8V Voltage Domain Signal Limits

5. External Connections


Follow the instruction and guidelines for the below different sections

- Power Supply
- Reset
- Configuration
- Host interfaces
- RF path or Antenna path
- GPIO

5.1 Power supply

Module has three power rails, provide proper decoupling and bypass capacitors for these rails.

- VDD
 - Module Digital and RF section power rail (3.3V)
- VIO_SD
 - SDIO Power rail (3.3V or 1.8V)
 - Connect the power rail VIO_SD, even if SDIO interface is not used.
- VIO
 - GPIO Power rail and other digital circuitry inside the module (3.3V or 1.8V)
 - Connect the power rail VIO, even if GPIO is not used

 Connect VIO_SD and VIO to power rail, even if interface is not used. These rails are used internally for other core section. Do not leave it open.

5.2 Reset

The module is reset to its default operating state under the following conditions

- Power-on-Reset (POR)
- Software/Firmware reset
- External pin assertion (PDn)

5.2.1 Internal Reset

The module is reset, and the internal CPU begins the boot sequence when any of the following internal reset events occurs:

- Module receives power and VDD supplies rise (triggers internal POR circuit)
- Host driver issues a soft reset

5.2.2 External PDn Assertion


The module is reset, and the internal CPU begins the boot sequence when the PDn input pin transitions from low to high following the power-up (VDD) sequence.

5.3 Host Configuration

CON [1:0] are host interface selection pins. By default these pins are pulled HIGH internally which selects USB interface. These pins need to be pulled LOW accordingly for other modes. No external circuitry is required to set a configuration bit to 1.

Pin #	Signal Name	Default
5	CON [1]	Internal Pull-up
7	CON [0]	Internal Pull-up

CON[1]	CON[0]	Mode
0	0	Reserved
0	1	Reserved
1	0	SDIO
1	1	USB (default)

 For USB mode, these pins can be left open.

5.4 Host interfaces

Based on the Host configuration pins as shown in section [Host Configuration](#), the interface will be selected.

5.4.1 SDIO interface

Module supports a SDIO interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access this wireless module.

This Module acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine. A unique set of commands are described in the software user guide.

Main features of the SDIO device interface include:

- On-chip memory used for CIS
- Supports 1-bit and 4-bit SDIO transfer modes at the full clock range of 0 to 50 MHz
- Special interrupt register for information exchange
- Allows cards to interrupt host

Pin #	Signal	SDIO Spec	Type
8	SD_CLK	CLK	I
9	SD_CMD	CMD	I/O
14	SD_D0	DAT0	I/O
13	SD_D1	DAT1	I/O
12	SD_D2	DAT2	I/O
11	SD_D3	DAT3	I/O

5.4.2 USB interface


The USB device interface is compliant with the Universal Serial Bus Specification, Revision 2.0, April 27, 2000. A USB host uses the USB cable bus and the USB 2.0 device interface to communicate with the module. A unique set of commands are described in the software user guide.

Main features of the USB device interface include:

- High/full-speed operation (480/12 Mbps)
- Suspend/host resume/device resume (remote wake-up)
- Built-in DMA engine that reduces interrupt loads on the embedded processor and reduces the system bus bandwidth requirement for serving the USB device operation
- Supports Link Power Management (LPM), corresponding host resume, or device resume (remote wakeup) to exit from L1 sleep state

The USB 2.0 device interface is designed with 3.3V signal level pads.

Pin #	Signal	USB Spec	Type	Description
16	USB_DP	D+	I/O	
17	USB_DM	D-	I/O	
9	SD_CMD/USB_VBUS_ON		INPUT	USB VBUS On USB power valid indication Connect to VDD with 51K resistor
		VBUS		Use regulators to convert from VBUS to VDD
		GND		Common Module Ground

 In USB mode, pull SD_CMD/USB_VBUS_ON **HIGH** to VDD with 51K resistor.

5.4.3 Clock

- Module has internal crystal oscillator and requires no external clock source.

5.4.4 Antenna / RF path


- Module has three Antenna options
 - Chip Antenna
 - MHF4 IPEX co-axial connector and
 - RF Pad for the user interface


WM825B00 module has a chip antenna on the module. It also has MHF4 IPEX connector on the module to connect an external antenna. By default, the chip antenna and MHF4 IPEX co-axial connector have antenna diversity feature between them. The antenna diversity can be enabled (or) disabled by the software command.

An External antenna can be connected by using RF pad. Leave RF, RFSW_CTRL pins open, if external antenna is not used.

Pin #	Signal
25	RF
24	RFSW_CTRL

RFSW_CTRL	Antenna Selected
Pull HIGH (Default, on Module)	Diversity between Chip antenna and MHF4 IPEX co-axial connector
Pull LOW	RF pin selected.

 RFSW_CTRL is pulled HIGH to VDD with 51K inside to module. No external Pull-up required on this pin.

 Diversity feature is the practice of using two different antennas with a RF data path to always capture the best wireless signal.

5.4.5 GPIO

 Please note: GPIOs are reserved with current release.

6. WLAN External Host Interface

For connection to a host processor, supports the SDIO HS 4 bit.

6.1 SDIO Timing Diagrams

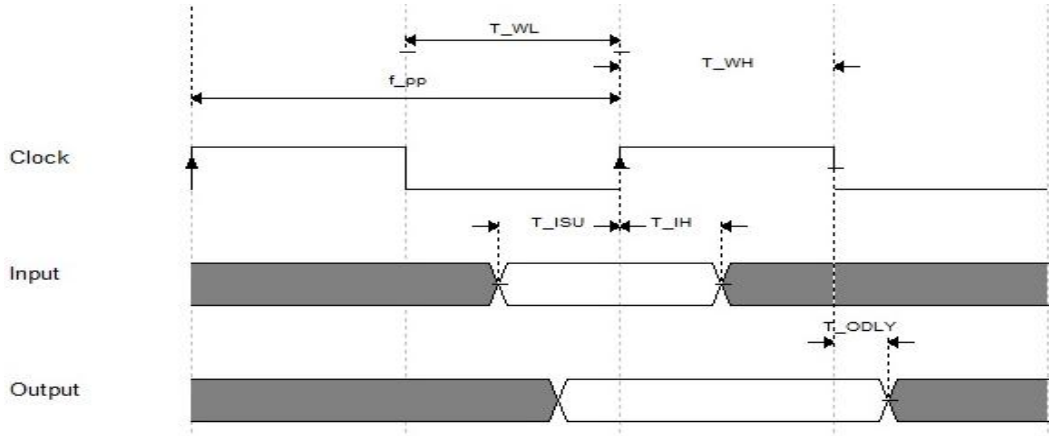


Figure 3: SDIO FS Timing

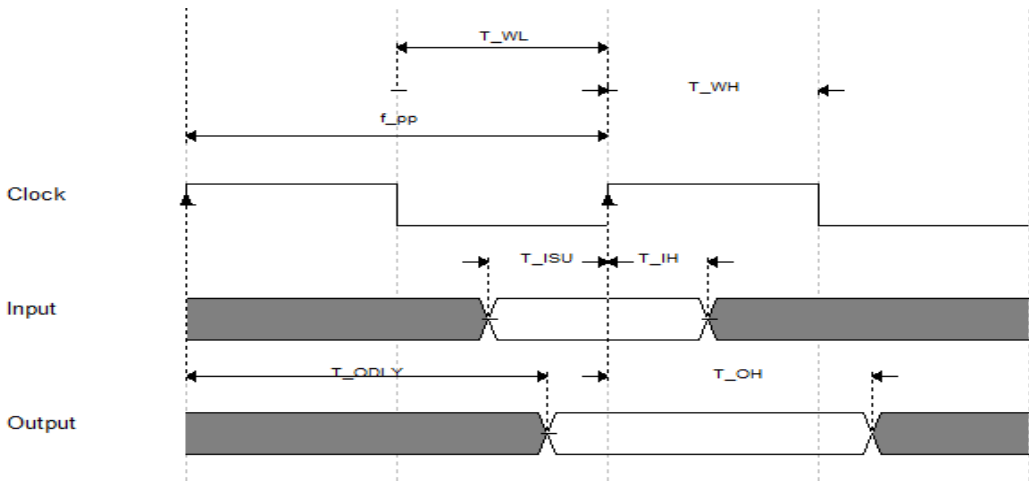




Figure 4: SDIO HS Timing

 The SDIO-SPI CS Signal timing is identical to all other SDIO inputs

Symbol	Parameter	Condition	Min	Typical	Max	Units
f_{pp}	Clock Frequency	Normal	0	--	25	MHz
		High speed	0	--	50	MHz
T_{WL}	Clock Low Time	Normal	10	--	--	ns
		High speed	7	--	--	ns
T_{WH}	Clock High Time	Normal	10	--	--	ns
		High speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High speed	6	--	--	
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High speed	2	--	--	
T_{ODLY}	Output Delay Time	--	0	--	14	ns

Table 5: SDIO Timing Data

 Over full range of values specified in the Recommended Operating Conditions, unless otherwise specified.

7. WLAN Power-Save Modes

Three types of power save modes can be used by the WM825B00. They are Full Power-Down mode, IEEE Power Save mode, and Deep Sleep mode. The key difference between the three modes is the current consumption, and the time it takes to the transition from the power save mode to normal Wi-Fi operation.

7.1 Full Power-Down Mode²


In this mode all internal clocks are shutdown, register and memory states are not maintained. Upon exiting power down mode, a reset is automatically performed and a firmware re-download is required to re-enter any of the other modes.

7.2 IEEE Power Save

This mode puts sections of the Wi-Fi into “sleep with periodic wake” mode. This mode is entered when the appropriate command is sent by the host processor to the Wi-Fi.

The device automatically wakes up to receive beacons periodically, and if there is no traffic indicated for the device, it will go back to sleep. Power consumption is dependent on the DTIM value of the AP it is connected to.

When DTIM=1, the device wakes up every 100ms to receive and acknowledge the beacon from AP to maintain association.

 Note ²: Power Down mode is for USB mode only.

7.3 Deep Sleep

This mode puts the complete Wi-Fi section into deep sleep mode, which is the same as the IEEE mode above except there are no periodic wake-ups to receive beacons. Thus it offers lower power consumption than IEEE mode.

This mode is entered when the host processor sends the appropriate command. In deep sleep mode, the device is not listening for packets or beacons from the AP, so it cannot maintain an association with it.

When the host processor sends a command to take the device out of deep sleep mode, the device will have to re-associate with the AP.

8. Software Specifications

Wi2Wi provides all the drivers needed for operating WM825B00. Wi2Wi provides drivers specific to operating systems in the form of source files, which can be cross compiled for different platforms. Wi2Wi also provides custom driver development services based on customers' requirements. Following is a brief description of the driver features along with the processors, operating systems and host buses. Please contact your sales representative for an up-to-date list of supported OS's and platforms.

Key Features:

- WEP encryption (64 bit/128 bit)
- Simultaneous peer-to-peer and Infrastructure Modes
- RTS/CTS for operation under DCF
- Hardware filtering of 32 multicast addresses
- On-chip Tx and Rx FIFO for maximum throughput
- Open System and Shared Key Authentication Services
- A-MPDU Rx (de-aggregation) and Tx (aggregation)
- Reduced Inter-Frame Spacing (RIFS) receive
- Management information base counters
- Radio resource measurement counters
- Quality of service queues
- Block acknowledgement extension
- Multiple-BSSID and Multiple-Station operation
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis
- Mobile hotspot
- IEEE power save mode
- Deep sleep mode
- Infrastructure and ad-hoc mode
- Rate adaptation
- WPA TKIP security
- WPA2
- Operating System Support
- Driver available for Linux Kernel version 3.10 to 4.14.1

In addition to the end user driver, Wi2Wi also provides, engineering tools needed for production testing and certification.

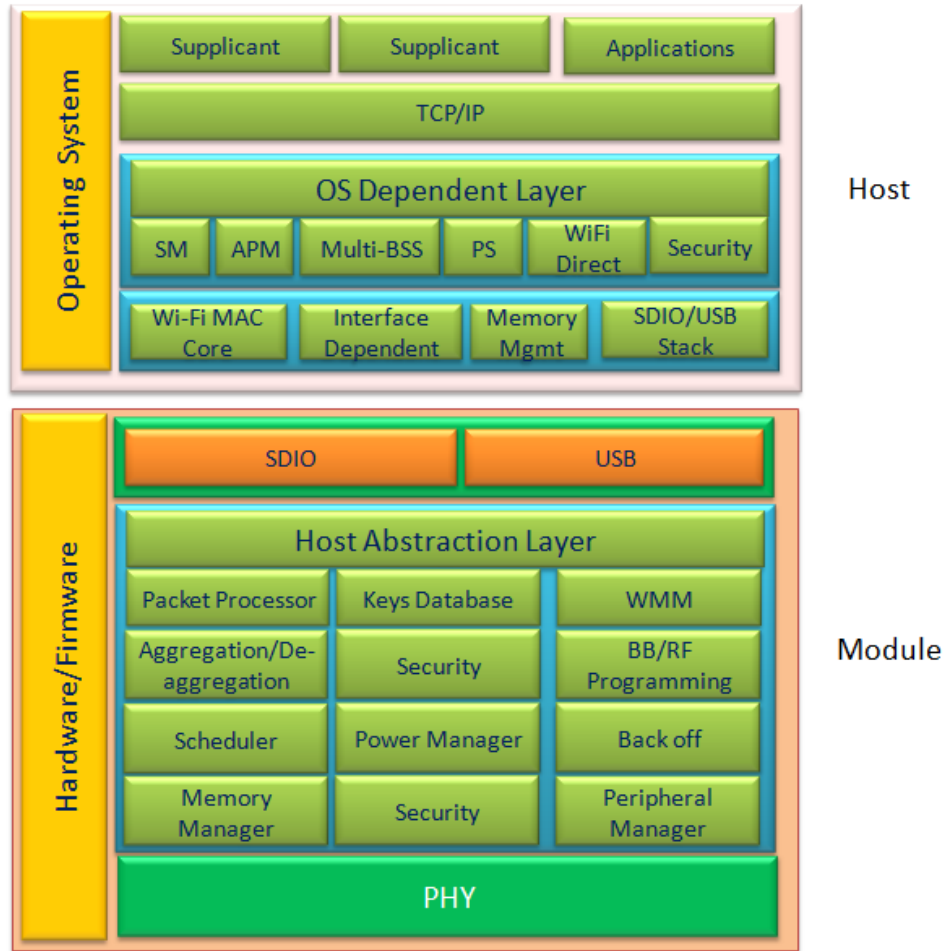


Figure 5: Stack Diagram

8.1 Host Processor

The TCP/IP stack, Ethernet Driver, Security Supplicant, and the 802.11 extensions reside on the host processor. The Hardware Interface driver is partitioned between the host and the module. WLAN firmware for Wi-Fi is downloaded through the host interface (SDIO or USB) by the Hardware Interface Driver at power up. Once the firmware is downloaded, the Data Path and the Control Path between the host and Wi-Fi are established, and information can flow between the two devices.

9. Reference Schematics

The Figure below shows the WM825B00's reference schematics.

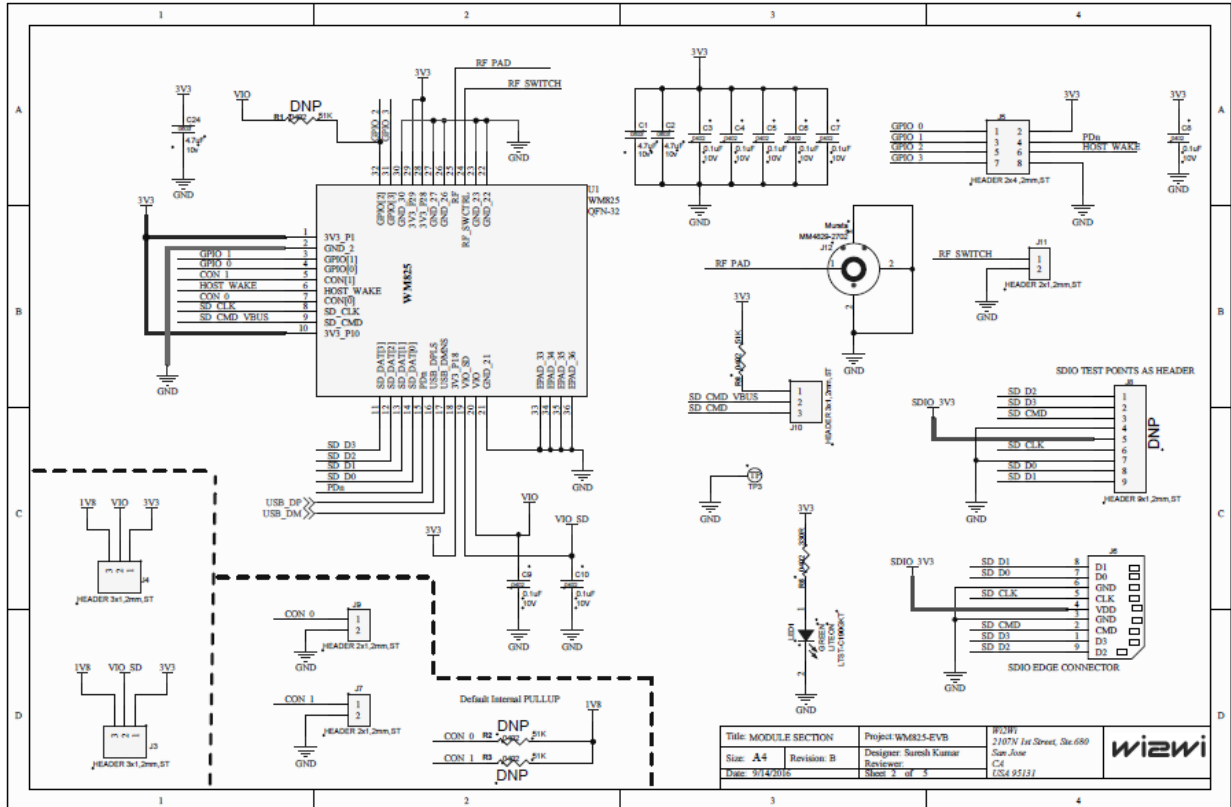


Figure 6: EVB Reference Schematics

Note ²: For complete reference schematics and guidelines, refer Hardware Integration guide.

10. Manufacturing Notes

10.1 Shield Marking

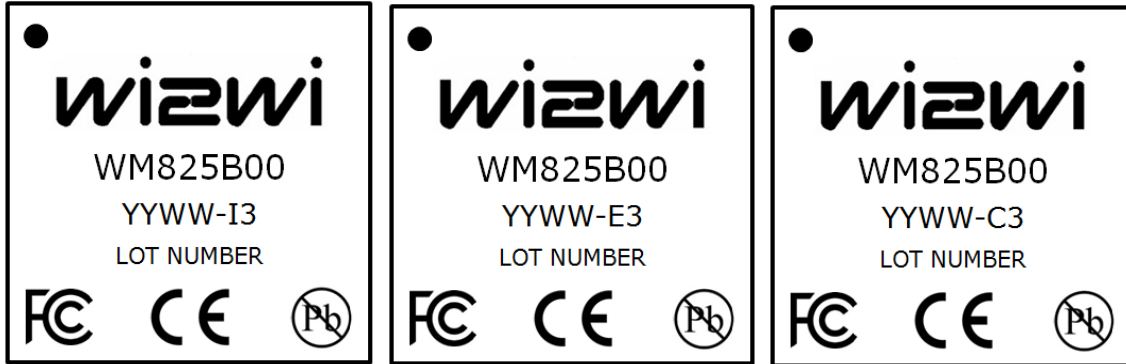


Figure 7: Shield Marking – Top View

YY indicates Year

WW indicates Work Week

- -I indicates Industrial operating temperature range (-40°C to +85°C)
- -E indicates Extended operating temperature range (-30°C to +85°C)
- -C indicates Commercial operating temperature range (0°C to +70°C)
- 3 indicates Chip Antenna and MHF4 IPEX connector

10.2 Storage and Baking Instructions

WM825B00 is an MSL3 qualified package.

- After opening the bag, the parts should be stored as per J-STD-033 standard, and mounted within 168 hours of factory conditions ($\leq 30^{\circ}\text{C}$, 60% RH)
- If the parts have been exposed in transit, they need to be baked at 125°C for 16 hours

10.3 Recommended Reflow Profile

Assembly Guidelines:

1. Follow solder paste manufacturers recommended profile
 - a. All RoHS solder pastes contain the same basic chemistry; however, each manufacturer may have a recommended reflow profile that performs best for their product
2. The profile illustrated below is for reference only
 - a. **There is no one profile that fits all scenarios**
3. Profiles must be dialed in to the specific assembly type
4. ENIG finishes are more susceptible to voids and air entrapment
 - a. Selecting a RoHS solder paste that is “ENIG” compatible is recommended

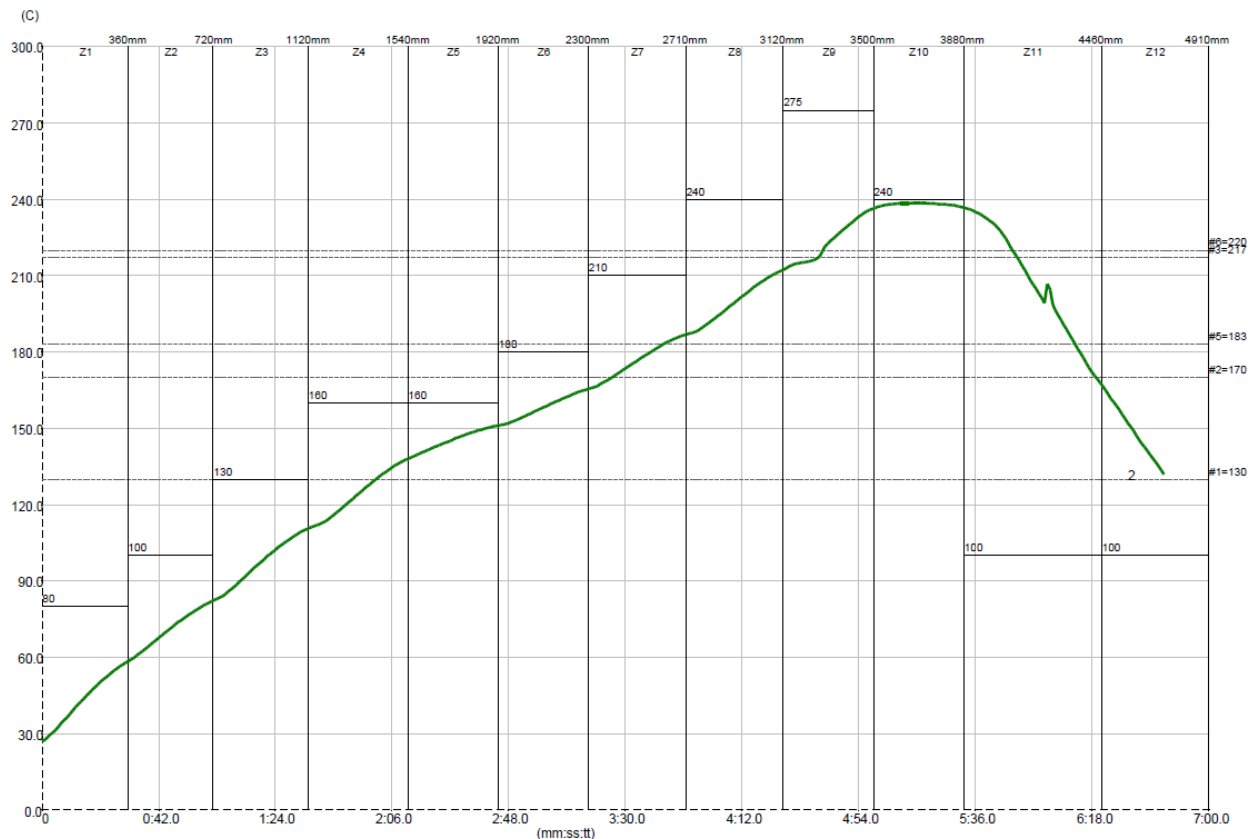


Figure 8: Recommended Reflow Profile

11. Ordering Information

Table 6: Ordering Information for Modules

Part Order Number	Operating Temperature Range	Packaging Method
WM825B00-I3QT	Industrial: -40°C to +85°C	Tray
WM825B00-I3QR	Industrial: -40°C to +85°C	Tape & Reel
WM825B00-E3QT	Extended: -30°C to +85°C	Tray
WM825B00-E3QR	Extended: -30°C to +85°C	Tape & Reel
WM825B00-C3QT	Commercial: 0°C to +70°C	Tray
WM825B00-C3QR	Commercial: 0°C to +70°C	Tape & Reel

Table 7: Ordering Information for Evaluation Kits

Part Order Number	Contents of the Evaluation Kit	Packaging Method
WM825B00-EVK3	WM825B00-I3 Module on Evaluation Board, 2.4 GHz Rubber Duck Antenna, MHF4 IPEX connector cable and USB-A / Micro-AB Cable	Box
WM825B00-DVK3-WBSL	WM825B00 DVK based on Wandboard Solo	Box
WM825B00-DVK3-RP02	WM825B00 DVK based on Raspberry Pi 2	Box
WM825B00-DVK3-RPBP	WM825B00 DVK based on Raspberry Pi Model B+	Box

12. Data Sheet Status

Wi2Wi, Inc. reserves the right to change the specification without prior notice in order to improve the design and supply the best possible product. Updated information, firmware and release notes will be made available on www.wi2wi.com. Please check with Wi2Wi Inc. for the most recent data before initiating or completing a design.

13. Certifications

WM825B00 complies with the following standards:

FCC:	15C
IC:	RSS-247
CE:	EN 300 328 v1.9.1, EN 301 489-1 v1.9.2 EN 301 489-17 v2.2.1, EN 60950-1

FCC Statement:

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Wi2Wi may void the user's authority to operate the equipment.

IC Statement:

English:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

1. This device may not cause harmful interference;
2. This device must accept any interference received, including interference that may cause undesired operation of the device.

Français:

Cet appareil est conforme à Industrie Canada une licence standard RSS exonérés (s). Son fonctionnement est soumis aux deux conditions suivantes:

1. Cet appareil ne doit pas provoquer d'interférences;
2. Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant provoquer un fonctionnement indésirable de l'appareil.

RF Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter must be at least 20 cm from the user and must not be co-located or operating in conjunction with any other antenna or transmitter. The information in this guide may change without notice. The manufacturer assumes no responsibility for any errors that may appear in this guide.

Integrator Guidance:

- All certifications apply to the integrated chip antenna only. Customers using any optional external antenna connecting via the onboard MHF4 IPEX connector or the RF Pad must get their antenna certified themselves.
- Only the antenna(s) described in the filings under this FCC ID or equivalent antenna(s) with equal or lesser gain may be used with this transmitter. Any new antenna type, or higher gain antenna would require a Class II permissive change.
- If the operation of the equipment is for portable use (within 20 cm of user), or where co-location configuration use is required; the end product, including the transmitter will require re-evaluation in accordance to the FCC rules.

Labeling:

The final end product must be labeled in a visible area with the following text:

“Contains FCC ID: U9RWM825, IC: 7089A-WM825”, where:

- “U9RWM825” is the approved FCC ID of this module
- “7089A-WM825” is the approved IC ID of this module

The grantee's FCC/IC ID can be used only when all FCC/IC compliance requirements are met.

14. References

14.1 Specifications

IEEE 802.11 b/g/n Wireless LAN Specification
SDIO HS 4-bit Specification

14.2 Trademarks, Patents and Licenses

Trademarks: Wi-Fi

14.3 Disclosures

WM825B00-EVK3: Evaluation Kit
WM825B00-DVK3: Development Kit

The specification maximum and minimum limits presented herein are those guaranteed when the unit is integrated into the Wi2Wi's Development System. These limits are to serve as representative performance characteristics of the WM825B00 when properly designed into a customer's product. Wi2Wi makes no warranty, implied or otherwise specified, with respect to design and performance characteristics presented in this specification when used in customer designs.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Wi2Wi:](#)

[WM825B00-E3QR](#) [WM825B00-I3QT](#) [WM828CC6-E6QR](#) [WM825B00-C3QT](#) [WM825B00-I3QR](#) [WM825B00-E3QT](#)
[WM828CC6-E6QT](#) [WM825B00-C3QR](#)