

Inverter Grade Thyristors (Stud Version), 300 A



TO-118 (TO- 209AE)

FEATURES

- Center amplifying gate
- High surge current capability
- Low thermal impedance
- High speed performance
- Compression bonding
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?999912


RoHS
COMPLIANT

TYPICAL APPLICATIONS

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

PRIMARY CHARACTERISTICS	
$I_{T(AV)}$	300 A
V_{DRM}/V_{RRM}	400 V, 800 V, 1200 V
V_{TM}	2.16 V
I_{TSM} at 50 Hz	3000 A
I_{TSM} at 60 Hz	3150 A
I_{GT}	200 mA
T_J	-40 °C to 125 °C
T_C	65 °C
Package	TO-118 (TO-209AE)
Circuit configuration	Single SCR

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		300	A
	T_C	65	°C
$I_{T(RMS)}$		471	A
I_{TSM}	50 Hz	7950	
	60 Hz	8320	
I^2t	50 Hz	316	kA ² s
	60 Hz	288	
V_{DRM}/V_{RRM}		400 to 1200	V
t_q		10 to 20	µs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST303S	04	400	500	50
	08	800	900	
	12	1200	1300	

**CURRENT CARRYING CAPABILITY**

FREQUENCY							UNITS
50 Hz	670	470	1050	940	5240	4300	A
400 Hz	480	330	1021	710	1800	1270	
1000 Hz	230	140	760	470	730	430	
2500 Hz	35	-	150	-	90	-	
Recovery voltage V _R	50		50		50		V
Voltage before turn-on V _D	V _{DRM}		V _{DRM}		V _{DRM}		
Rise of on-state current di/dt	50		-		-		A/μs
Case temperature	40	65	40	65	40	65	°C
Equivalent values for RC circuit	10/0.47		10/0.47		10/0.47		Ω/μF

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave			300	A
					65	°C
Maximum RMS on-state current	I _{T(RMS)}	DC at 45 °C case temperature			471	A
Maximum peak, one half cycle, non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	7950	
		t = 8.3 ms			8320	
		t = 10 ms	100 % V _{RRM} reapplied		6690	
		t = 8.3 ms			7000	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		316	kA ² s
		t = 8.3 ms		288		
		t = 10 ms	100 % V _{RRM} reapplied	224		
		t = 8.3 ms		204		
Maximum I ² √t for fusing	I ² √t	t = 0.1 ms to 10 ms, no voltage reapplied			3160	kA ² √s
Maximum peak on-state voltage	V _{TM}	I _{TM} = 1255 A, T _J = T _J maximum, t _p = 10 ms sine wave pulse			2.16	V
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)} < I < π × I _{T(AV)}), T _J = T _J maximum			1.44	
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.46	
Low level value of forward slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)} < I < π × I _{T(AV)}), T _J = T _J maximum			0.57	mΩ
High level value of forward slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum			0.56	
Maximum holding current	I _H	T _J = 25 °C, I _T > 30 A			600	
Typical latching current	I _L	T _J = 25 °C, V _A = 12 V, R _a = 6 Ω, I _G = 1 A			1000	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$ $I_{TM} = 2 \times di/dt$	1000	A/μs
Typical delay time	t_d	$T_J = 25$ °C, $V_{DM} = \text{Rated } V_{DRM}$, $I_{TM} = 50$ A DC, $t_p = 1$ μs Resistive load, gate pulse: 10 V, 5 Ω source	0.80	μs
Maximum turn-off time	minimum	$T_J = T_J$ maximum, $I_{TM} = 550$ A, commutating $di/dt = 40$ A/μs $V_R = 50$ V, $t_p = 500$ μs, $dV/dt = 200$ V/μs	10	
	maximum		20	

**BLOCKING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % V_{DRM} , higher value available on request	500	V/ μ s
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	50	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	60	W
Maximum average gate power	$P_{G(AV)}$		10	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	A
Maximum peak positive gate voltage	$+V_{GM}$		20	V
Maximum peak negative gate voltage	$-V_{GM}$		5	
Maximum DC gate current required to trigger	I_{GT}	$T_J = 25$ °C, $V_A = 12$ V, $R_a = 6$ Ω	200	mA
Maximum DC gate voltage required to trigger	V_{GT}		3	V
Maximum DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied	20	mA
Maximum DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T_J		-40 to +125	°C
Maximum storage temperature range	T_{Stg}		-40 to +150	
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.10	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, flat and greased	0.03	
Mounting force, ± 10 %		Non-lubricated threads	48.5 (425)	N · m (lbf · in)
Approximate weight			535	g
Case style		See dimensions - link at the end of datasheet	TO-118 (TO-209AE)	

 ΔR_{thJ-hs} CONDUCTION

CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.011	0.008	$T_J = T_J$ maximum	K/W
120°	0.013	0.014		
90°	0.017	0.018		
60°	0.025	0.026		
30°	0.041	0.042		

Note

- The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

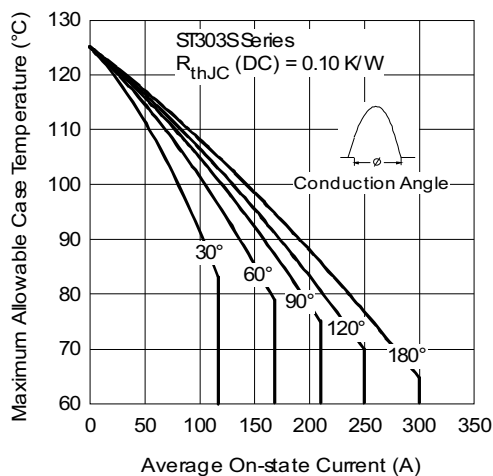


Fig. 1 - Current Ratings Characteristics

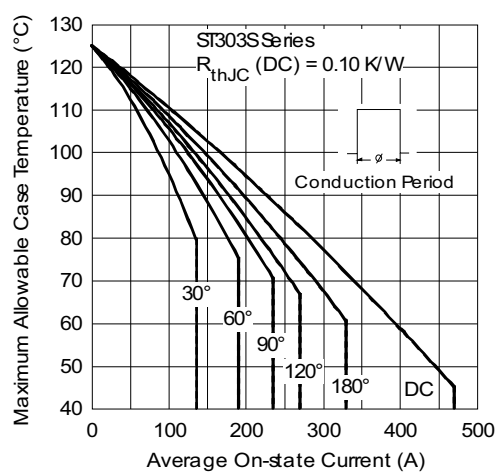


Fig. 2 - Current Ratings Characteristics

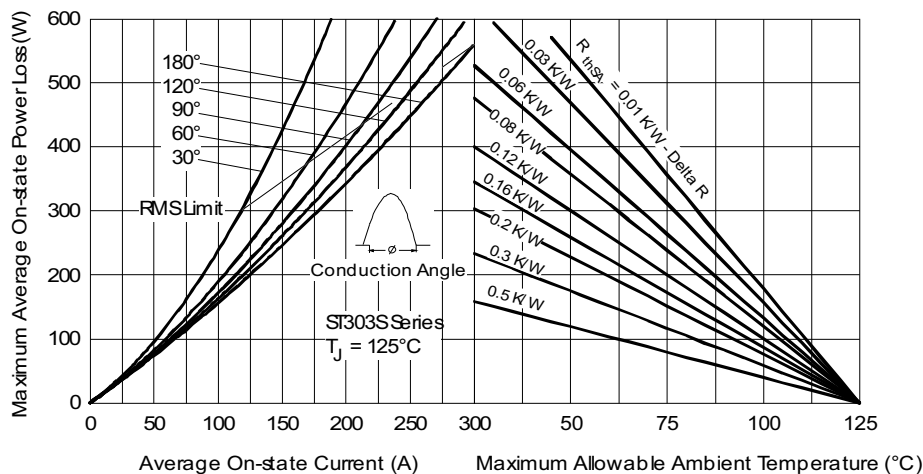


Fig. 3 - On-State Power Loss Characteristics

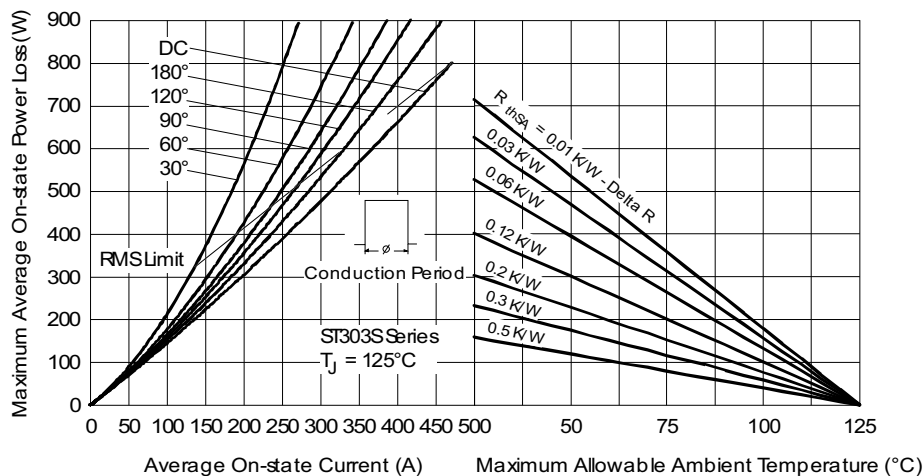


Fig. 4 - On-State Power Loss Characteristics

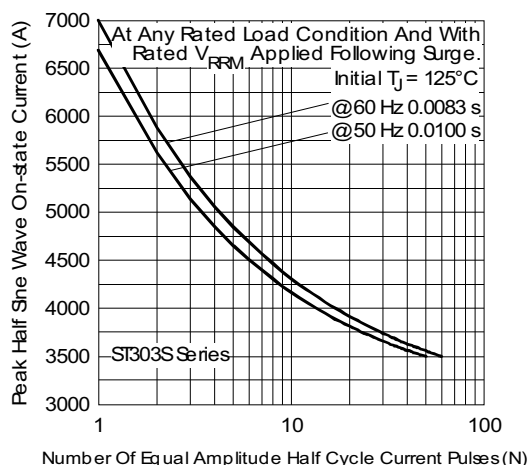


Fig. 5 - Maximum Non-Repetitive Surge Current

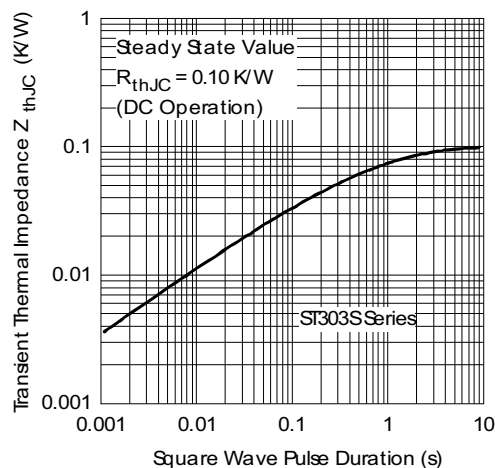
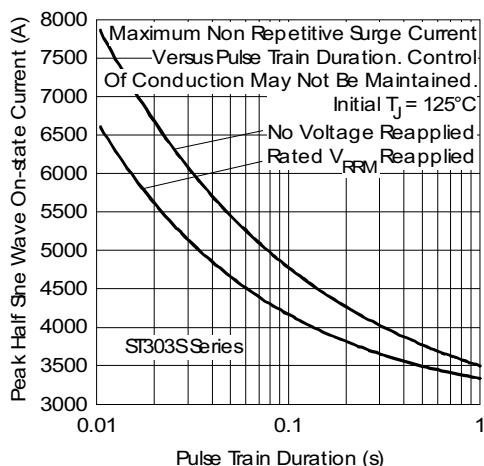

Fig. 8 - Thermal Impedance Z_{thJC} Characteristics


Fig. 6 - Maximum Non-Repetitive Surge Current

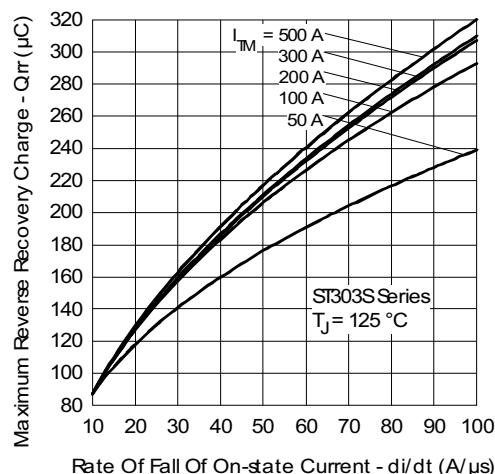


Fig. 9 - Reverse Recovered Charge Characteristics

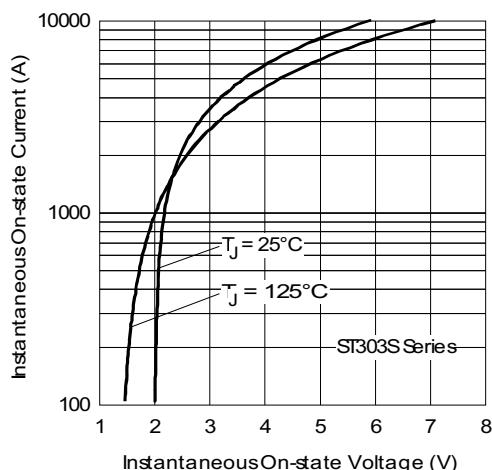


Fig. 7 - On-State Voltage Drop Characteristics

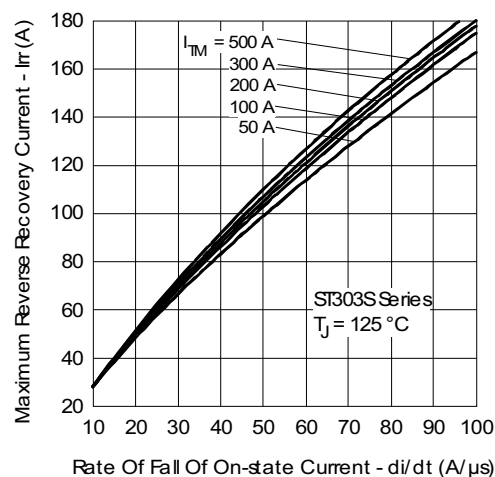


Fig. 10 - Reverse Recovery Current Characteristics

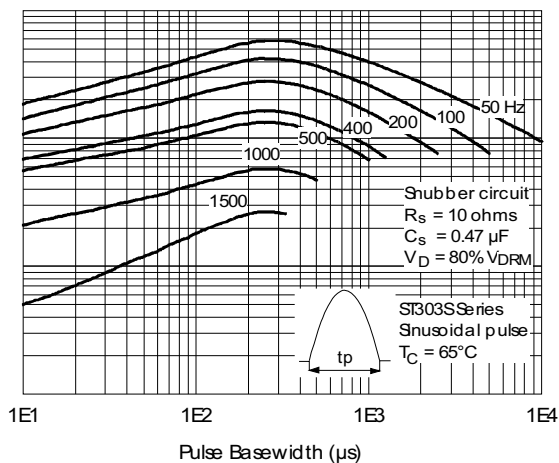
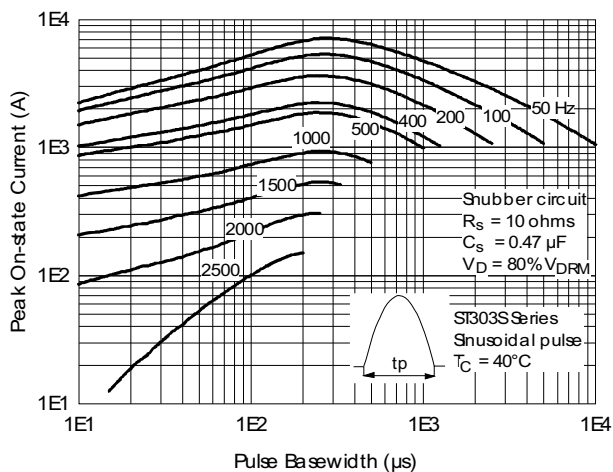


Fig. 11 - Frequency Characteristics

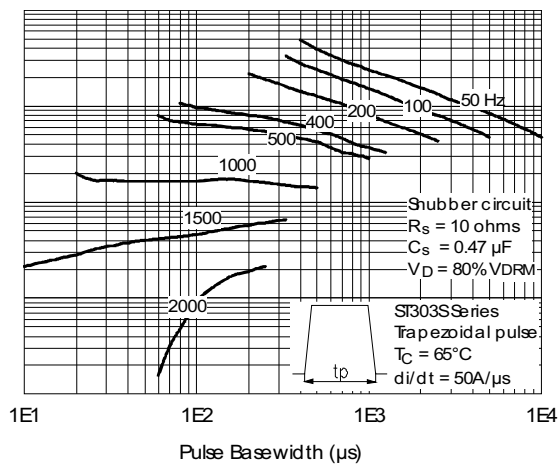
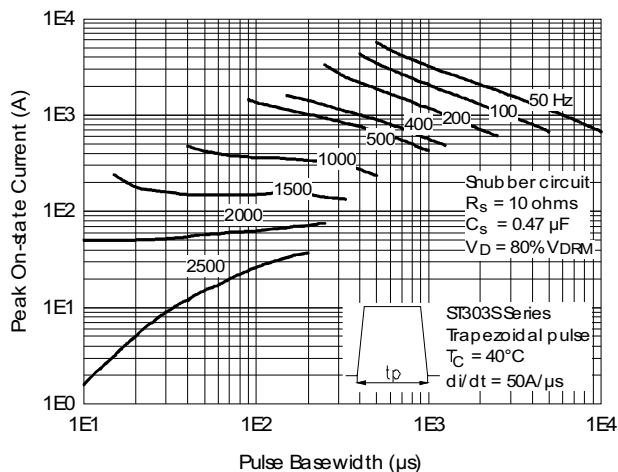


Fig. 12 - Frequency Characteristics

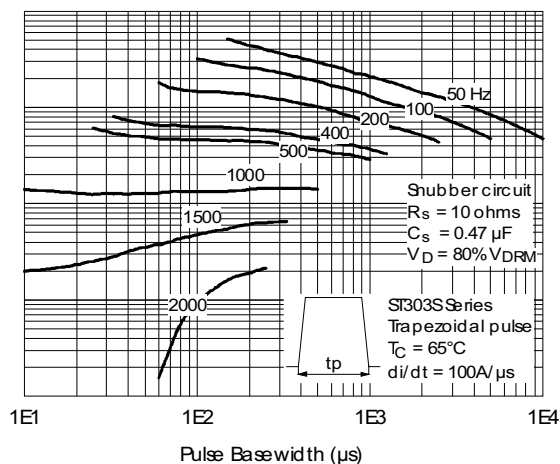
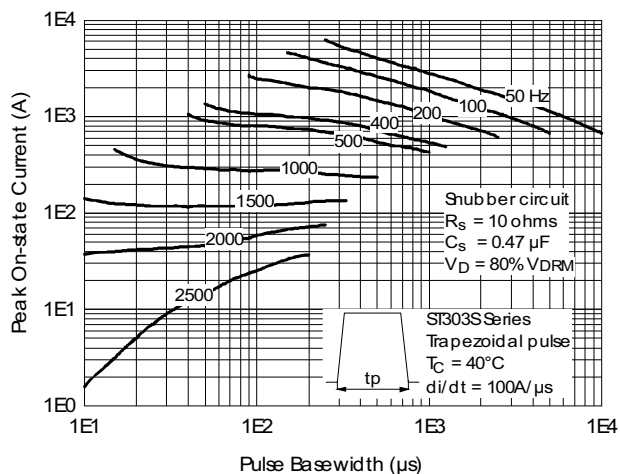


Fig. 13 - Frequency Characteristics

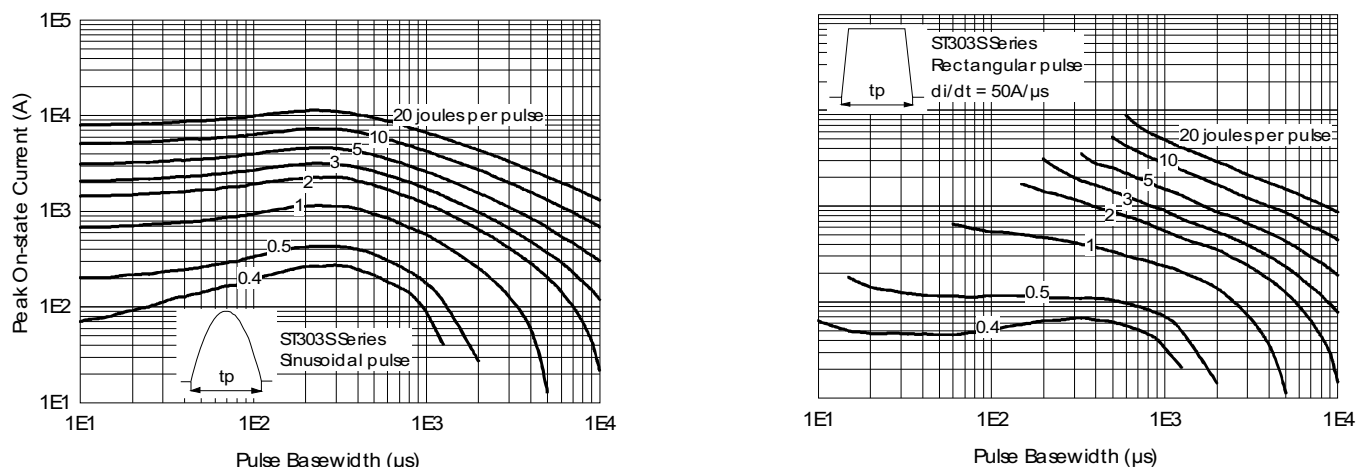


Fig. 14 - Maximum On-State Energy Power Loss Characteristics

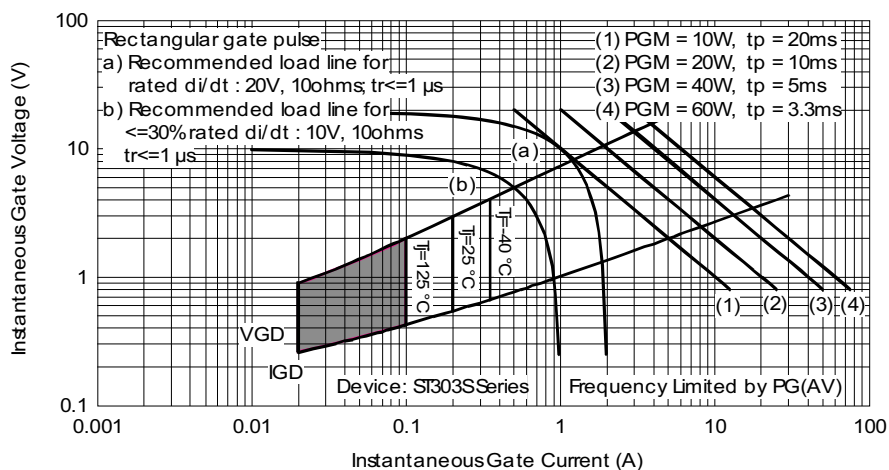


Fig. 15 - Gate Characteristics



ORDERING INFORMATION TABLE

Device code	VS-	ST	30	3	S	12	P	F	K	0	P
	1	2	3	4	5	6	7	8	9	10	11

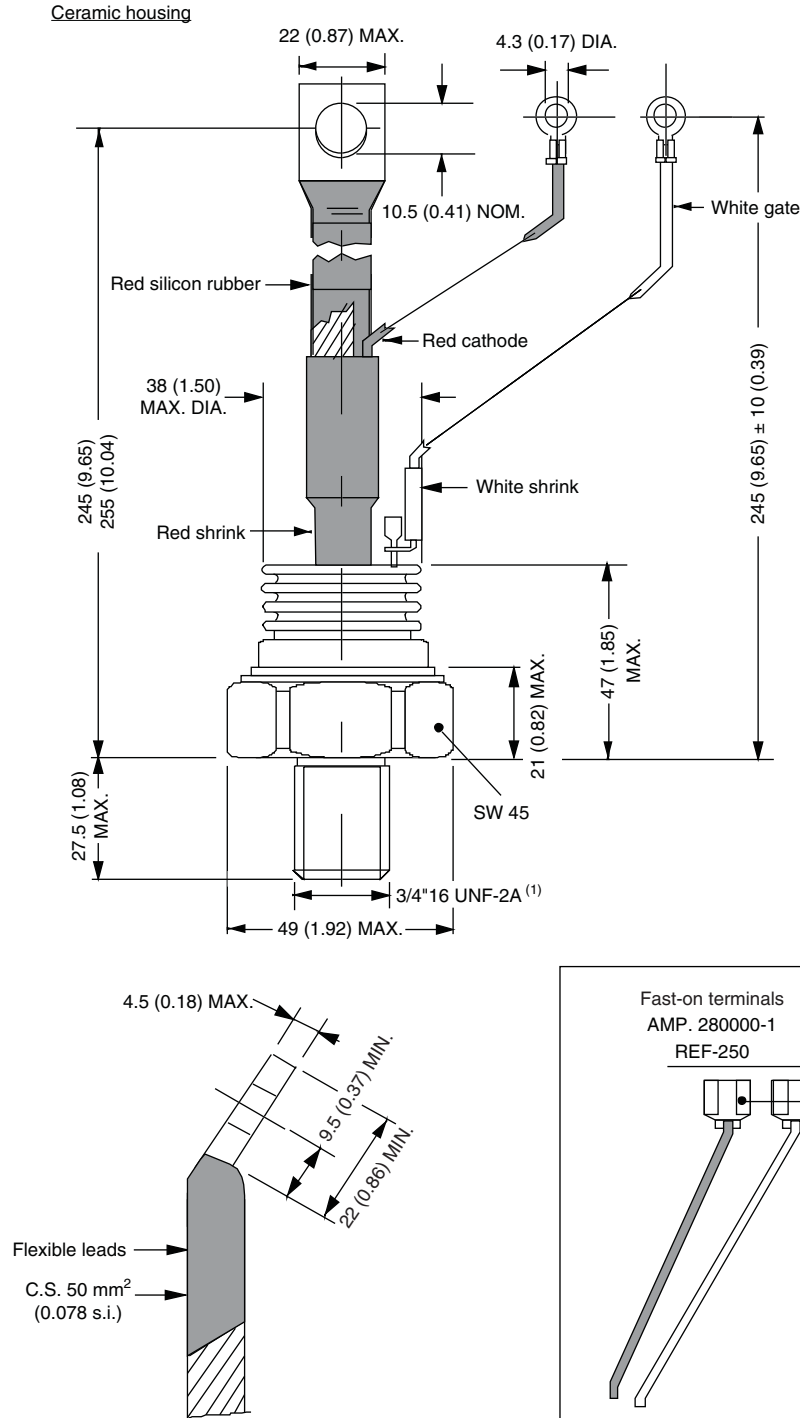
- 1 - Vishay Semiconductors product
- 2 - Thyristor
- 3 - Essential part number
- 4 - 3 = fast turn-off
- 5 - S = compression bonding stud
- 6 - Voltage code x 100 = V_{RRM}
(see Voltage Ratings table)
- 7 - P = stud base 3/4" 16UNF-2A
- 8 - Reapplied dV/dt code (for t_q test condition)
- 9 - t_q code
- 10 - 0 = eyelet terminals
(gate and auxiliary cathode leads)
1 = fast-on terminals
(gate and auxiliary cathode leads)
- 11 - None = standard production
P = lead (Pb)-free

dV/dt - t_q combinations available		
	dV/dt (V/ μ s)	200
t_q (μ s) up to 800 V	10	FN
	15	FL
	20	FK
t_q (μ s) only for 1000/1200 V	20	FK

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95080

TO-209AE (TO-118)

DIMENSIONS in millimeters (inches)



Note

⁽¹⁾ For metric device: M24 x 1.5 - length 21 (0.83) maximum



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