




Power MOSFET, 57 A



SOT-227

FEATURES

- Fully isolated package
- Easy to use and parallel
- Low on-resistance
- Dynamic dV/dt rating
- Fully avalanche rated
- Simple drive requirements
- Low gate charge device
- Low drain to case capacitance
- Low internal inductance
- Designed for industrial level
- UL approved file E78996 
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS
COMPLIANT

PRODUCT SUMMARY

V_{DS}	500 V
$R_{DS(on)}$	0.08 Ω
I_D	57 A
Type	Modules - MOSFET
Package	SOT-227

DESCRIPTION

Third Generation Power MOSFETs from Vishay Semiconductors provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-227 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 500 W. The low thermal resistance of the SOT-227 contribute to its wide acceptance throughout the industry.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Continuous drain current at V_{GS} 10 V	I_D	$T_C = 25^\circ\text{C}$	57	A
		$T_C = 100^\circ\text{C}$	36	
Pulsed drain current	$I_{DM}^{(1)}$		228	
Power dissipation	P_D	$T_C = 25^\circ\text{C}$	625	W
Linear derating factor			5.0	W/ $^\circ\text{C}$
Gate to source voltage	V_{GS}		± 20	V
Single pulse avalanche energy	$E_{AS}^{(2)}$		725	mJ
Avalanche current	$I_{AR}^{(1)}$		57	A
Repetitive avalanche energy	$E_{AR}^{(1)}$		62.5	mJ
Peak diode recovery dV/dt	dV/dt ⁽³⁾		10	V/ns
Operating junction and storage temperature range	T_J, T_{Stg}		- 55 to + 150	$^\circ\text{C}$
Insulation withstand voltage (AC-RMS)	V_{ISO}		2.5	kV
Mounting torque		M4 screw	1.3	Nm

Notes

- (1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
 (2) Starting $T_J = 25^\circ\text{C}$, $L = 446 \mu\text{H}$, $R_g = 25 \Omega$, $I_{AS} = 57 \text{ A}$ (see fig. 12)
 (3) $I_{SD} \leq 57 \text{ A}$, $dI/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

**THERMAL AND MECHANICAL SPECIFICATIONS**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Junction and storage temperature range	T_J, T_{Stg}		- 55	-	150	°C
Junction to case	R_{thJC}		-	-	0.20	°C/W
Case to heatsink	R_{thCS}	Flat, greased surface	-	0.05	-	
Weight			-	30	-	g
Mounting torque			-	-	1.3	Nm
Case style		SOT-227				

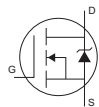
ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ °C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}$	500	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25 °C , $I_D = 1\text{ mA}$	-	0.62	-	V/°C
Static drain to source on-resistance	$R_{DS(on)}^{(1)}$	$V_{GS} = 10\text{ V}, I_D = 34\text{ A}$	-	-	0.08	Ω
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 34\text{ A}$	43	-	-	S
Drain to source leakage current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	μA
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$	-	-	500	
Gate to source forward leakage	I_{GSS}	$V_{GS} = 20\text{ V}$	-	-	200	nA
Gate to source reverse leakage		$V_{GS} = -20\text{ V}$	-	-	- 200	
Total gate charge	Q_g	$I_D = 57\text{ A}$	-	225	338	nC
Gate to source charge	Q_{gs}	$V_{DS} = 400\text{ V}$	-	51	77	
Gate to drain ("Miller") charge	Q_{gd}	$V_{GS} = 10\text{ V}$; see fig. 6 and 13 ⁽¹⁾	-	98	147	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$	-	32	-	ns
Rise time	t_r	$I_D = 57\text{ A}$	-	152	-	
Turn-off delay time	$t_{d(off)}$	$R_g = 2.0\text{ }\Omega$ (internal)	-	108	-	
Fall time	t_f	$R_D = 4.3\text{ }\Omega$, see fig. 10 ⁽¹⁾	-	118	-	
Internal source inductance	L_S	Between lead, and center of die contact	-	5.0	-	nH
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	-	10 000	-	pF
Output capacitance	C_{oss}	$V_{DS} = 25\text{ V}$	-	1500	-	
Reverse transfer capacitance	C_{rss}	$f = 1.0\text{ MHz}$, see fig. 5	-	50	-	

Note

⁽¹⁾ Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

SOURCE-DRAIN RATINGS AND CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous source current (body diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	57	A
Pulsed source current (body diode)	$I_{SM}^{(1)}$		-	-	228	
Diode forward voltage	$V_{SD}^{(2)}$	$T_J = 25\text{ °C}, I_S = 57\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ °C}, I_F = 57\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$ ⁽²⁾	-	901	1351	ns
Reverse recovery charge	Q_{rr}		-	15	23	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes

⁽¹⁾ Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

⁽²⁾ Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

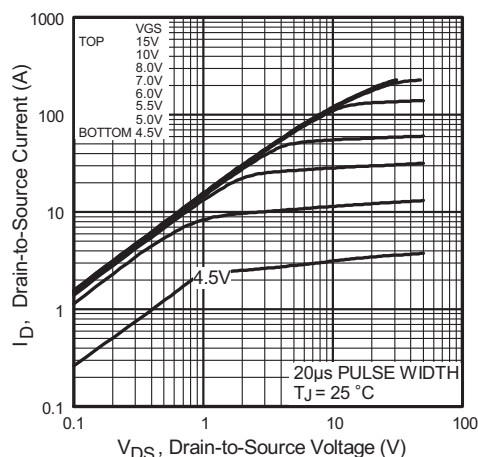


Fig. 1 - Typical Output Characteristics

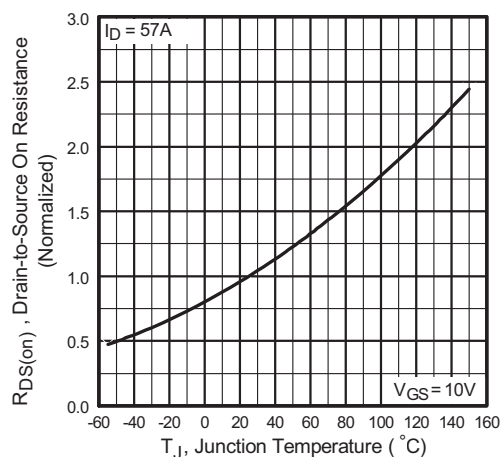


Fig. 4 - Normalized On-Resistance vs. Temperature

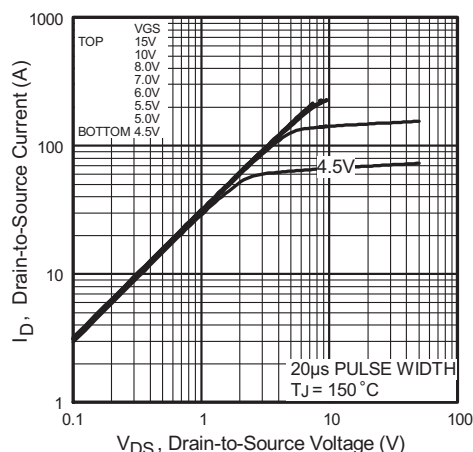


Fig. 2 - Typical Output Characteristics

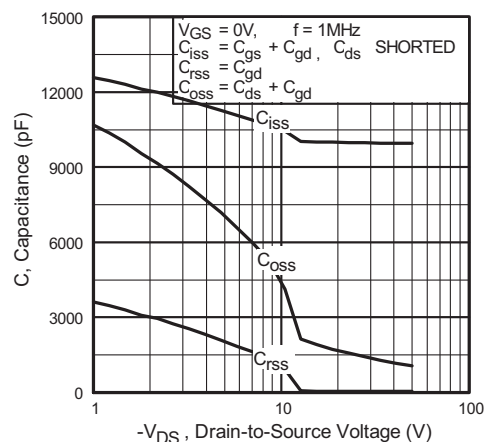


Fig. 5 - Typical Capacitance vs. Drain to Source Voltage

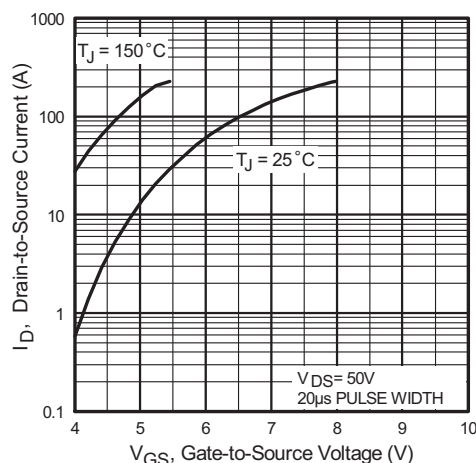


Fig. 3 - Typical Transfer Characteristics

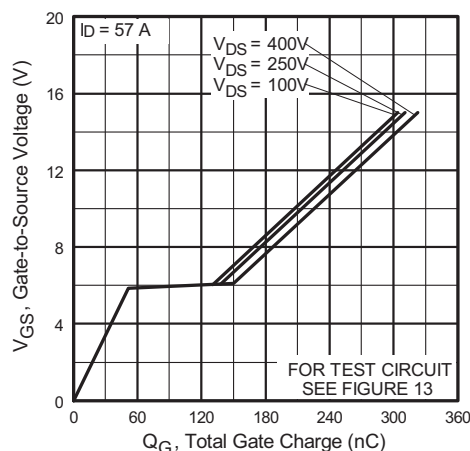


Fig. 6 - Typical Gate Charge vs. Gate to Source Voltage

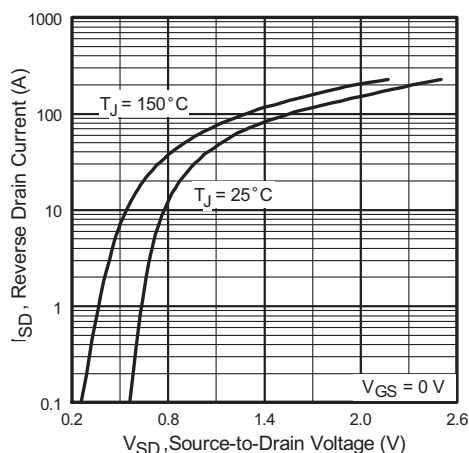


Fig. 7 - Typical Source Drain Diode Forward Voltage

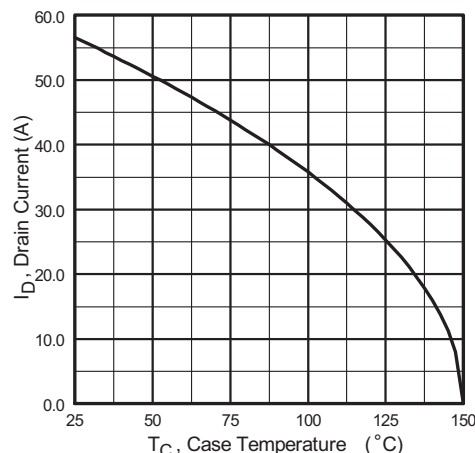


Fig. 9 - Maximum Drain Current vs. Case Temperature

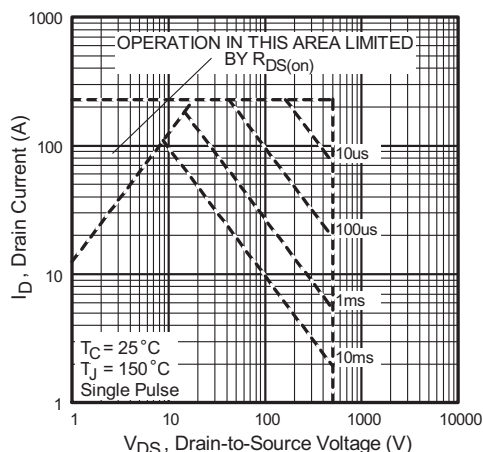


Fig. 8 - Maximum Safe Operating Area

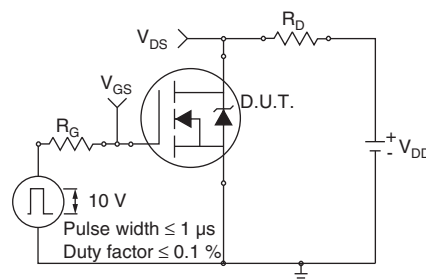


Fig. 10a - Switching Time Test Circuit

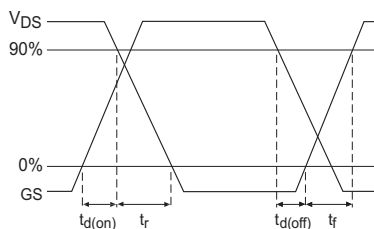


Fig. 10b - Switching Time Waveforms

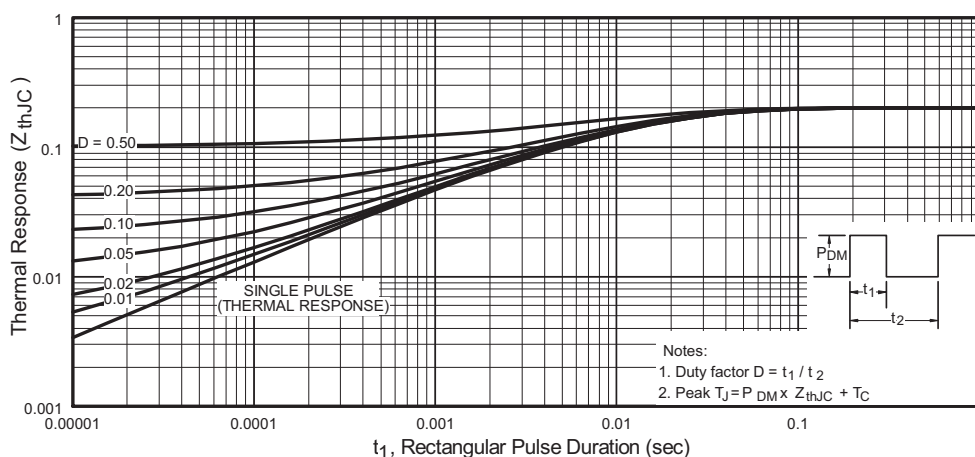


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction to Case

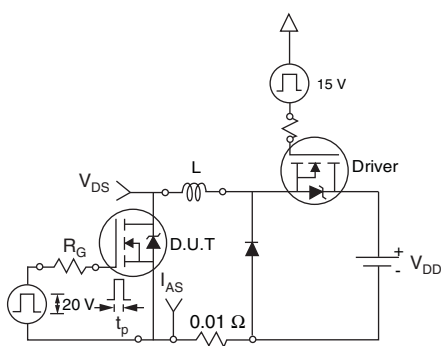


Fig. 12a - Unclamped Inductive Test Circuit

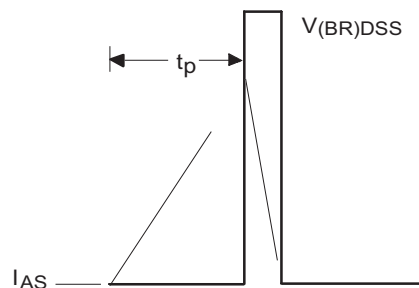


Fig. 12b - Unclamped Inductive Waveforms

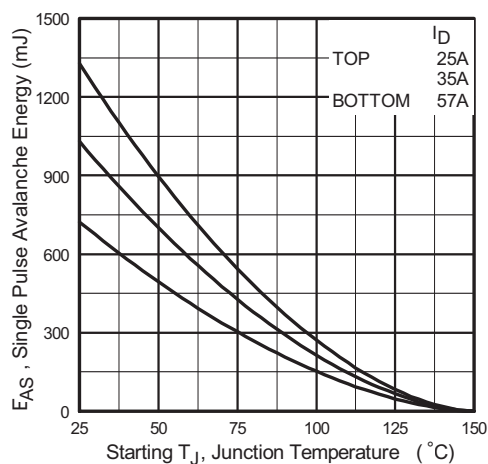


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

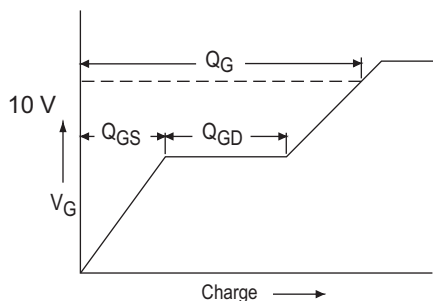


Fig. 13a - Basic Gate Charge Waveform

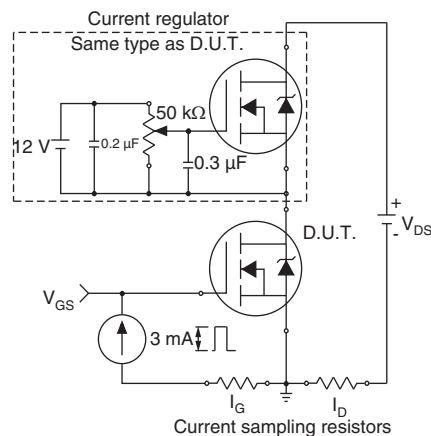


Fig. 13b - Gate Charge Test Circuit

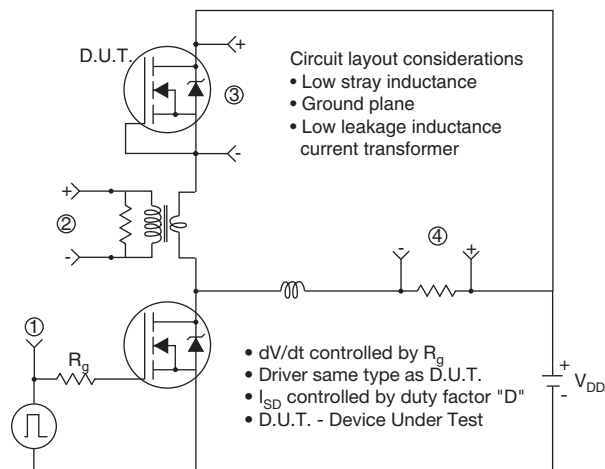
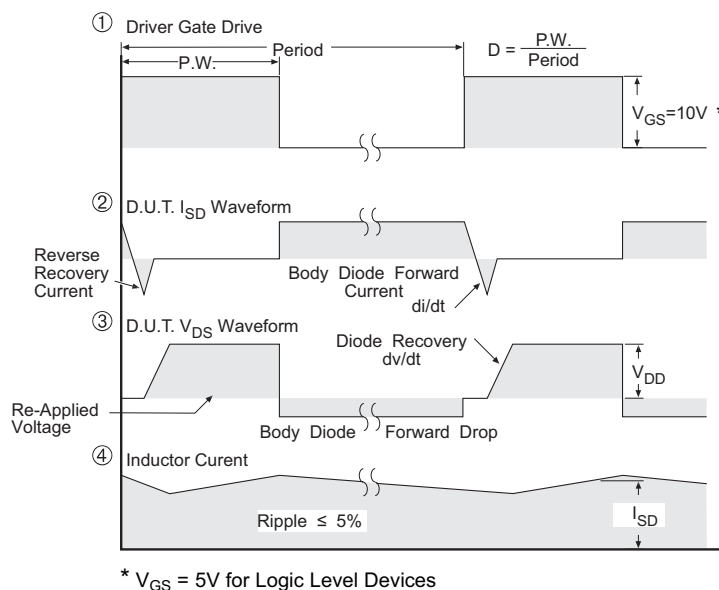


Fig. 13c - Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig. 14 - For N-Channel Power MOSFETs



ORDERING INFORMATION TABLE

Device code	VS-	F	A	57	S	A	50	LC	P
	1	2	3	4	5	6	7	8	9

- 1** - Vishay Semiconductors product
- 2** - Power MOSFET
- 3** - Generation 3, MOSFET silicon, DBC construction
- 4** - Current rating (57 = 57 A)
- 5** - Single switch (see Circuit Configuration table)
- 6** - SOT-227
- 7** - Voltage rating (50 = 500 V)
- 8** - Low charge
- 9** - P = Lead (Pb)-free

CIRCUIT CONFIGURATION		
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Single switch no diode	S	<p>Lead assignment</p>

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95036
Packaging information	www.vishay.com/doc?95037

DIMENSIONS in millimeters (inches)



- Dimensioning and tolerancing per ANSI Y14.5M-1982
- Controlling dimension: millimeter



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