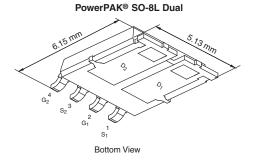
SQJ963EP



Vishay Siliconix

Automotive Dual P-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	- 60				
$R_{DS(on)} (\Omega)$ at $V_{GS} = -10 V$	0.085				
$R_{DS(on)} (\Omega)$ at $V_{GS} = -4.5 V$	0.115				
I _D (A) per leg	- 8				
Configuration	Dual				

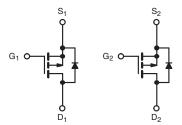


FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- TrenchFET[®] Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS COMPLIANT HALOGEN FREE



P-Channel MOSFET P-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ963EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _C =	= 25 °C, unles	s otherwise noted	I)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage Gate-Source Voltage		V _{DS}	- 60	V
		V _{GS}	± 20	v
Continuous Drain Current	$T_C = 25 \ ^{\circ}C^a$	1	- 8	
Continuous Drain Current	T _C = 125 °C	Ι _D	- 7	
Continuous Source Current (Diode Conduction) ^a		IS	- 8	A
Pulsed Drain Current ^b		I _{DM}	- 25	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	- 20	
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	20	mJ
Maximum Dawar Dissinction ^b	T _C = 25 °C	D	27	10/
Maximum Power Dissipation ^b	power Dissipation ^b P_D P_D W	vv		
Operating Junction and Storage Temperature Range	; ;	T _J , T _{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) ^{e, f}			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	85	°C/W
Junction-to-Case (Drain)		R _{thJC}	5.5	C/VV

Notes

- a. Package limited.
- b. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.
- e. See solder profile (<u>www.vishav.com/doc?73257</u>). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static					I			
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	0 V, I _D = - 250 μA	- 60	-	-	v	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = - 250 μA	- 1.5	- 2.0	- 2.5	v	
Gate-Source Leakage	I _{GSS}	V _{DS} =	0 V, $V_{GS} = \pm 20 V$	-	-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = - 60 V	-	-	- 1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	$V_{DS} = -60 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$	-	-	- 50	μA	
		$V_{GS} = 0 V$	$V_{DS} = -60 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	- 150		
On-State Drain Current ^a	I _{D(on)}	V _{GS} = - 10 V	$V_{DS} \le -5 V$	- 12	-	-	Α	
		V _{GS} = - 10 V	I _D = - 3.5 A	-	0.067	0.085	Αμ Α Ω	
Drain Source On State Resistence?	В	V _{GS} = - 10 V	$I_D = -3.5 \text{ A}, \text{ T}_J = 125 \ ^\circ\text{C}$	-	-	0.143	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 3.5 A, T _J = 175 °C	-	-	0.176		
		$V_{GS} = -4.5 V$	I _D = - 2.5 A	-	0.087	0.115		
Forward Transconductanceb	9 _{fs}	V _{DS} =	- 15 V, I _D = - 3.5 A	-	10	-	S	
Dynamic ^b	•	-						
Input Capacitance	C _{iss}			-	912	1140		
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	V_{DS} = - 30 V, f = 1 MHz	-	100	125	pF	
Reverse Transfer Capacitance	C _{rss}			-	60	75		
Total Gate Charge ^c	Qg			-	26.5	40		
Gate-Source Charge ^c	Q _{gs}	V _{GS} = - 10 V	V_{DS} = - 30 V, I_{D} = - 4.3 A	-	3.8	-	nC	
Gate-Drain Charge ^c	Q _{gd}			-	5.8	-		
Gate Resistance	R _g		f = 1 MHz	3.4	6.9	10.4	Ω	
Turn-On Delay Time ^c	t _{d(on)}			-	11	17		
Rise Time ^c	t _r	V _{DD} =	- 30 V, R _L = 8.8 Ω	-	13	20		
Turn-Off Delay Time ^c	t _{d(off)}	I _D ≅ - 3.4 A,	V_{GEN} = - 10 V, R_g = 1 Ω	-	36	54	ns	
Fall Time ^c	t _f	1		-	8	12		
Source-Drain Diode Ratings and Chara	acteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	- 25	Α	
Forward Voltage	Vsd	1	- 3 A, V _{GS} = 0 V		- 0.84	- 1.2	V	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

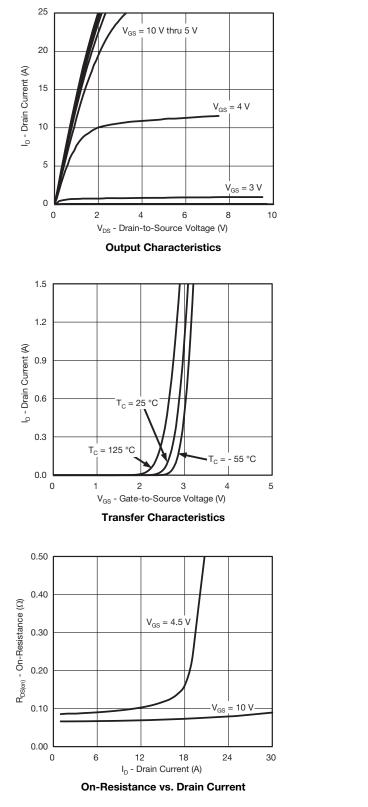
b. Guaranteed by design, not subject to production testing.

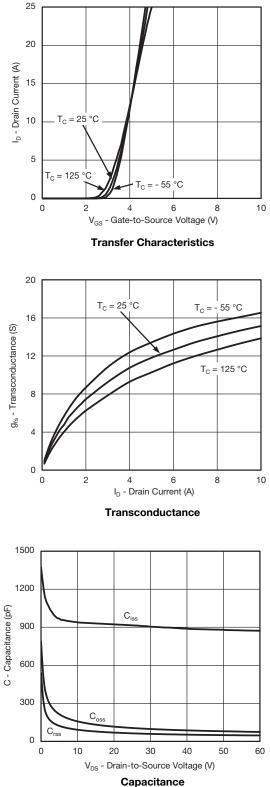
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



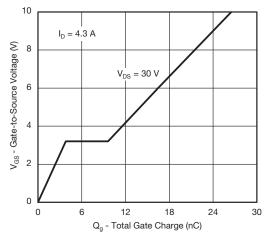


S11-1372-Rev. A, 18-Jul-11

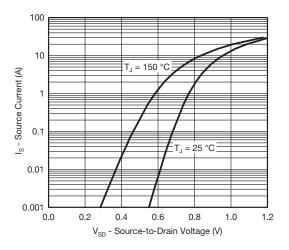
Document Number: 67581



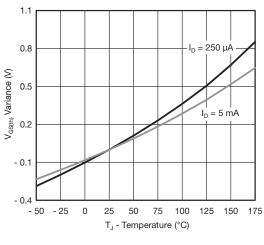
TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



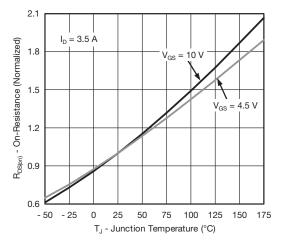
Gate Charge



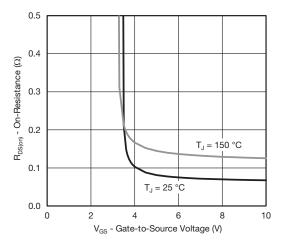
Source Drain Diode Forward Voltage



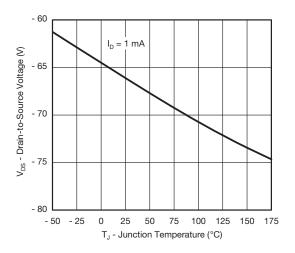
Threshold Voltage



On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature

S11-1372-Rev. A, 18-Jul-11

Document Number: 67581

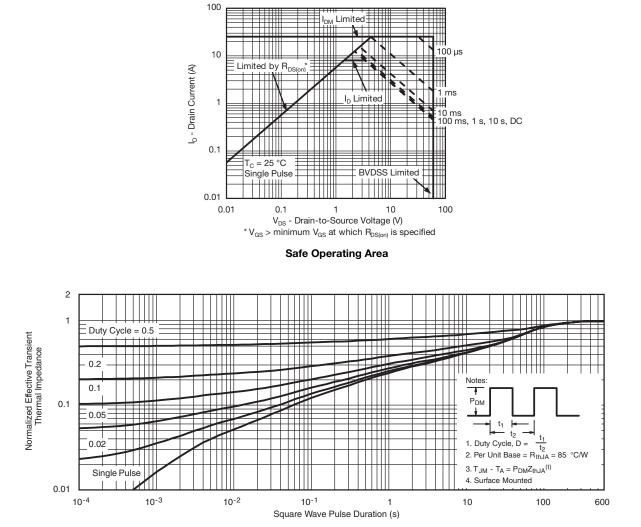
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SQJ963EP

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THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)

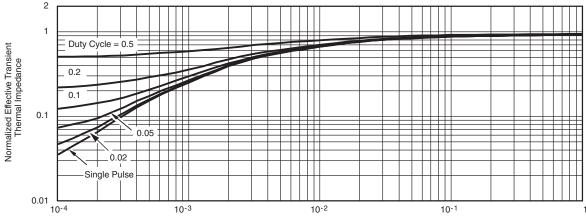


Normalized Thermal Transient Impedance, Junction-to-Ambient

S11-1372-Rev. A, 18-Jul-11



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Square Wave Pulse Duration (s)

Normalized Thermal Transient Impedance, Junction-to-Case

Note

• The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67581.

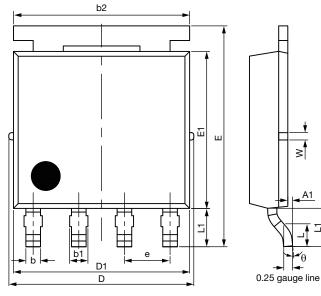


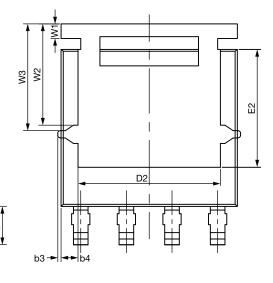


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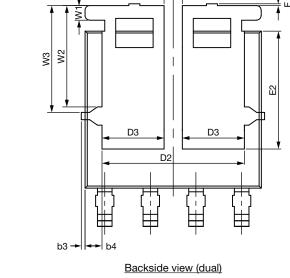
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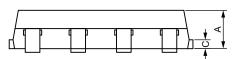




Topside view

Backside view (single)





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Package Information



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DIM	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	MIN. NOM.		
А	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094			0.004		
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC		0.050 BSC			
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	3.18	3.28	3.38	0.125	0.129	0.133	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
К		0.51			0.020		
W		0.23			0.009		
W1	0.41			0.016			
W2	2.82			0.111			
W3		2.96		0.117			
θ	0°	-	10°	0°	-	10°	

Note

• Millimeters will gover



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L DUAL



Recommended Minimum Pads Dimensions in mm (inches) Keep-out 6.75 (0.266) x 7.75 (0.305)

Revision: 07-Feb-12



Vishay

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