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Vishay Siliconix

Document Number: 67996

Automotive P-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	- 60			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.085			
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5 \text{ V}$	0.115			
I _D (A)	- 8			
Configuration	Single			

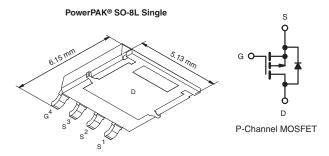
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- AEC-Q101 Qualifiedd
- 100 % R_q and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS COMPLIANT HALOGEN

FREE



ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ465EP-T1-GE3

ABSOLUTE MAXIMUM RATING	S (T _C = 25 °C, unles	s otherwise noted	(k		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V _{DS}	- 60		
Gate-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current ^a	T _C = 25 °C	1	- 8		
	T _C = 125 °C	- I _D	- 8		
Continuous Source Current (Diode Conduction) ^a		I _S	- 8	Α	
Pulsed Drain Current ^b		I _{DM}	- 25		
Single Pulse Avalanche Current		I _{AS}	- 20		
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	20	mJ	
Maximum Power Dissipation ^b	T _C = 25 °C	D	45	\A/	
	T _C = 125 °C	P_{D}	15	W	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175		
Soldering Recommendations (Peak Temperature)e, f		-	260	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	70	°C/W
Junction-to-Case (Drain)		R _{thJC}	3.3	C/VV

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.
- e. See Solder Profile (www.vishay.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static	•						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	0 V, I _D = - 250 μA	- 60	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = - 250 μA	- 1.5	- 2.0	- 2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = - 60 V	-	-	- 1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = - 60 V, T _J = 125 °C	-	-	- 50	μΑ
		V _{GS} = 0 V	V _{DS} = - 60 V, T _J = 175 °C	-	-	- 150	1
On-State Drain Current ^a	I _{D(on)}	V _{GS} = - 10 V	$V_{DS} \le -5 V$	- 12	-	-	Α
		V _{GS} = - 10 V	I _D = - 3.5 A	-	0.070	0.085	
Drain-Source On-State Resistance ^a	_	V _{GS} = - 4.5 V	I _D = - 2.5 A	-	0.090	0.115	Ω
	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 3.5 A, T _J = 125 °C	-	-	0.143	
		V _{GS} = - 10 V	I _D = - 3.5 A, T _J = 175 °C	-	-	0.176	
Forward Transconductance ^b	9 _{fs}	V _{DS} = - 15 V, I _D = - 3.5 A		-	10	=	S
Dynamic ^b							
Input Capacitance	C _{iss}			-	912	1140	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = -30 \text{ V, f} = 1 \text{ MHz}$	-	100	125	pF
Reverse Transfer Capacitance	C _{rss}			-	60	75	
Total Gate Charge ^c	Qg			-	26.5	40	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = - 10 V	$V_{DS} = -30 \text{ V}, I_{D} = -5 \text{ A}$	-	3.8	-	nC
Gate-Drain Charge ^c	Q _{gd}			-	5.8	-	
Gate Resistance	R _g		f = 1 MHz	3.5	7.18	10.8	Ω
Turn-On Delay Time ^c	t _{d(on)}			-	11	17	
Rise Time ^c	t _r		30 V, R _L = 6 Ω	-	13	20	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong -5 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$ - 36		36	54	- ns	
Fall Time ^c	t _f			-	8	12	1
Source-Drain Diode Ratings and Chara	acteristics ^b	•					
Pulsed Current ^a	I _{SM}			-	-	- 25	Α
Forward Voltage	V_{SD}	I _F = - 3 A, V _{GS} = 0 V		-	- 0.84	- 1.2	V

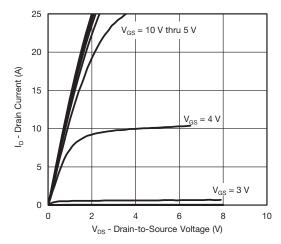
Notes

- g. Pulse test; pulse width $\leq 300~\mu s,\,duty~cycle \leq 2~\%.$
- h. Guaranteed by design, not subject to production testing.
- i. Independent of operating temperature.

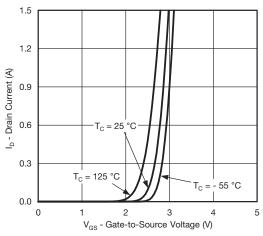
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



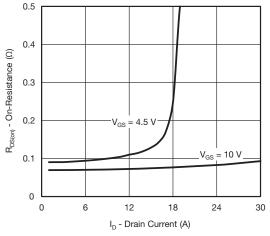
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



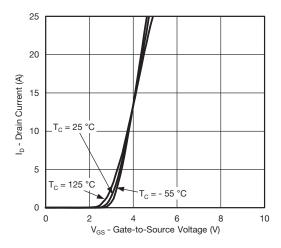
Output Characteristics



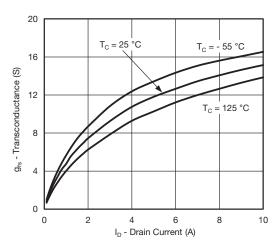
Transfer Characteristics



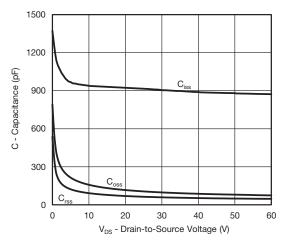
On-Resistance vs. Drain Current



Transfer Characteristics



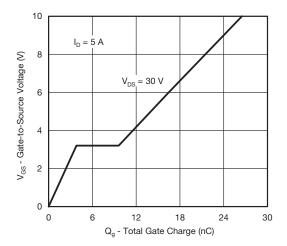
Transconductance



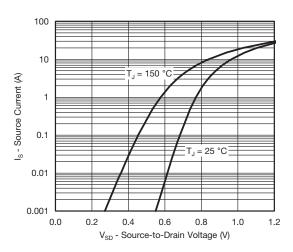
Capacitance



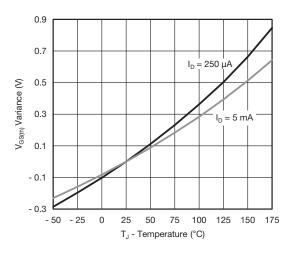
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



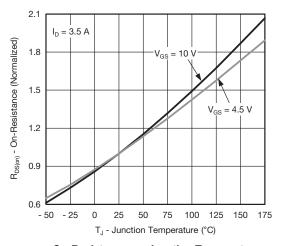
Gate Charge



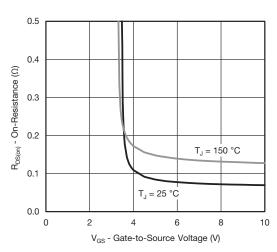
Source Drain Diode Forward Voltage



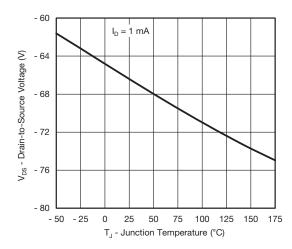
Threshold Voltage



On-Resistance vs. Junction Temperature



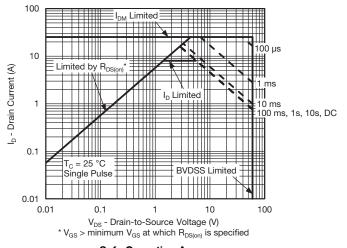
On-Resistance vs. Gate-to-Source Voltage



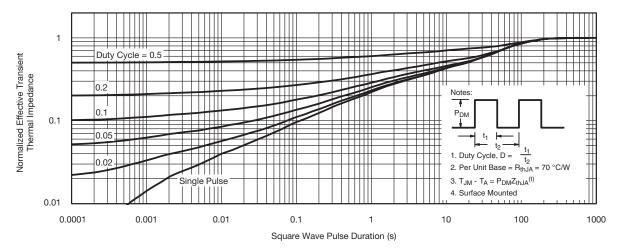
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



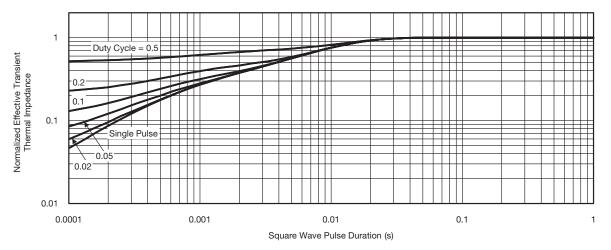
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

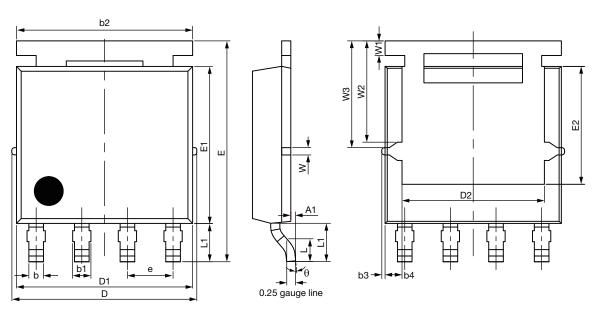
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67996.

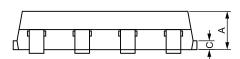


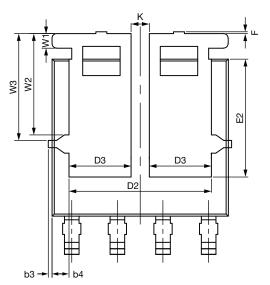
PowerPAK® SO-8L Case Outline 1



Topside view

Backside view (single)





Backside view (dual)



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DIM	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094	•		0.004		
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC	•	0.050 BSC			
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	3.18	3.28	3.38	0.125	0.129	0.133	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
K		0.51		0.020			
W		0.23		0.009			
W1	0.41		0.016				
W2	2.82		0.111				
W3		2.96			0.117		
θ	0°	-	10°	0°	-	10°	

ECN: S19-0643-Rev. E, 05-Aug-2019

DWG: 5976

Note

• Millimeters will gover



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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