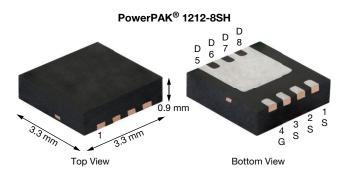


www.vishay.com

Vishay Siliconix

N-Channel 30 V (D-S) Fast Switching MOSFET



PRODUCT SUMMARY							
V _{DS} (V)	30						
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.0075						
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0082						
Q _g typ. (nC)	18						
I _D (A)	17.8						
Configuration	Single						

FEATURES

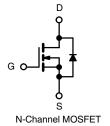
- TrenchFET® power MOSFET
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



FREE

APPLICATIONS

- Synchronous rectification
- · Load switch



ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH112DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 ^{\circ}C$, unless	s otherwise no	ited)			
PARAMETER		SYMBOL	10 S	STEADY STATE	UNIT	
Drain-source voltage	V _{DS}	30	30			
Gate-source voltage		V _{GS}	±12	±12	V	
Continuous drain surrent /T 150 °C) 3	T _C = 25 °C		17.8	11.3		
Continuous drain current (T _J = 150 °C) ^a	T _C = 70 °C	- I _D	14.2	9.1		
Pulsed drain current		I _{DM}	60	60	А	
Continuous source current (diode conduction) a		I _S	3.2	1.3		
Single avalanche current		I _{AS}	20	20		
Single avalanche energy L = 0.1 mH		E _{AS}	20	20	mJ	
Manian and a substitution of the substitution	T _C = 25 °C	Б	3.8	1.5	W	
Maximum power dissipation ^a	T _C = 70 °C	P _D	2	0.8		
Operating junction and storage temperature range		T _J , T _{stg}	-50 to +150		°C	
Soldering recommendations (peak temperature) b, c			260			

Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

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THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^a	t ≤ 10 s	В	24	33	
waximum junction-to-ambient ~	Steady state	R _{thJA}	65	81	°C/W
Maximum junction-to-foot (drain)	Steady state	R _{thJC}	1.9	2.4	

Note

a. Surface mounted on 1" x 1" FR4 board

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.6	-	1.5	V
Gate-body leakage	age I_{GSS} $V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$		-	-	±100	nA
Zara gata valtaga drain aurrent		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	5	
On-state drain current a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α
Drain course on state registeres a	Б	V _{GS} = 10 V, I _D = 17.8 A	-	0.0060	0.0075	Ω
Drain-source on-state resistance a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 17 \text{ A}$	-	0.0065	0.0082	
Forward transconductance a	9 _{fs}	V _{DS} = 15 V, I _D = 17.8 A	-	97	-	S
Diode forward voltage a	V _{SD}	$I_S = 3.2 \text{ A}, V_{GS} = 0$	-	0.7	1.2	V
Dynamic ^b						
Input capacitance	C _{iss}		-	2610	-	
Output capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	340	-	pF
Reverse transfer capacitance	C _{rss}		-	145	-	1
Total gate charge	Qg		-	18	27	
Gate-source charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 17.8 \text{ A}$	-	6.2	-	nC
Gate-drain charge	Q _{gd}		-	3.1	-	
Gate resistance	R_g	f = 1 MHz	0.5	1.2	1.8	Ω
Turn-on delay time	t _{d(on)}		-	10	15	
Rise time	t _r	V_{DD} = 15 V, R_L = 15 Ω	-	10	15	ns
Turn-off delay time	t _{d(off)}	$I_D\cong 1$ A, $V_{GEN}=10$ V, $R_g=6~\Omega$	-	65	100	
Fall time	t _f		-	10	15	
Body diode reverse recovery time	t _{rr}	1 2 2 A di/d+ 100 A/va	-	30	60	
Body diode reverse recovery charge	Q _{rr}	$I_F = 3.2 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	-	18	-	nC

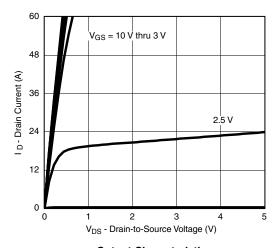
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

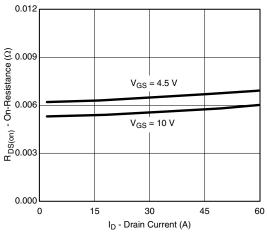
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



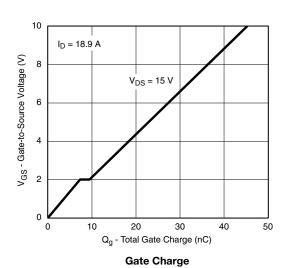
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

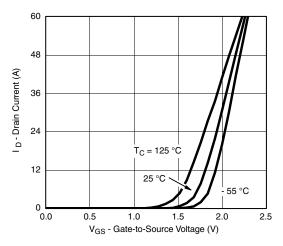


Output Characteristics

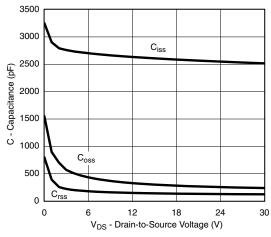


On-Resistance vs. Drain Current

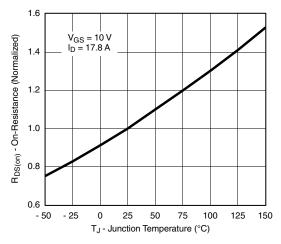




Transfer Characteristics



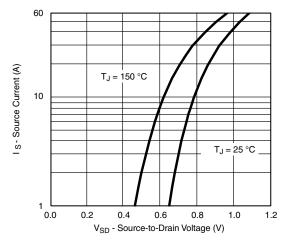
Capacitance



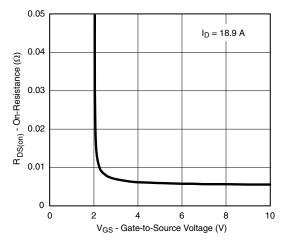
On-Resistance vs. Junction Temperature



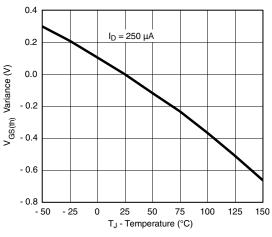
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



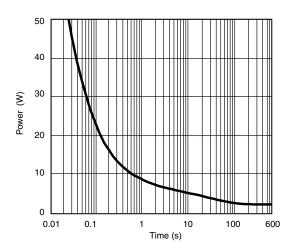
Source-Drain Diode Forward Voltage



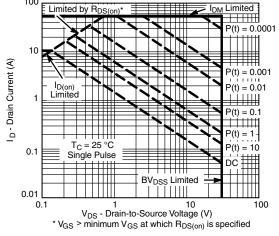
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



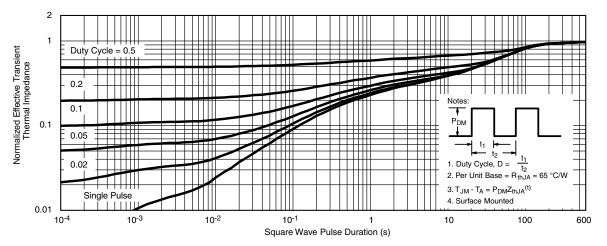
Single Pulse Power, Junction-to-Ambient



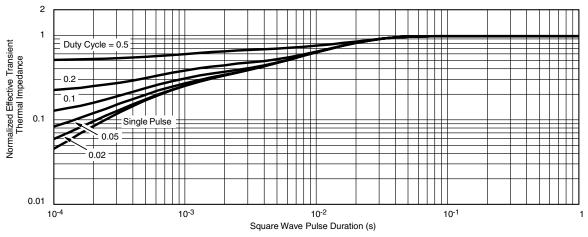
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

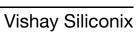


Normalized Thermal Transient Impedance, Junction-to-Ambient



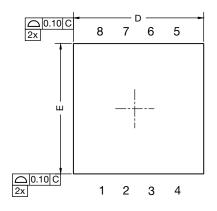
Normalized Thermal Transient Impedance, Junction-to-Case

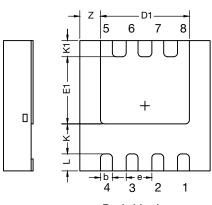
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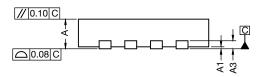


PowerPAK® 1212-SWLH





Backside view



DIM	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN. NOM.	NOM.	MAX.	
Α	0.82	0.90	0.98	0.032	0.035	0.038	
A1	0	-	0.05	0	-	0.002	
A3	0.20 ref.			0.008 ref.			
b	0.30 BSC			0.012 BSC			
D	3.30 BSC			0.130 BSC			
D1	2.15	2.25	2.35	0.084	0.088	0.092	
E	3.30 BSC			0.130 BSC			
E1	1.60	1.70	1.80	0.063	0.067	0.071	
е	0.65 BSC			0.026 BSC			
K	0.76 typ.			0.030 typ.			
K1	0.41 typ.			0.016 typ.			
L	0.43 BSC			0.017 BSC			
Z	0.525 typ.			25 typ. 0.021 typ.			

DWG: 6062



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