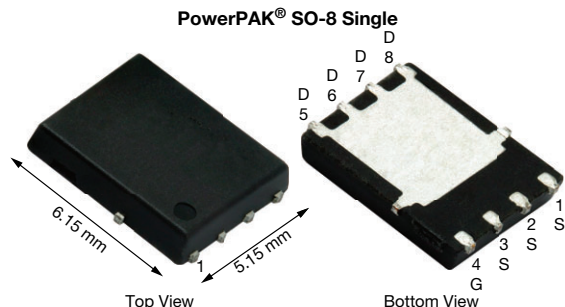


N-Channel 30 V (D-S) MOSFET with Schottky Diode



FEATURES

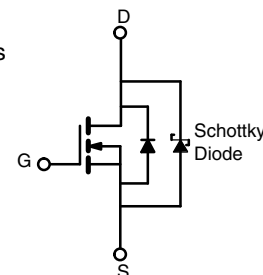
- TrenchFET® Gen IV power MOSFET
- SkyFET® with monolithic Schottky diode
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Personal computers and servers
- Synchronous buck
- Synchronous rectification
- DC/DC conversion



PRODUCT SUMMARY

V _{DS} (V)	30
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.0027
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.0040
Q _g typ. (nC)	17.5
I _D (A)	60 ^{a, g}
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiRC06DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	30	V
Gate-source voltage	V _{GS}	+20, -16	
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	60 ^g
		T _C = 70 °C	60 ^g
		T _A = 25 °C	32 ^{b, c}
		T _A = 70 °C	25.6 ^{b, c}
Pulsed drain current (t = 300 μs)	I _{DM}	100	
Continuous source-drain diode current	I _S	T _C = 25 °C	60 ^g
		T _A = 25 °C	7.1 ^{b, c}
Single pulse avalanche current	I _{AS}	15	
Single pulse avalanche energy	E _{AS}	11.25	mJ
Maximum power dissipation	P _D	T _C = 25 °C	50
		T _C = 70 °C	32
		T _A = 25 °C	5 ^{b, c}
		T _A = 70 °C	3.2 ^{b, c}
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	R _{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	R _{thJC}	1.9	2.5	

Notes

- Based on T_C = 25 °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W
- Package limit



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V
Drain-source breakdown voltage (transient) ^c	V _{DS} t	V _{GS} = 0 V, I _{D(aval)} = 15 A, t _{transcient} ≤ 50 ns	36	-	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.1	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	0.02	0.10	mA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	0.13	1	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	-	0.0022	0.0027	Ω
		V _{GS} = 4.5 V, I _D = 10 A	-	0.0032	0.0040	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 15 A	-	120	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	2455	-	pF
Output capacitance	C _{oss}		-	350	-	
Reverse transfer capacitance	C _{rss}		-	60	-	
C _{rss} /C _{iss} ratio			-	0.025	0.050	
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 15 A	-	38.5	58	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 15 A	-	17.5	27	
Gate-source charge	Q _{gs}		-	6.3	-	
Gate-drain charge	Q _{gd}		-	2.8	-	
Output charge	Q _{oss}	V _{DS} = 15 V, V _{GS} = 0 V	-	29	-	
Gate resistance	R _g	f = 1 MHz	0.4	1.15	2	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	12	24	ns
Rise time	t _r		-	14	28	
Turn-off delay time	t _{d(off)}		-	23	46	
Fall time	t _f		-	8	16	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	29	58	
Rise time	t _r		-	50	100	
Turn-off delay time	t _{d(off)}		-	20	40	
Fall time	t _f		-	9	18	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	60	A
Pulse diode forward current (t = 100 μs)	I _{SM}		-	-	100	
Body diode voltage	V _{SD}	I _S = 5 A	-	0.47	0.7	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	31	62	ns
Body diode reverse recovery charge	Q _{rr}		-	19	38	nC
Reverse recovery fall time	t _a		-	16	-	ns
Reverse recovery rise time	t _b		-	15	-	

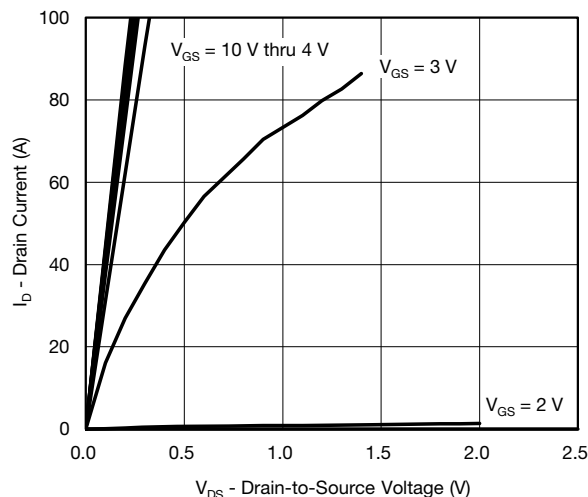
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. $T_{CASE} = 25\text{ }^{\circ}\text{C}$; Expected voltage stress during 100 % UIS test. Production data log is not available

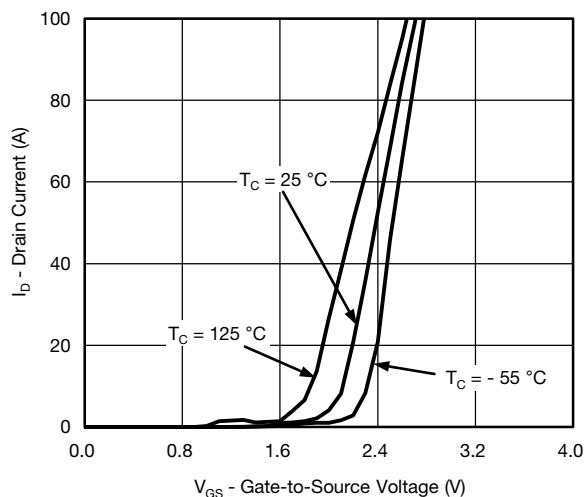
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



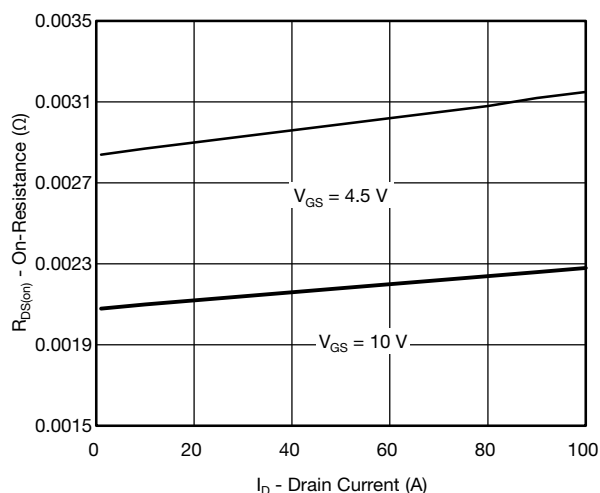
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



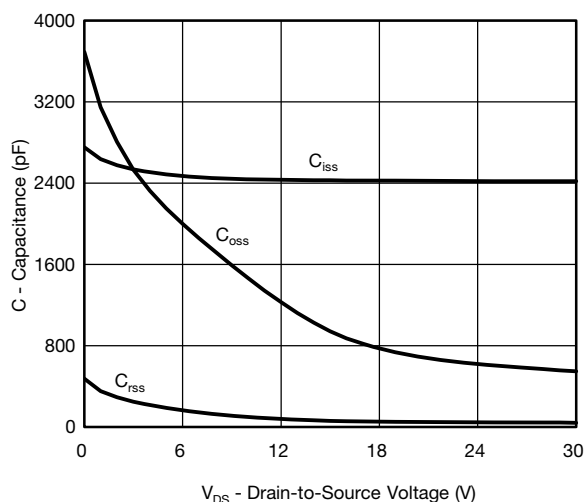
Output Characteristics



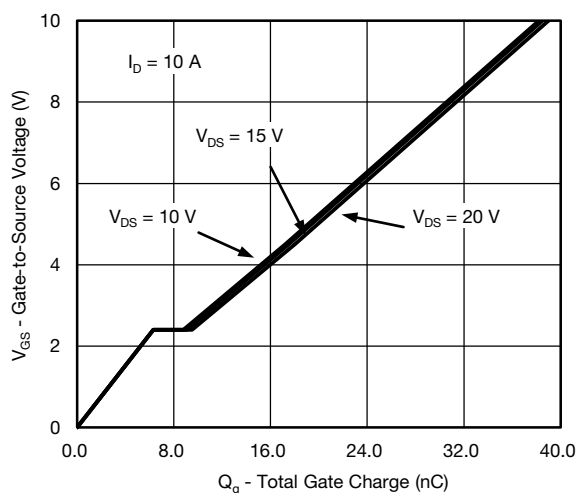
Transfer Characteristics



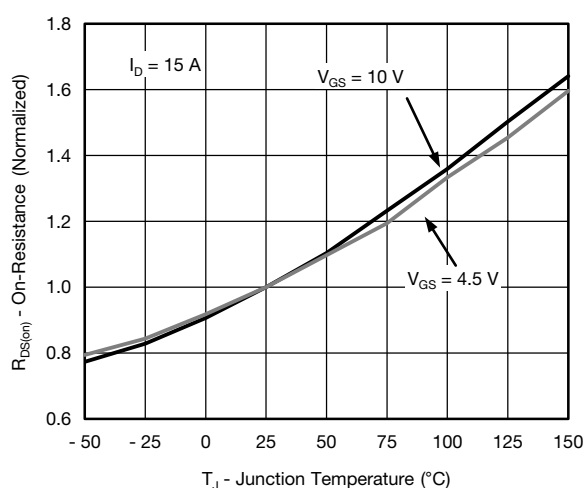
On-Resistance vs. Drain Current



Capacitance



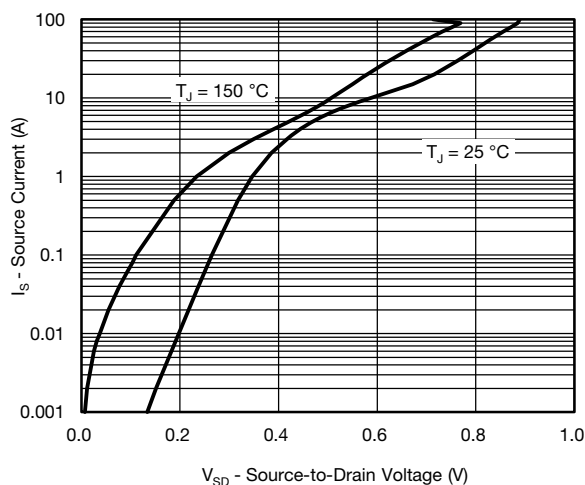
Gate Charge



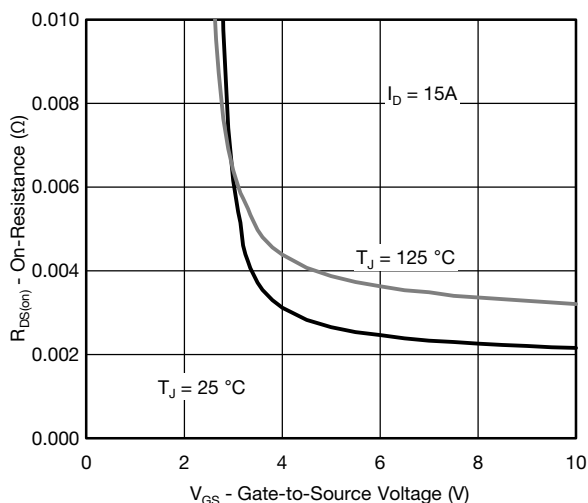
On-Resistance vs. Junction Temperature



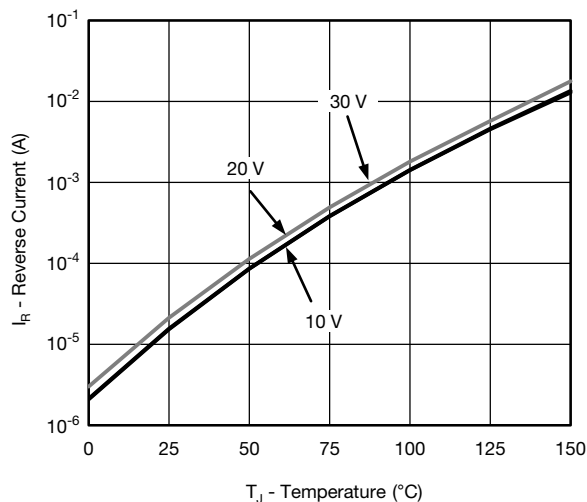
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



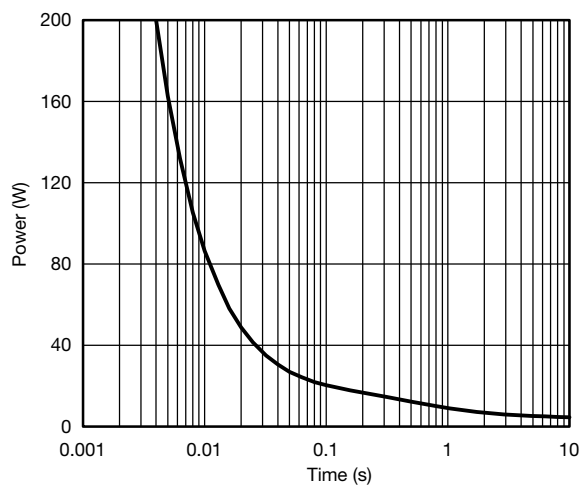
Source-Drain Diode Forward Voltage



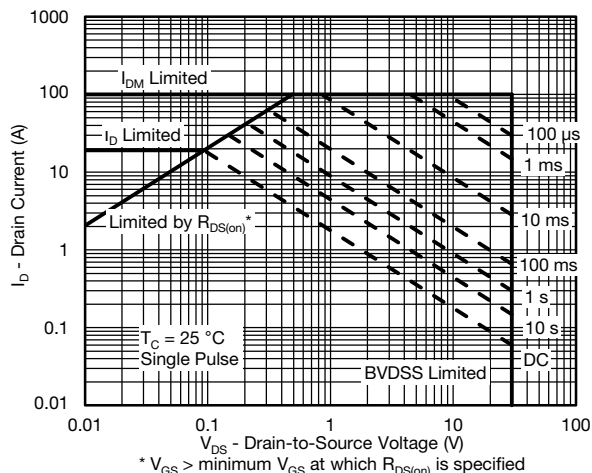
On-Resistance vs. Gate-to-Source Voltage



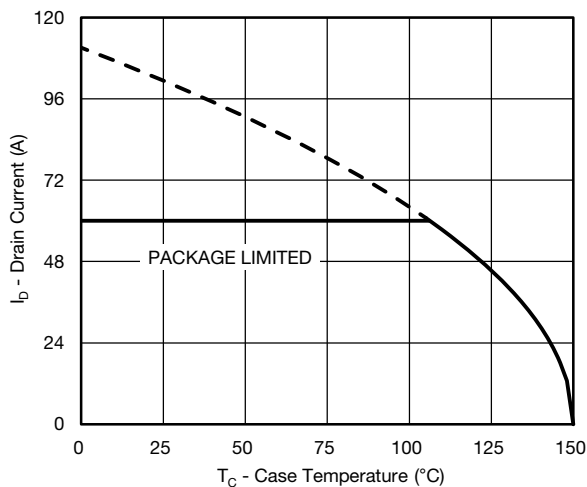
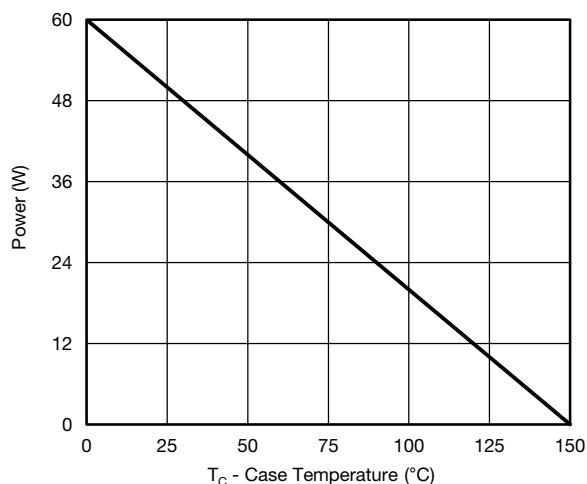
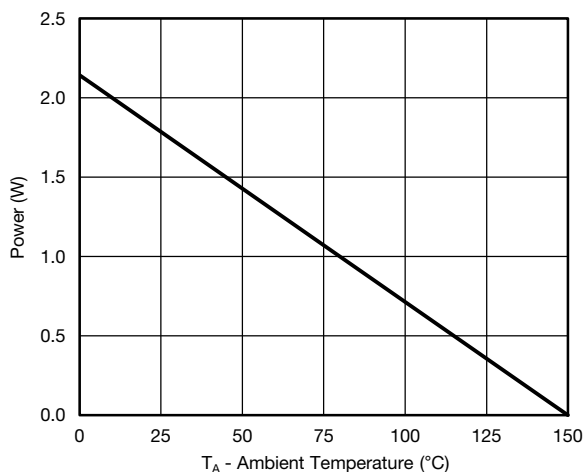
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



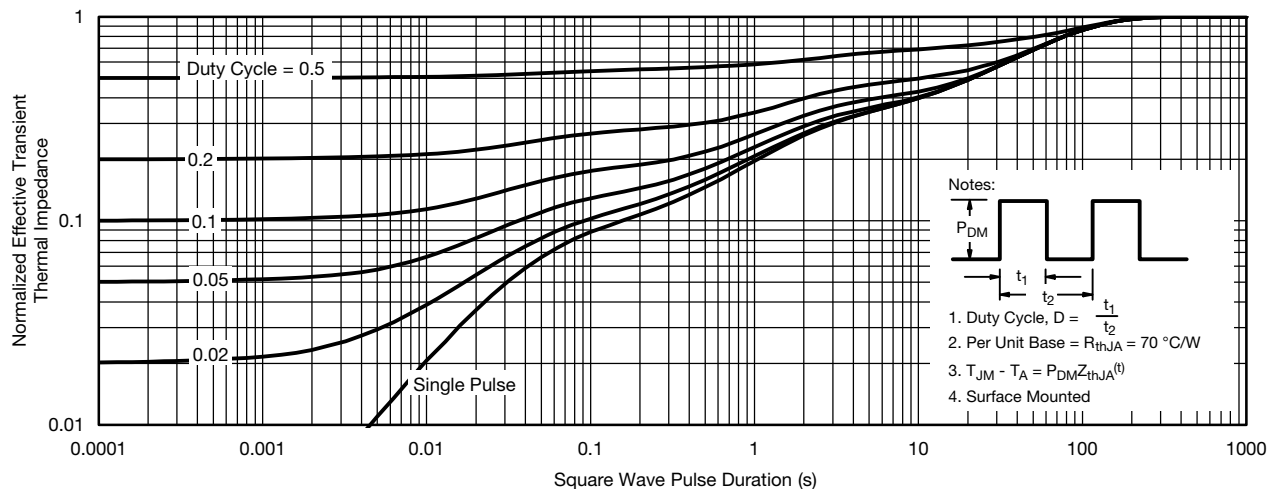
Safe Operating Area

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

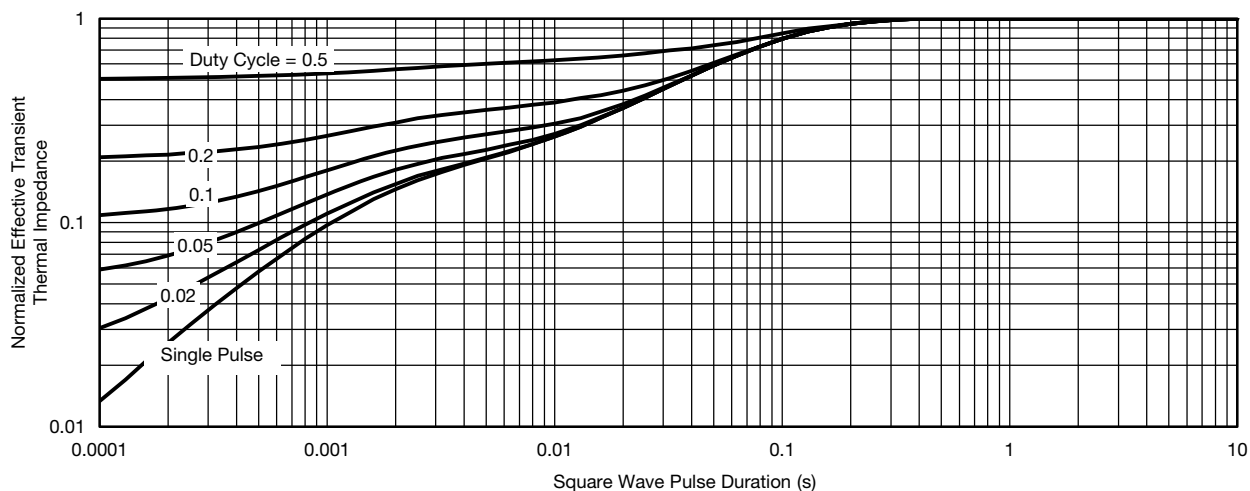
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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