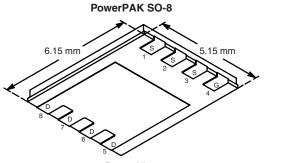


**Vishay Siliconix** 

## N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)		
30 -	0.0047 at V <sub>GS</sub> = 10 V	40 <sup>g</sup>	16.8 nC		
	0.0061 at $V_{GS}$ = 4.5 V	40 <sup>g</sup>	10.0110		



Bottom View

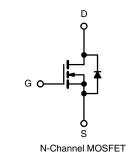
Ordering Information: SiR460DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

#### FEATURES

- Halogen-free According to IEC 61249-2-21
- TrenchFET<sup>®</sup> Gen III Power MOSFET
- 100 % R<sub>q</sub> Tested
- 100 % Avalanche Tested

#### **APPLICATIONS**

- Notebook Vcore
- DC/DC



ABSOLUTE MAXIMUM RATINGS T Parameter	Symbol	Limit	Unit		
				Unit	
Drain-Source Voltage		V <sub>DS</sub>	30	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	•	
	T <sub>C</sub> = 25 °C		40 <sup>g</sup>		
Continuous Drain Current ( $T_1 = 150 \ ^{\circ}C$ )	T <sub>C</sub> = 70 °C	I <sub>D</sub>	40 <sup>g</sup>		
Continuous Drain Current (1j = 130 C)	T <sub>A</sub> = 25 °C	'D	24.3 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		19.4 <sup>b, c</sup>	A	
Pulsed Drain Current	•	I <sub>DM</sub>	70	A	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	L.	40 <sup>g</sup>		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	4.5 <sup>b, c</sup>		
Single Pulse Avalanche Current		I <sub>AS</sub>	30		
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	45	mJ	
	T <sub>C</sub> = 25 °C		48		
Maximum Davies Disaination	T <sub>C</sub> = 70 °C		31	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5.0 <sup>b, c</sup>	vv	
	T <sub>A</sub> = 70 °C		3.2 <sup>b, c</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260	·U	

#### THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	20	25	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	2.1	2.6	0/11

Notes:

- a. Based on T<sub>C</sub> = 25 °C.
- b. Surface Mounted on 1" x 1" FR4 board.

- d. See Solder Profile (<u>www.vishay.com/ppg?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

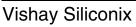
f. Maximum under Steady State conditions is 65 °C/W.

g. Package Limited.



FREE

c. t = 10 s.





Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static					1	1
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	30			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L 050 A		29		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	l <sub>D</sub> = 250 μA		- 5.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1.0		2.4	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 \text{ °C}$			10	μA
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			А
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.0038	0.0047	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A	_			Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		60		S
Dynamic <sup>b</sup>					I	1
Input Capacitance	C <sub>iss</sub>			2071		
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		406		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			168		
	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$	36 54		54	
Total Gate Charge				16.8	25.5	nC
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$		5.1		
Gate-Drain Charge	Q <sub>gd</sub>			5.2		
Gate Resistance	Rg	f = 1 MHz	0.2	0.85	1.7	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			25	45	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		16	30	1
Turn-Off Delay Time	t <sub>d(off)</sub>	${ m I}_{ m D}\cong$ 10 A, ${ m V}_{ m GEN}$ = 10 V, ${ m R}_{ m g}$ = 1 $\Omega$		28	50	1
Fall Time	t <sub>f</sub>			12	24	
Turn-On Delay Time	t <sub>d(on)</sub>			10	20	- ns - -
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		9	18	
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong$ 10 A, $\text{V}_\text{GEN}$ = 4.5 V, $\text{R}_\text{g}$ = 1 $\Omega$		25	45	
Fall Time	t <sub>f</sub>			9	18	
Drain-Source Body Diode Characteris	tics	· · · · · ·				
Continuous Source-Drain Diode Current	۱ <sub>S</sub>	$T_{C} = 25 \ ^{\circ}C$			40	А
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				70	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 3 A		0.73	1.1	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>			19	38	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 10 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C		10	20	nC
Reverse Recovery Fall Time	t <sub>a</sub>	$r_F = 10 \text{ A}, \text{ u/u} = 100 \text{ A/} \mu \text{s}, 1 \text{ J} = 25 \text{ C}$		10		ns
Reverse Recovery Rise Time	t <sub>b</sub>			9		

Notes:

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

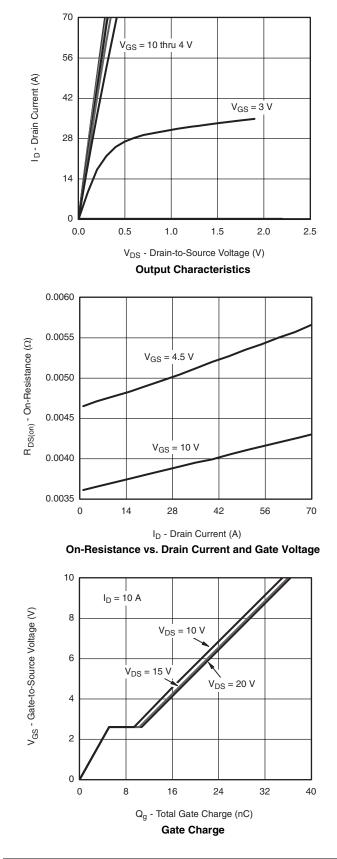
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

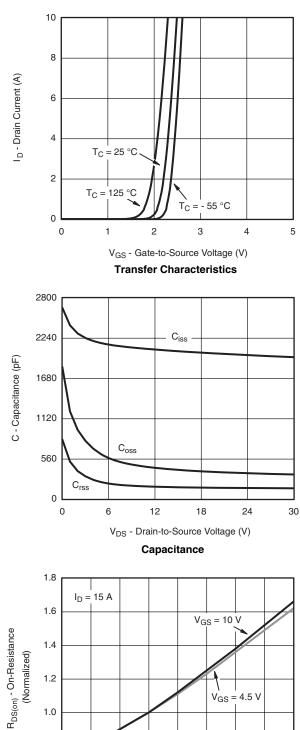




Vishay Siliconix

#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





1.0

0.8

0.6

- 50

- 25

0

25

50

T<sub>J</sub> - Junction Temperature (°C)

**On-Resistance vs. Junction Temperature** 

75

Document Number: 69095 S09-0140-Rev. A, 02-Feb-09 125 150

V<sub>GS</sub> = 4.5 V

100

## Vishay Siliconix



 $T_J = 125 \ ^\circ C$ 

 $T_J = 25 \degree C$ 

8 9 10

7

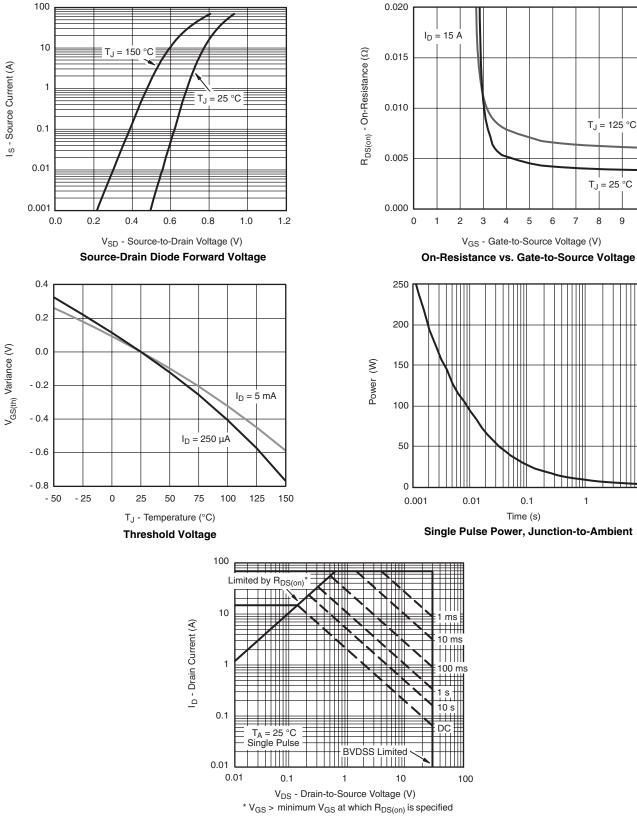
1

10

0.1

5 6

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



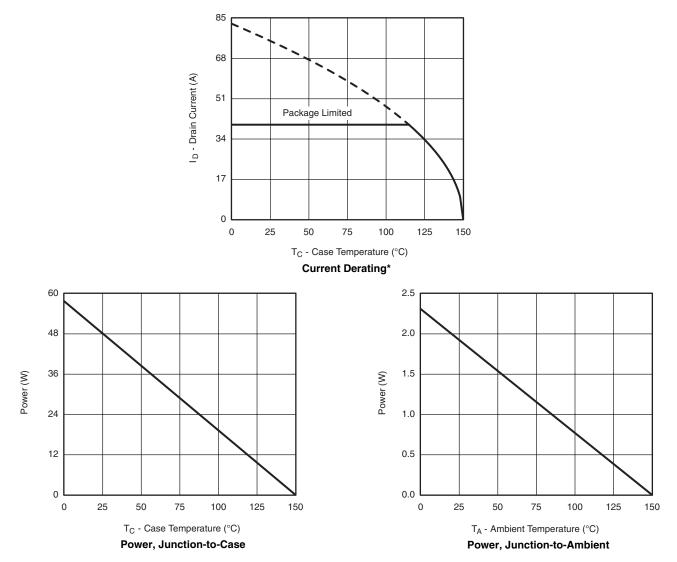
Safe Operating Area, Junction-to-Ambient

**New Product** 

VISHAY.

## SiR460DP Vishay Siliconix

#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

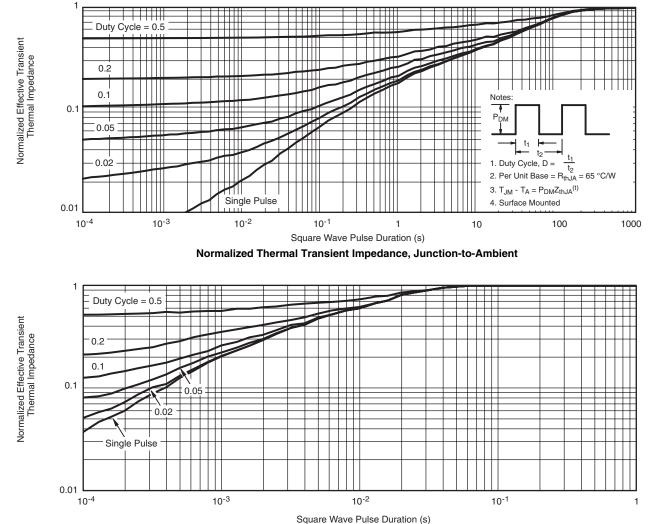


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

# VISHAY.

## Vishay Siliconix

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?69095">www.vishay.com/ppg?69095</a>.



**Vishay Siliconix** 

# PowerPAK<sup>®</sup> SO-8, (Single/Dual)









Backside View of Dual Pad

Notes

1. Inch will govern.

2 Dimensions exclusive of mold gate burrs.

3. Dimensions exclusive of mold flash and cutting burrs.

	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.56	3.76	3.91	0.140	0.148	0.154	
D3	1.32	1.50	1.68	0.052	0.059	0.066	
D4	0.57 typ.				0.0225 typ.		
D5		3.98 typ.		0.157 typ.			
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	5.79	5.89	5.99	0.228	0.232	0.236	
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144	
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151	
E3	3.68	3.78	3.91	0.145	0.149	0.154	
E4 (for AL product)		0.58 typ.		0.023 typ.			
E4 (for other product)	0.75 typ.			0.030 typ.			
е	1.27 BSC			0.050 BSC			
K (for AL product)	1.45 typ.			0.057 typ.			
K (for other product)	1.27 typ.			0.050 typ.			
K1	0.56	-	-	0.022	-	-	
Н	0.51	0.61	0.71	0.020	0.024	0.028	
L	0.51	0.61	0.71	0.020	0.024	0.028	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
М	0.125 typ.			0.005 typ.			

Revison: 20-May-13

Document Number: 71655



# Application Note 826

Vishay Siliconix

## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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Vishay

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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