1-MHz Boost Converter with OVP for White LED Applications

DESCRIPTION

The SiP12506 is a 1 MHz current-mode boost converter with a feedback voltage of 0.208 V which offers small size and high power conversion efficiency. Its input voltage range is from 2.6 V to 9 V, and output voltage can go up to 20 V. The internal frequency compensation minimizes number of external components. The integrated 28 V power switch can carry up to 1.6 A easily providing for 200 mA load current from a 3.6 V input supply. These features make the SiP12506 the ideal. The internal soft-start circuit controls the rate of rise of the output voltage during start-up to prevent overshoot. The logic-level shutdown pin can be used to reduce quiescent current to < 1 µA and, effectively, extend battery life. Thermal shutdown at 160 °C is also included. The low FB voltage of 0.208 V improves the overall circuit efficiency. These features and more, make the SiP12506 an ideal power solution to white LED, OLED, LCD, and CCD applications operating from a single or dual cell lithium-ion battery.

SiP12506 is available in 6-pin MLP33 package and is specified to operate over the industrial temperature range of - 40 °C to 85 °C.

FEATURES

- Output Voltage Range up to 20 V
- FB Voltage of 0.208 V
- Cycle-By-Cycle Current Limiting with Internal Frequency Compensation
- 2.6 V to 9 V Input Voltage Range
- 1 MHz Switching Frequency
- > 90 % efficiency
- Low $R_{DS(on)}$: 0.4 Ω (at 3.3 V)
- 1.6 A Switch Current Limit
- < 1 µA Low Shutdown Current
- Internal Soft-Start Control
- Thermal Shutdown Protection (160 °C)
- 6 pin MLP33 Package

Pb-free

RoHS COMPLIANT

APPLICATIONS

- CCD Bias Supplies
- TFT-LCD Displays
- OLED Driver
- White LED Backlight
- Digital Cameras
- Portable Phones and Game Devices
- PDAs and Palm-Top Computers

TYPICAL APPLICATION CIRCUIT

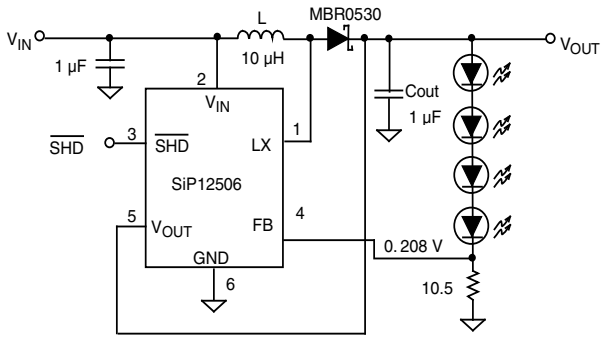


Figure 1. SiP12506 Typical Application Circuit

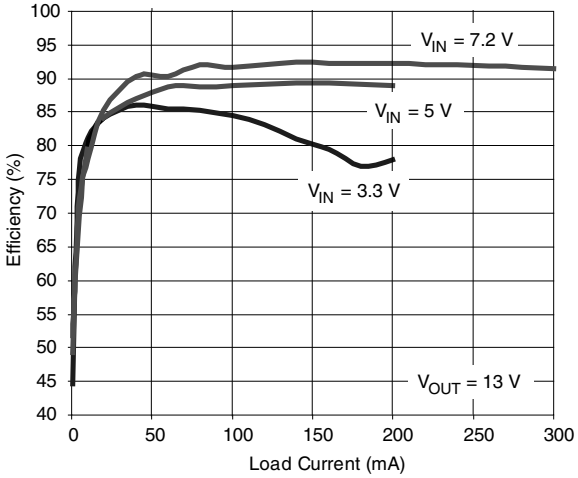


Figure 2. Efficiency Curve

ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit
Voltages Referenced Input Voltage V_{IN} to GND	- 0.3 to 12	V
V_{OUT}, LX Voltages	- 0.3 to 28	
$\overline{SHD}$ Voltage	- 0.3 to 12	
FB Voltage	- 0.3 to 12	
ESD (Human Body Model)[a]	2	kV
Operating Junction Temperature	125	°C
Storage Temperature	- 55 to + 150	°C
Power Dissipation (T_A = 70 °C)[b]	1100	mW
Thermal Resistance[c]	50	°C/W

Notes:
a. The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
b. Derate 20 mW/°C above 70 °C.
c. Devise mounted with all leads soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Voltages Referenced Input Voltage Range (V_{IN}) to GND	2.6 to 9	V
$\overline{SHD}$	0 to V_{IN}	
V_{OUT}	V_{IN} to 18	
LX	0 to 18.5	
FB	0 to 2	
Operating Temperature Range	- 40 to 85	°C

SPECIFICATIONS

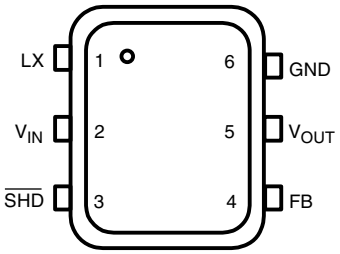
Parameter	Symbol	Test Conditions Unless Specified V_{IN} = 5.0 V, $V_{\overline{SHD}}$ = 2 V, T_A = 25 °C	Temp	Min[a]	Typ[b]	Max[a]	Unit
Input Voltage	V_{IN}		FULL	2.6		9	V
Switch Current Limit	I_{LIMIT}		FULL	1.1	1.6	2.2	A
Switch on Resistance	$R_{DS(on)}$	I_{SW} = 200 mA	FULL		0.4	0.65	Ω
$\overline{SHD}$ Input High Level	$V_{\overline{SHD}H}$	V_{IN} = 2.6 to 9 V	FULL	1.5			V
$\overline{SHD}$ Input Low Level	$V_{\overline{SHD}L}$		FULL			0.5	
$\overline{SHD}$ Input Leakage Current	$I_{\overline{SHD}}$					1	µA
Feedback Voltage	V_{FB}		25 °C	0.198	0.208	0.218	V
			FULL	0.188		0.224	
Feedback Bias Current	I_{FB}				60		nA
Feedback Voltage Line Regulation	$\Delta V_{FB}/(V_{FB} \times \Delta V_{IN})$	V_{IN} = 2.6 V to 9 V	FULL		0.2		%/V
Feedback Voltage Load Regulation	$\Delta V_{FB}/(V_{FB} \times \Delta V_{OUT})$	V_{OUT} = 10 V			0.15		%/A
Quiescent Current	$I_{V_{IN}}$	V_{FB} = 0 V (Switching)	FULL		2.1	3.0	mA
		V_{FB} = 1.5 V (Not Switching)	FULL		0.35	0.5	
		$V_{\overline{SHD}}$ = 0 V	FULL			1	µA
Switching Frequency	F_{SW}		FULL	0.75	1	1.25	MHz
Maximum Duty Cycle	D_{MAX}		FULL	86	91		%
Switch Leakage	I_{LEAK}	Not Switching, V_{LX} = 5 V	25 °C			1	µA
			FULL			5	

SPECIFICATIONS							
Thermal Shutdown	$T_{\overline{SHD}}$				160		°C
Thermal Shutdown Hysteresis	T_{HYST}				25		
Under Voltage Lockout	T_{UVLO}	V_{IN} Rising	FULL	2.25	2.4	2.55	V
UVLO Hysteresis	$T_{UVLOHYST}$				0.1		
OVLO	T_{OVLO}	V_{OUT} Rising	FULL	18	20	22.5	
OVLO Hysteresis	$T_{OVLOHSYST}$				1		
OUT Bias Current	I_{VOUT}	V_{OUT} = 5 V			3.2		µA

Notes:
a. Limits are guaranteed by testing.
b. Typical values are derived from the mean value of a large quantity of samples tested during characterization and represent the most likely expected value of the parameter at room temperature.

PIN CONFIGURATION

6 Lead MLP33 Package



Top View

Figure 3.

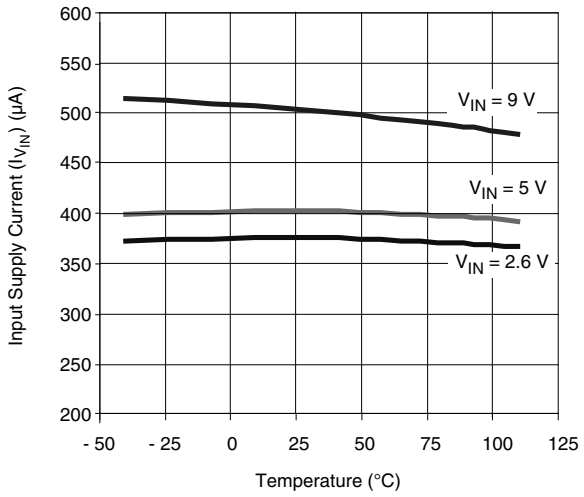
ORDERING INFORMATION			
Part Number	**Marking**	**Temperature Range**	**Package**
SiP12506DMP-TI-E3	2506	- 40 °C to 85 °C	MLP33-6

PIN DESCRIPTION		
Pin Number	**Name**	**Function**
1	LX	Drain Pin of the Internal Switch.
2	V_{IN}	Input Power Pin.
3	$\overline{SHD}$	Logic Controlled Shutdown Input. $\overline{SHD}$ = high: Normal operation. $\overline{SHD}$ = low: Shutdown.
4	FB	Voltage Feedback Pin.
5	V_{OUT}	Output Voltage Pin.
6	GND	Signal and Power Ground.

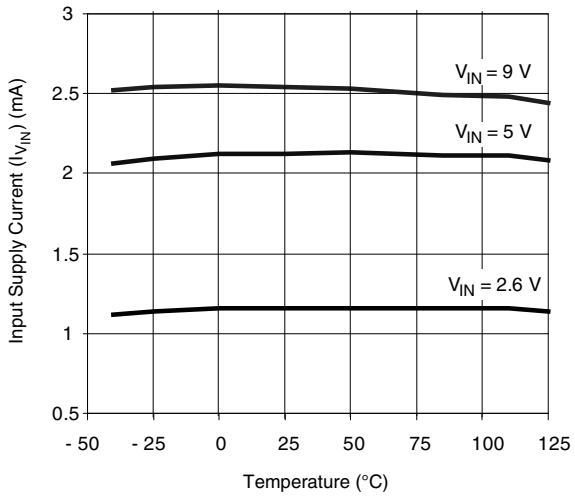
DETAILED PIN DESCRIPTION

LX: Drain of the Internal 26 V NMOS. Connect inductor/diode to LX. Minimize trace area at this pin to keep electromagnetic interference down to a minimum.
V_{IN}: the analog and power input of the controller IC. A bypass capacitor is required on this pin.
$\overline{SHD}$: the $\overline{SHD}$ pin provides shutdown control. To allow for normal operation, connect $\overline{SHD}$ to V_{IN}. Connect $\overline{SHD}$ to GND to disable the device.
FB: The inverting input of the voltage error amplifier. This is internally compared against a voltage of 0.208 V appearing on the voltage error amplifier's non-inverting input. External resistors are connected to this pin to set the regulated output voltage.
V_{OUT}: Output voltage sense for over voltage protection and slop compensation.
GND: This pin acts as both the analog ground and the power ground for this part.

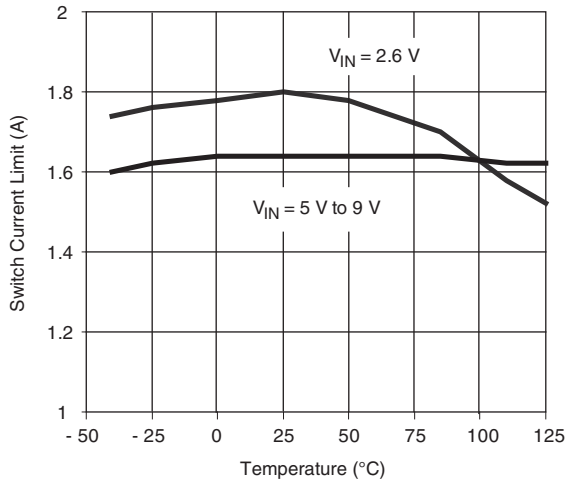
TYPICAL CHARACTERISTICS



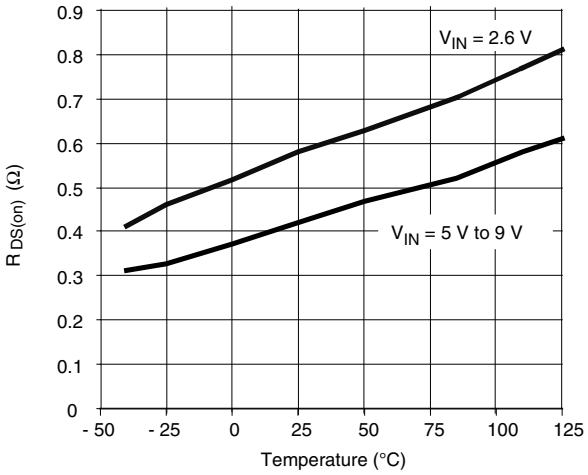
$I_{V_{IN}}$ (Active) vs. Temperature



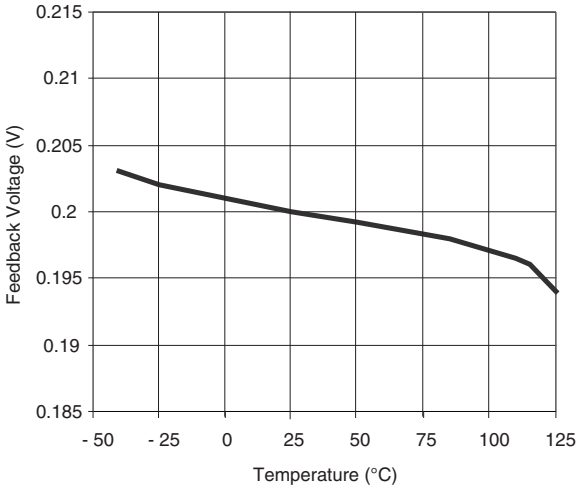
$I_{V_{IN}}$ (Active - Switching) vs. Temperature



Switch Current Limit vs. Temperature

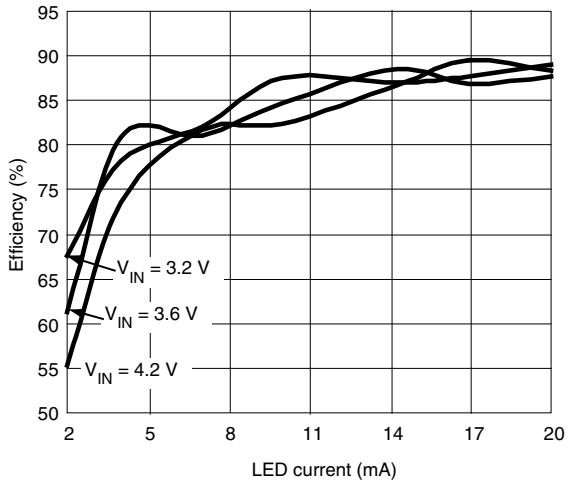


Switching On Resistance vs. Temperature

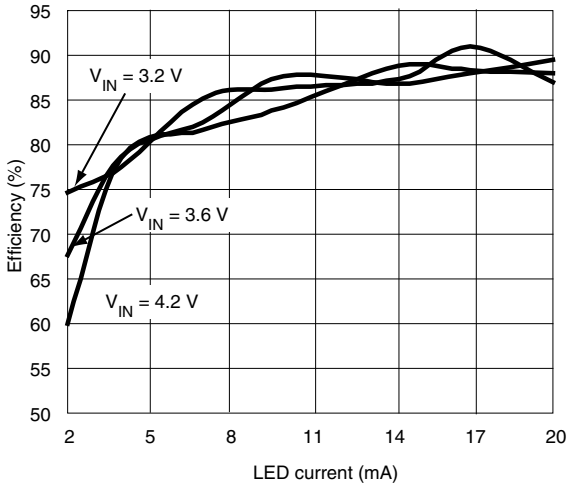


Feedback Voltage vs. Temperature

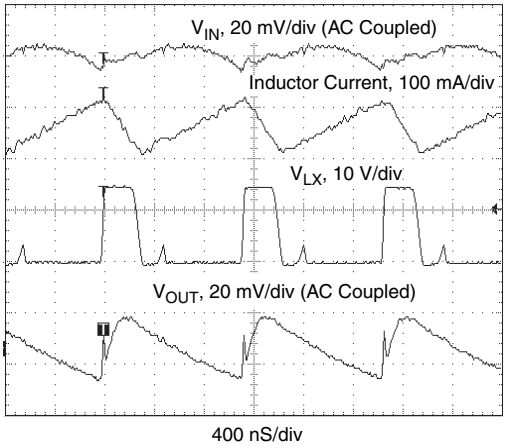
TYPICAL WAVEFORMS



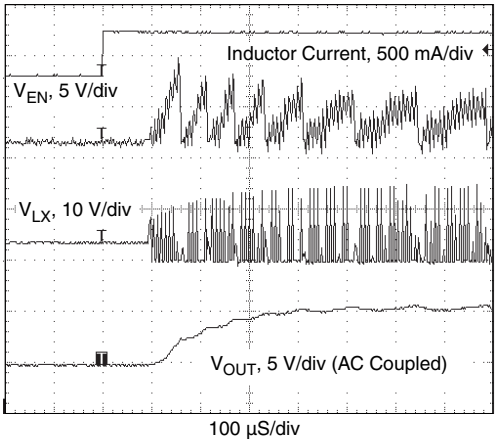
Efficiency vs. LED Current - Driving 3 Series LEDs



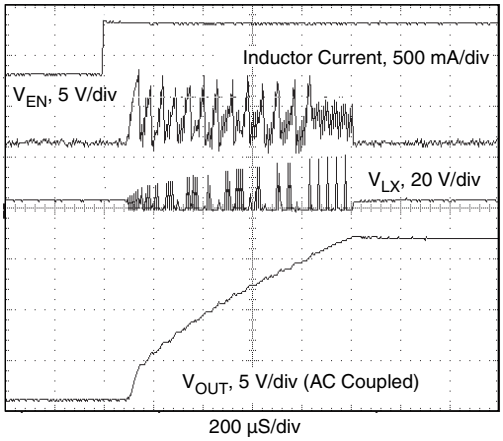
Efficiency vs. LED Current - Driving 4 Series LEDs



Steady State Condition
V_{IN} = 3.6 V, 4 series LEDs, I_{LOAD} = 20 mA



Start-Up
V_{IN} = 3.6 V, 4 series LEDs, I_{LOAD} = 20 mA



Start-Up under Open-Load Condition
V_{IN} = 3.6 V, open load

FUNCTIONAL BLOCK DIAGRAM

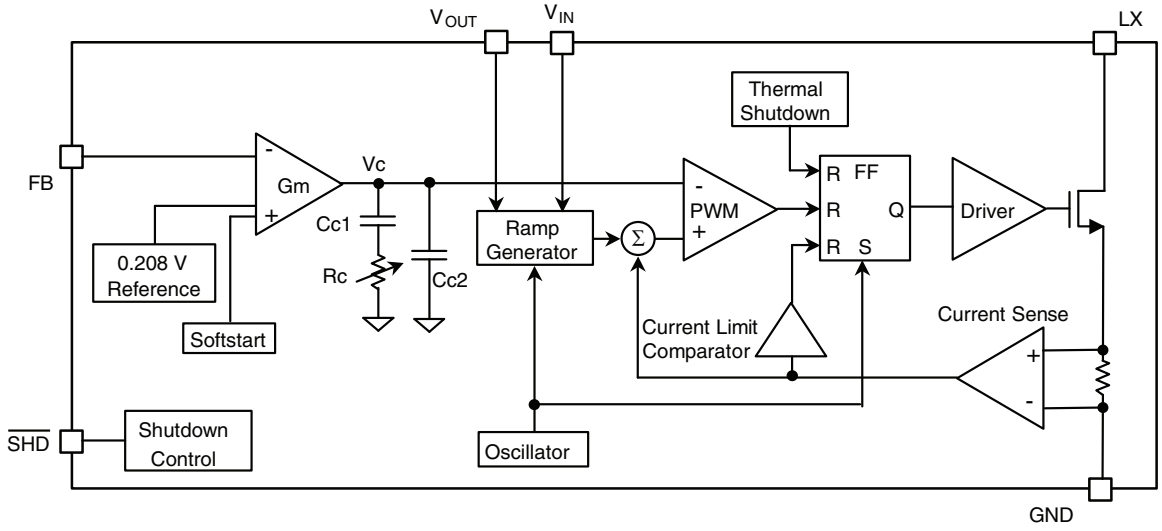


Figure 4. Internal Block Diagram

DETAILED OPERATION DESCRIPTION:

The SiP12506 is a current mode, internally compensated, step-up switching converter that operates at a fixed frequency of 1 MHz. The current mode topology allows for fast transient response over a wide input range and provides a real-time, cycle-by-cycle current limiting function. The operation of the converter can be described through the interaction of two separate internal loops: the current sense loop and voltage sense loop.

Within the current sense loop, the switch FET current is monitored by sensing the voltage across an internal current sense resistor which is fed to the inputs of both the current limit amplifier and the pulse width modulation (PWM) comparator.

At the beginning of each switch cycle, the oscillator sets the S-R latch thereby turning on the FET. As current through the switch increases, so does the voltage drop across the sense resistor. This voltage is summed with the ramp coming from the ramp generator and applied to the input of the PWM comparator. When this ramping voltage exceeds Vc (the output of the Gm amplifier), the latch changes state and turns off the FET. The slope of the ramp generator is proportional to voltages on the V_{IN} and V_{OUT} pins, therefore, any sudden changes in input or output voltage can be corrected and accommodated for on a cycle-by-cycle basis. If the FET current surpasses the current limit threshold, the current limit comparator will unconditionally turn off the internal power switch. At the beginning of the next oscillator cycle, the switch is allowed to turn on again.

The voltage feedback loop works by monitoring the LED drive current through a resistor divider on FB and comparing that voltage with an internal reference voltage (V_{ref}). If the LED current falls below the set current, the voltage on the feedback pin will drop slightly below Vref causing Vc to increase. This will keep the PWM comparator's output high for a greater portion of an oscillator cycle, thus ensuring that the FET will stay on longer. This, in turn, will allow more current to be delivered to the load. Following similar logic, should the LED current become higher than the set current, FB voltage will increase above Vref, the converter will decrease its duty cycle, which will lessen the energy delivered to the load at each cycle, and thereby, reduce LED current and maintain desired brightness.

In essence, by modifying the on time of the switch, the PWM comparator continually sets the correct maximum current through the FET to regulate the LED current to a desired value.

POWER DISSIPATION CONSIDERATIONS:

An important consideration when designing power converters is the maximum allowable power dissipation of a part. The maximum power dissipation in any application is dependant on the maximum junction temperature, $T_{J(MAX)}$ = 125 °C, the junction-to-ambient thermal resistance for the MLP33-6 package, Θ_{J-A} = 50 °C/W, and the ambient temperature, T_A, which may be formulaically expressed as:

$$P_{(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{J-A}} = \frac{125 - T_A}{50}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 1.1 watts.

In the event that the power dissipation exceeds the value specified above and the die temperature reaches 160 °C, the internal thermal protection circuitry will ensure safe operation by turning off the internal FET, thereby maintaining junction temperature at a safe level. In this state, only the system monitor circuitry will be active. Once the temperature of the chip drops below 135 °C, the chip re-enters soft-start mode and resumes normal operation.

DIODE SELECTION:

A schottky diode is recommended for use as the external rectifier. Schottky diodes are typically preferred in DC-DC conversion applications because of their low forward voltage drop and fast recovery time, which allows for high frequency switching. In choosing a diode, ensure that the diode's reverse breakdown voltage exceeds the intended V_{OUT} of design and that its current rating is greater then the peak inductor current. For applications in which less than 0.5 A of average output current is required and output voltage is less than 15 V, a diode such as the MBR0520 is recommended. For V_{OUTs} higher than 15 V, a 30 V diode such as the MBR0530 should be considered.

INPUT CAPACITOR SELECTION:

The input bypass capacitor acts as an energy reservoir that satisfies the transient inductor current needs each time the switch turns on. In effect, the input capacitor is responsible for reducing the input voltage ripple and the amount of EMI that is inevitably passed to other circuitry on that line. For this purpose, a 4.7 µF ceramic capacitor is recommended. If preferred, tantalum capacitors may be used instead of ceramics.

OUTPUT CAPACITOR SELECTION:

To curb output voltage ripple, a multi-layer ceramic capacitor should be used as the output filter capacitor. Ceramic capacitors are favored for their low ESR (equivalent series resistance) and high resonance frequency which makes them ideal for high frequency switching converters. A high ESL (equivalent series inductance) can give rise to ringing in the low megahertz region and a high ESR could reduce phase margin and potentially cause instability of the design. In addition, the ripple current flowing through the capacitor's ESR causes power dissipation and heats up the capacitor internally. If the ripple current ratings of the capacitor are exceeded, the excessive temperature could shorten the expected life of the capacitor.

If a high value capacitor is required for improved transient response, to keep component costs down and to save PC board real estate, tantalum capacitor may be used in parallel with ceramics. If the maximum tolerated ripple current (I_{P-P}) and ripple voltage (ΔV_O) design specifications are known, the maximum tolerated ESR on the output capacitor and its value can be calculated using the following formulas:

$$ESR_{(MAX)} = \frac{\Delta V_{OUT}}{\left(\frac{1}{1 - D_{MAX}} \times I_{OUT\,(MAX)} + \frac{I_{P-P}}{2}\right)}$$

$$C_{OUT\,(MIN)} = \frac{I_{OUT\,(MAX)} \times D_{MAX}}{f_{SW} \times \Delta V_{OUT}}$$

Where $I_{OUT\,(MAX)}$ is the maximum output current and D_{MAX} represents the maximum duty cycle.

DUTY CYCLE CALCULATION:

In continuous mode of operation, the maximum duty cycle of a boost switching regulator determines the maximum amount of boost (V_{OUT}/V_{IN}) attainable and can be calculated using the expression

$$D_{(MAX)} = \frac{V_{OUT} + V_{Diode} - V_{IN}}{V_{OUT} + V_{Diode} - V_{SW}}$$

Where V_{Diode} is the forward bias voltage of the schottky diode and Vsw denotes the voltage drop across the internal switch and can be expressed as

$$V_{SW} = R_{DS(on)} \times I_{L(PEAK)}$$

The above equation yields only an approximation of the duty cycle since it ignores power loss terms resulting from wire losses in the inductor, switching losses of the internal FET, and capacitor ripple current losses due to their inherent non-zero ESR. A more accurate estimate of the duty cycle can be determined by

$$D = 1 - \text{Efficiency} \times \frac{V_{IN}}{V_{OUT}}$$

And by using the provided efficiency curves to approximate efficiency for a given input and output voltage.

INDUCTOR SELECTION:

An inductor is one of the energy storage components in a converter. Choosing an inductor means specifying its size, structure, material, inductance, saturation level, DC-resistance (DCR), and core loss. Choosing the right inductor is not a simple task and involves tradeoffs in performance. The following are some key parameters that should be focused on. In PWM mode, inductance has a direct impact on the ripple current. The peak-to-peak inductor ripple current can be calculated as

$$I_{p-p} = \frac{D \times (V_{IN} - V_{sw})}{L \times f_{sw}}$$

Where Vsw is the voltage drop across the switch in its on state, fsw is the switching frequency, and D is the duty cycle. Higher inductance means lower ripple current, lower rms current, lower voltage ripple on both input and output, and higher efficiency, unless the resistive loss of the inductor dominates the overall conduction loss. However, higher inductance also means a larger inductor size and a slower transient response. For fixed line, load, and frequency conditions, higher inductance results in a lower peak current for each pulse and a higher load capability.

The saturation current is another important parameter in choosing inductors. Note that the saturation levels specified in data sheets are maximum currents. For a DC-DC converter operating in PWM mode, it is the maximum peak inductor current that is relevant, and which can be calculated using these equations:

$$I_{PEAK} = I_{L(avg)} + \frac{I_{p-p}}{2}, I_{L(avg)} = \frac{I_{OUT}}{1 - D}$$

This peak current varies with inductance tolerance and other errors, and the rated saturation level varies over temperature. So a sufficient design margin is required when choosing current ratings.

A high-frequency core material, such as ferrite, should be chosen, the core loss could lead to serious efficiency penalties. The DCR should be kept as low as possible to reduce conduction losses.

LAYOUT CONSIDERATIONS:

In high frequency switching regulators such as the SiP12506, great attention must be given to the layout process in order to ensure stable operation and minimize noise. Since most power traces in step up converters carry pulsating current, energy stored in trace inductance during the pulse can cause high-frequency ringing with input and output capacitors. This effect can generally be curbed by minimizing the length and increasing the width of power traces.

To minimize stray capacitance and even more importantly, parasitic trace inductance, all components must be kept as close to the switcher as possible. Of special importance, is the path between the switching node LX, D1, C2, and ground of the regulator; the length of this path must be kept as small as possible since any parasitic inductance in series with the diode and output capacitance will increase noise and produce ringing in the circuit.

Pulsating currents in the ground trace can cause voltage drops due to trace resistance and cause ground bounce. For this reason, it is strongly recommended to use a separate ground plane. V_{Bias} should be used at the negative ends of capacitors C3 and C2 as well as the device GND pin to connect to the ground the plane.

The feedback components (R1, R2) should be kept close to the FB pin and the trace connecting the negative end of R2 to ground should be kept thin in order to minimize noise injection into the feedback pin. As an example, Figure 5 demonstrates a recommended layout of components. It is urged that this layout be followed closely as possible to obtain best performance.

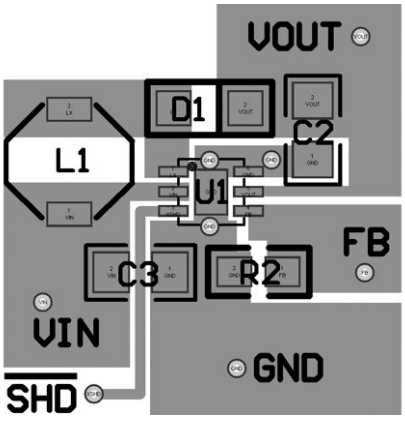


Figure 5.

START UP AND SOFT-START:

When voltage is applied to the V_{IN} pin, the undervoltage lockout (UVLO) circuit prevents the controller's output switch and oscillator circuit from turning on until the voltage on the V_{IN} pin exceeds 2.4 V. Provided the V_{IN} pin is above this threshold, when $\overline{SHD}$ pin is raised high, soft-start is initiated. Soft-start is achieved by slowly ramping up the internal reference. Once the soft-start time has elapsed, SiP12506 enters into a normal state of operation. The converter then operates continuously unless the voltage on V_{IN} drops below 2.4 V or $\overline{SHD}$ is set low. UVLO hysteresis prevents the converter from dropping in and out of start-up, unintentionally locking up the system.

LED CURRENT CONTROL:

The SiP12506 is a white LED driver. The low feedback voltage of 0.208 V is designed to reduce losses outside of the white LEDs and thus improve overall circuit efficiency. The LED current is set by the small sense resistor on FB and can be calculated using the following expression:

$$I_{LED} = \frac{V_{ref}}{R_{FB}} = \frac{0.208\ V}{R_{FB}}$$

In order to have accurate LED current, use of 1 % precision resistor is recommended.

As shown in Figures 6 and 7, the SiP12506 can be used to drive four LEDs in series or to drive parallel strings of LEDs.

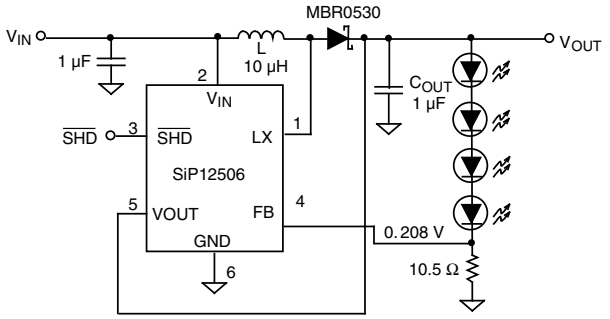


Figure 6. SiP12506 Driving Four LEDs

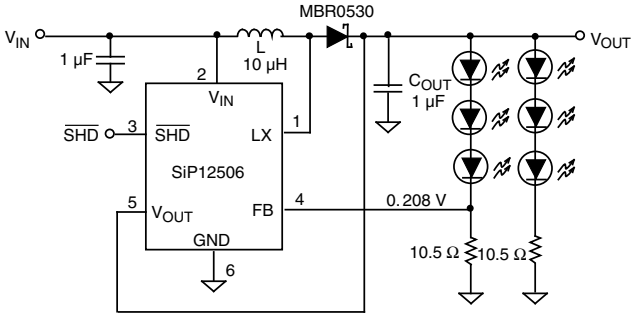


Figure 7. SiP12506 Driving Six LEDs

WHITE LED BRIGHTNESS CONTROL

Figures 8 and 9 delineate two possible brightness control schemes. In Figure 8, a PWM signal is injected into the shutdown pin. The average LED current is proportional to the duty cycle of the PWM signal and thus, the brightness will vary from low to high as the duty cycle of the PWM signal is increased. The frequency of the PWM signal has to be low enough to allow the part to undergo soft-start and fully power up at each cycle. A frequency of 100 Hz to 500 Hz is, therefore, recommended. The magnitude of the PWM signal should be higher than the maximum enable voltage of $\overline{SHD}$ pin, in order to let the dimming control perform correctly.

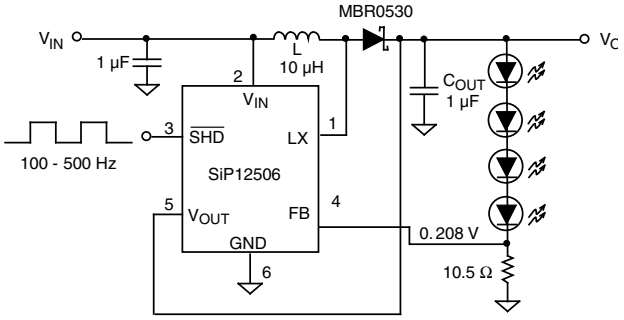


Figure 8. SiP12506 Driving Four LEDs

In Figure 9, a more analog approach to brightness control. As the control voltage V_{CTRL} is increased from 0 V, the voltage drop across R2 and R3 increases driving voltage on node A low thereby reducing current through the White LEDs and dimming brightness. Reducing V_{CTRL} to about 0 V, will turn the LEDs fully on with 20 mA of current. The equation for the LED current can be expressed as

$$I_{LED} = \frac{0.208\ V}{15\ \Omega} + \frac{R2}{R3} \times \frac{(0.208\ V - V_{CTRL})}{15\ \Omega}$$

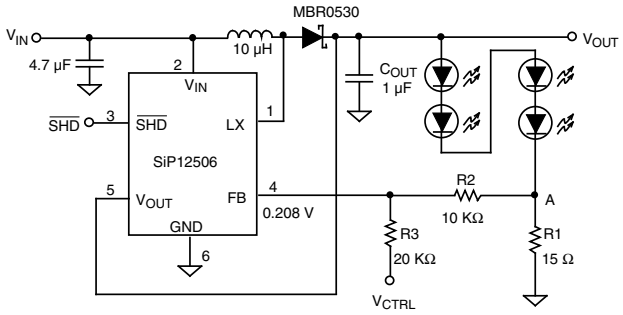


Figure 9. White LED driver with adjustable brightness

Figure 10 demonstrates a more practical approach for dimming control which is really the synthesis of the two ideas demonstrated above. In this approach, a filtered PWM signal acts as a DC voltage to control the brightness of the LEDs. It is recommended that PWM signal with frequency higher than 22 kHz be used. Figures 11 and 12 illustrate other variations of the previously mentioned ideas.

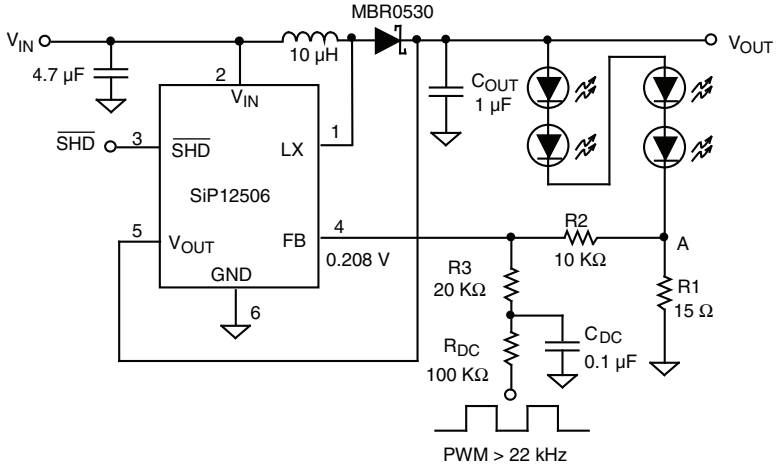


Figure 10. White LED driver with adjustable brightness control using a filtered PWM signal

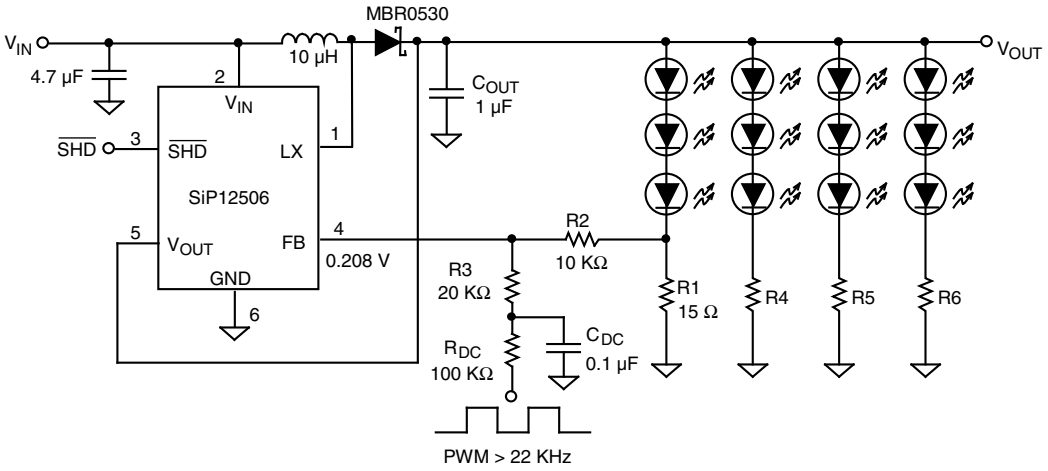


Figure 11. White LED driver with adjustable brightness control using a filtered PWM signal

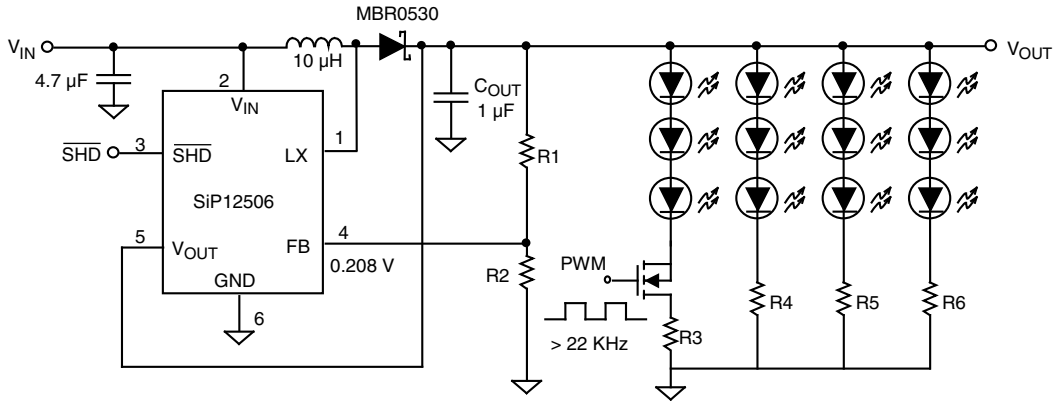


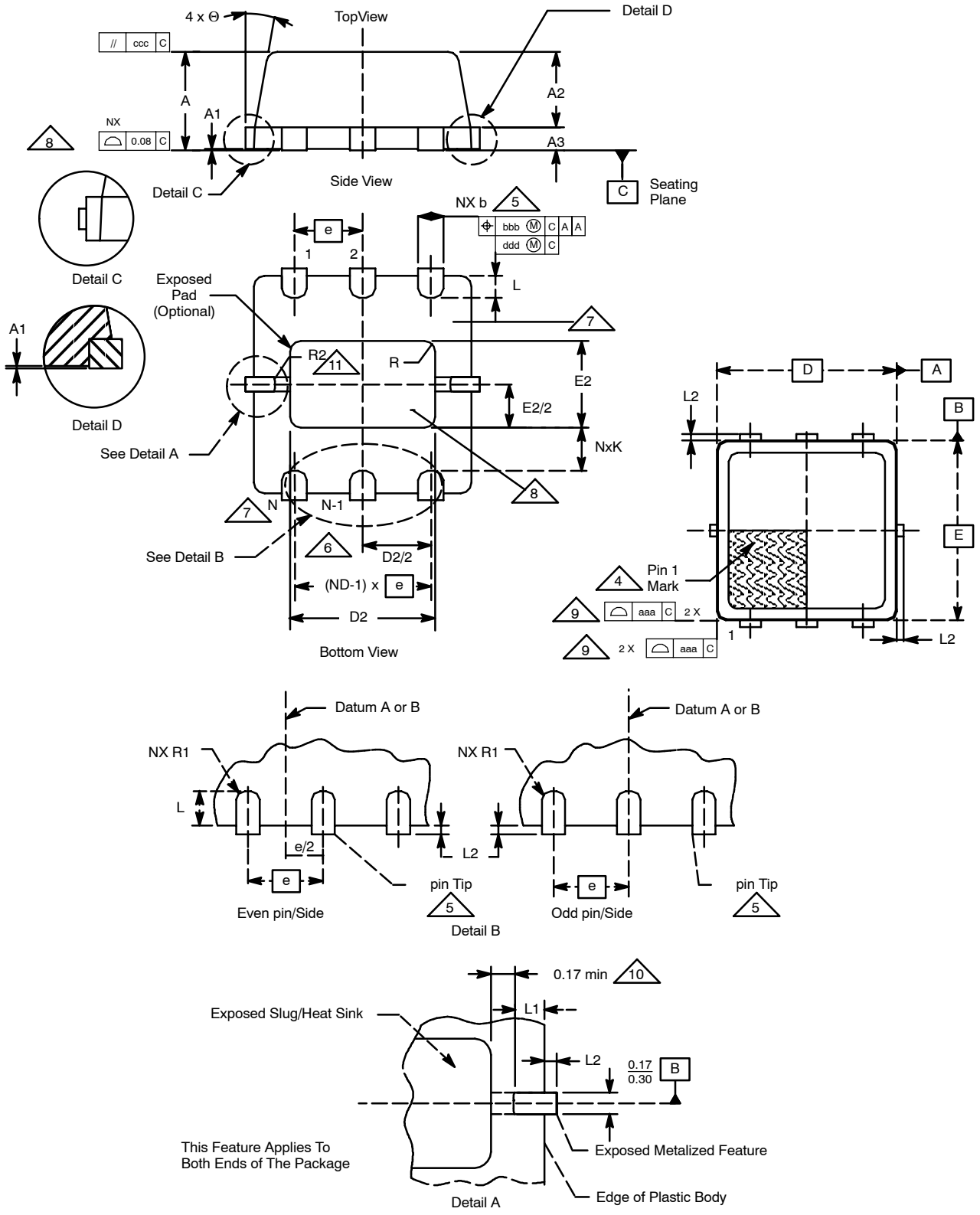
Figure 12. White LED driver with a fixed output and adjustable brightness control using a filtered PWM signal

OPEN-CIRCUIT PROTECTION:

In the event of an output open circuit (e.g. when the LEDs are either disconnected form the output or an LED fails), the feedback voltage will become zero causing the SiP12506 to go to maximum duty cycle. This would generally result in a high output voltage and, possibly, cause the voltage on the LX pin to exceed it's absolute maximum rating and damage the part. However, the SiP12506 has a built-in over-voltage protection circuitry that will clamp the output to 20 V and guarantee safe operation under open-circuit conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73861.

PowerPAK® MLP33-6, 8 and 10 (POWER IC ONLY)



PowerPAK® MLP33-6, 8, 10

N = 6 PITCH: 0.95 mm
N = 8 PITCH: 0.65 mm
N = 10 PITCH: 0.50 mm

Dim	MILLIMETERS*				INCHES				Notes
	Basic	Min	Nom	Max	Basic	Min	Nom	Max	
A	–	0.80	0.90	1.00	–	0.031	0.035	0.039	1, 2
A1	–	0.00	0.025	0.05	–	0.000	0.001	0.002	1, 2
A2	–	0.65	0.70	0.75	–	0.026	0.028	0.030	1, 2
A3	–	0.15	0.20	0.25	–	0.006	0.008	0.010	1, 2
aaa	–	–	0.10	–	–	–	0.004	–	1, 2
b-6	–	0.33	0.35	0.43	–	0.013	0.014	0.017	1, 2, 8
b-8	–	0.285	0.305	0.385	–	0.011	0.012	0.015	1, 2, 8
b-10	–	0.18	0.20	0.28	–	0.007	0.008	0.011	1, 2, 8
bbb	–	–	0.10	–	–	–	0.004	–	1, 2
ccc	–	–	0.10	–	–	–	0.004	–	1, 2
D	3.00	–	–	–	0.118	–	–	–	1, 2, 8
D2	–	1.92	2.02	2.12	–	0.076	0.080	0.083	1, 2, 8
ddd	–	–	0.05	–	–		0.002		1, 2
E	3.00	–	–	–	0.118	–	–	–	1, 2, 8
E2	–	1.10	1.20	1.30	–	0.043	0.047	0.051	1, 2, 8
e-6	–	–	0.95	–	–	–	0.037	–	1, 2
e-8	–	–	0.65	–	–	–	0.026	–	1, 2
e-10	–	–	0.50	–	–	–	0.020	–	1, 2
K	–	0.20	–	–	–	0.008	–	–	5, 11
L	–	0.20	0.29	0.45	–	0.008	0.011	0.018	1, 2, 8
L1-6	–	0.16	0.24	0.40	–	0.006	0.009	0.016	1, 2, 8
L1-8	–	0.16	0.24	0.40	–	0.006	0.009	0.016	1, 2, 8
L1-10	–	–	–	–	–	–	–	–	1, 2, 8
L2	–	–	–	0.125	–	–	–	0.005	5, 11
R Ref	–	–	0.15	–	–	–	0.006	–	1, 2, 8
R1 Ref-6	–	–	0.127	–	–	–	0.005	–	1, 2, 8
R1 Ref-8	–	–	0.15	–	–	–	0.006	–	1, 2, 8
R1 Ref-10	–	–	0.075	–	–	–	0.003	–	1, 2, 8
Θ	–	0°	10°	12°	–	0°	10°	12°	1, 2

* Use millimeters as the primary measurement.

ECN: S-40082—Rev. A, 02-Feb-04
DWG: 5925

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angels are in degrees.
3. N is the total number of pins.
4. The pin #1 identifier and pin numbering convention shall conform to JESD 95-1 SPP-012. Details of pin #1 identifier is located within the zone indicated. The pin #1 identifier is marked.
5. Dimension b applies to metallized pin and is measured between 0.15 mm and 0.20 mm from the pin tip.
6. ND refers to the maximum number of pins on the D side.
7. Depopulation of pins is allowed and will be called out on the individual variation.
8. Coplanarity applies to the exposed heat sink slug as well as the pins.
9. Profile tolerance (aaa) will be applicable only to the plastic body and not to the metallized features (such as the pin tips and tie bars.) Metallized features may protrude a maximum of L2 from the plastic body profile.
10. L1 max is not called out, the metallized feature will extend to the exposed pad. Thus, the 0.17-mm gap does not apply.
11. The corner will be sharp unless otherwise specified with radius dimensions.

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Vishay:
SIP12506DMP-T1-E3