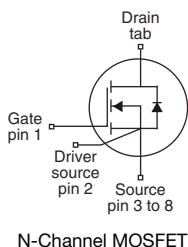


E Series Power MOSFET



FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	650
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V 0.070
Q_g max. (nC)	62
Q_{gs} (nC)	17
Q_{gd} (nC)	9
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 10 x 12
Lead (Pb)-free and halogen-free	SiHK075N60E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	600	V
Gate-source voltage		V_{GS}	± 30	
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	I_D	29	A
			18	
Pulsed drain current ^a		I_{DM}	75	
Linear derating factor			1.33	W/°C
Single pulse avalanche energy ^b		E_{AS}	204	mJ
Maximum power dissipation		P_D	167	W
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	$T_J = 125$ °C	dv/dt	100	V/ns
Reverse diode dv/dt ^d			23	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω, $I_{AS} = 3.8$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $di/dt = 100$ A/μs, starting $T_J = 25$ °C

THERMAL RESISTANCE RATINGS

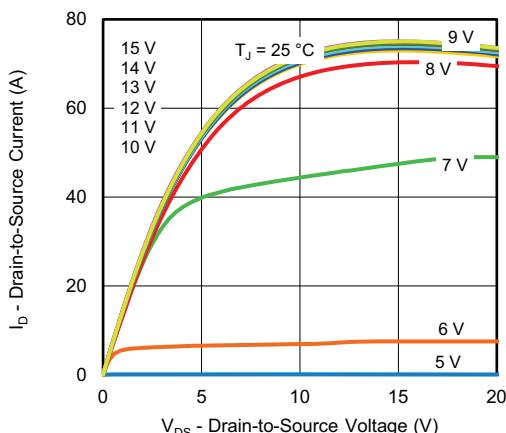
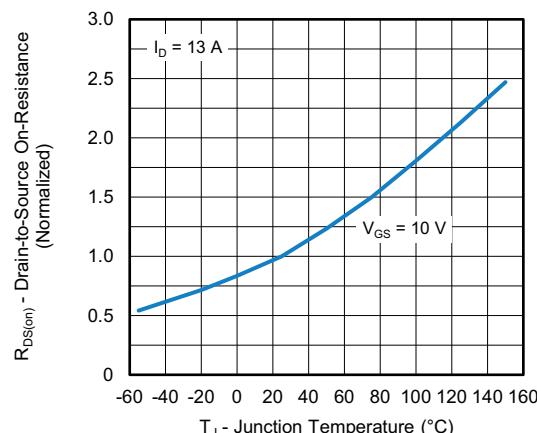
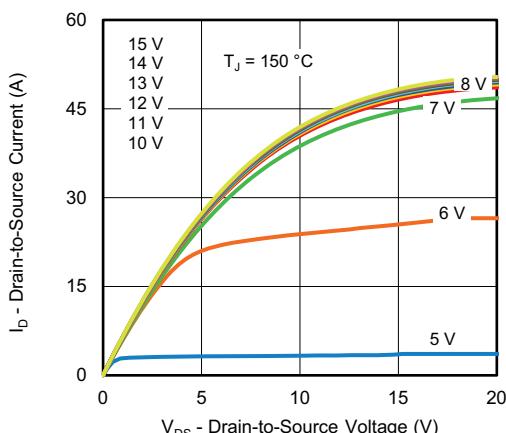
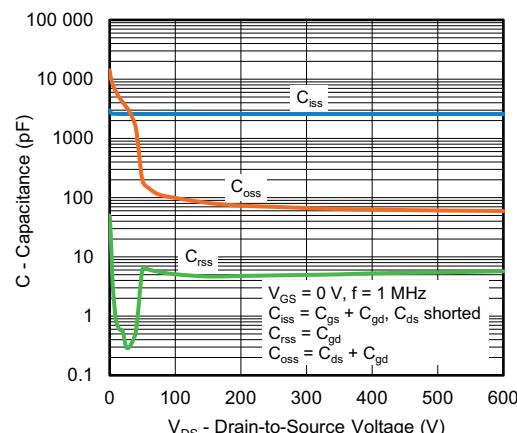
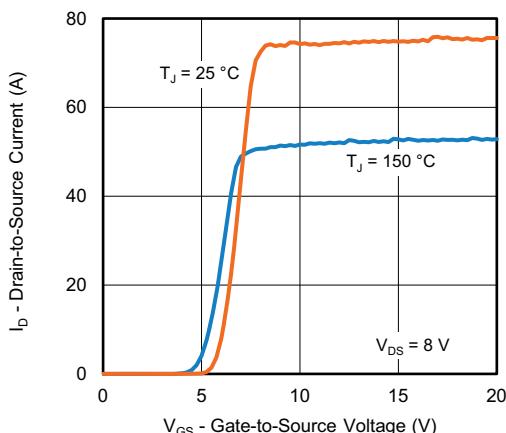
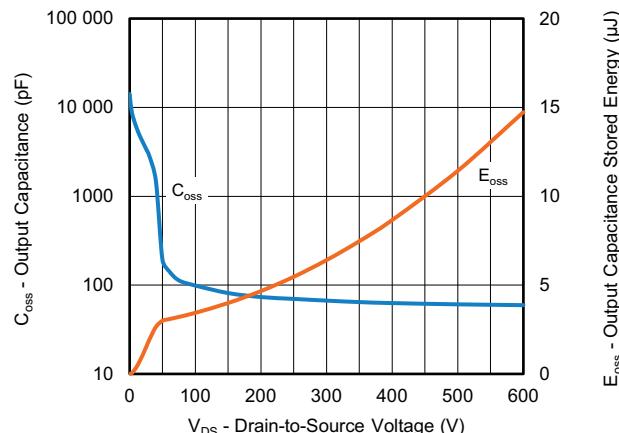
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	50 °C	
Maximum junction-to-case (drain)	R_{thJC}	-	0.75	°C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A		600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1$ mA		-	0.64	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A		3.0	-	5.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20$ V		-	-	± 100	nA
		$V_{GS} = \pm 30$ V		-	-	± 1	μ A
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 600$ V, $V_{GS} = 0$ V		-	-	1	
		$V_{DS} = 480$ V, $V_{GS} = 0$ V, $T_J = 125$ °C		-	-	10	μ A
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 13$ A	-	0.070	0.080	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 10$ V, $I_D = 13$ A		-	2.3	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 100$ V, $f = 1$ MHz		-	2582	-	pF
Output capacitance	C_{oss}			-	99	-	
Reverse transfer capacitance	C_{rss}			-	5	-	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{DS} = 0$ V to 480 V, $V_{GS} = 0$ V		-	75	-	
Effective output capacitance, time related ^b	$C_{o(tr)}$			-	474	-	
Total gate charge	Q_g			-	41	62	nC
Gate-source charge	Q_{gs}	$V_{GS} = 10$ V	$I_D = 13$ A, $V_{DS} = 480$ V	-	17	-	
Gate-drain charge	Q_{gd}			-	9	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 480$ V, $I_D = 13$ A, $V_{GS} = 10$ V, $R_g = 9.1$ Ω		-	26	52	ns
Rise time	t_r			-	26	52	
Turn-off delay time	$t_{d(off)}$			-	45	90	
Fall time	t_f			-	12	24	
Gate input resistance	R_g	$f = 1$ MHz		0.4	0.8	1.6	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	29	A
Pulsed diode forward current	I_{SM}			-	-	75	
Diode forward voltage	V_{SD}	$T_J = 25$ °C, $I_S = 13$ A, $V_{GS} = 0$ V		-	-	1.2	V
Reverse recovery time	t_{rr}	$T_J = 25$ °C, $I_F = I_S = 13$ A, $di/dt = 100$ A/ μ s, $V_R = 25$ V		-	317	816	ns
Reverse recovery charge	Q_{rr}			-	4.2	12.8	μ C
Reverse recovery current	I_{RRM}			-	23	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
c. When mounted on 1" x 1" FR4 board

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

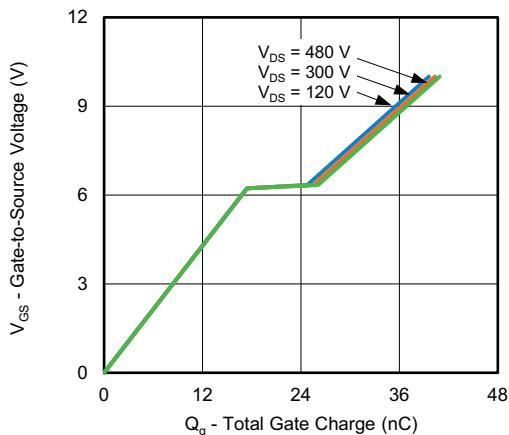


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

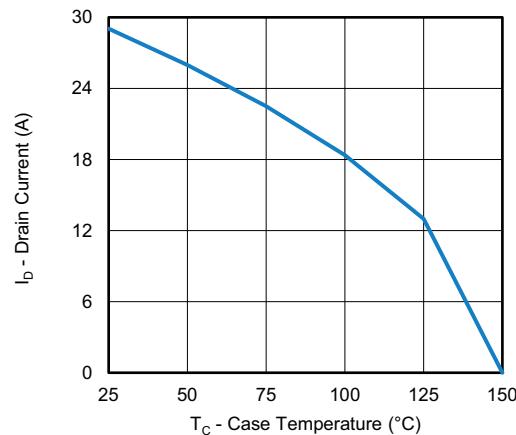


Fig. 10 - Maximum Drain Current vs. Case Temperature

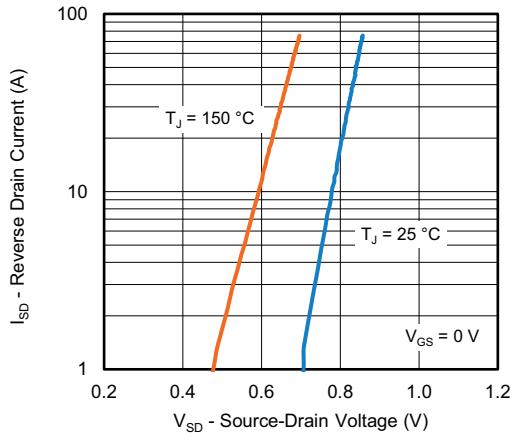


Fig. 8 - Typical Source-Drain Diode Forward Voltage

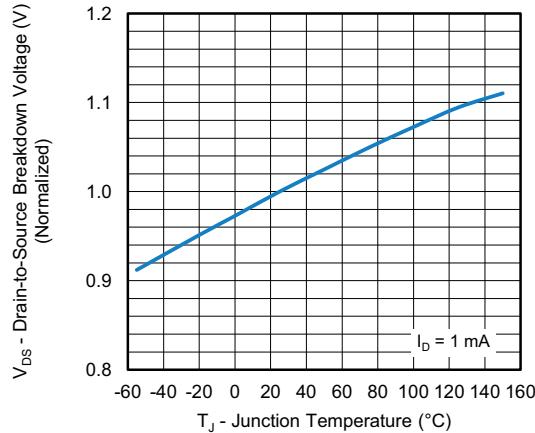


Fig. 11 - Temperature vs. Drain-to-Source Voltage

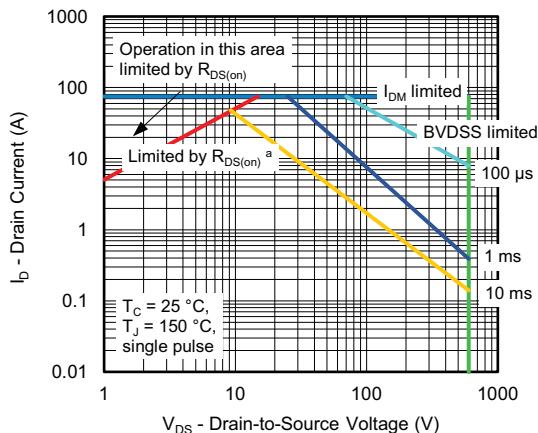


Fig. 9 - Maximum Safe Operating Area

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

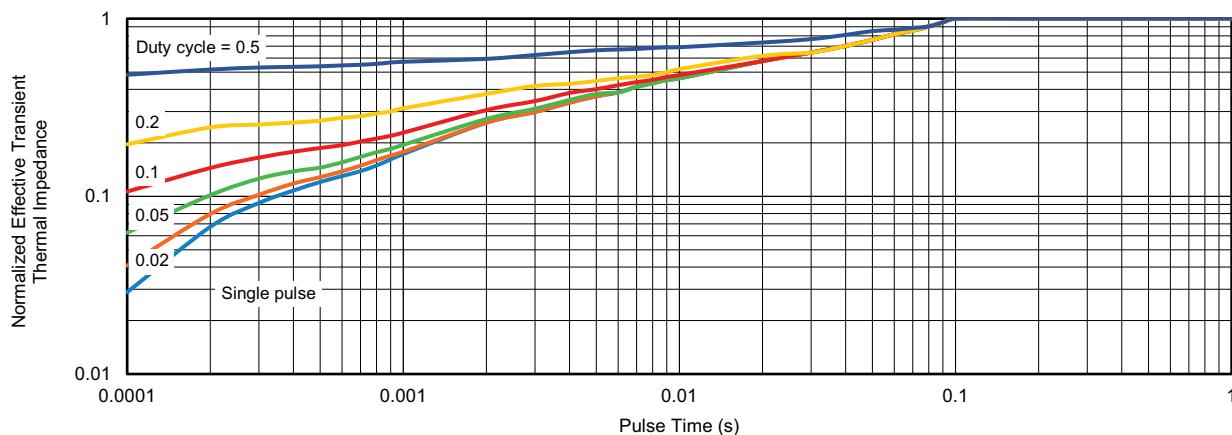


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

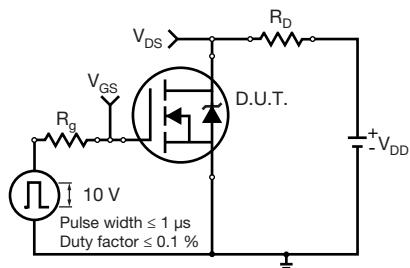


Fig. 13 - Switching Time Test Circuit

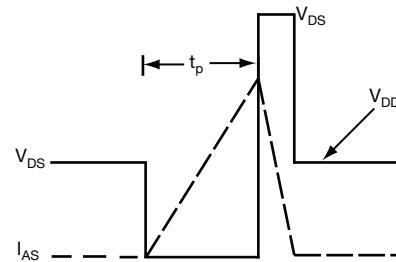


Fig. 16 - Unclamped Inductive Waveforms

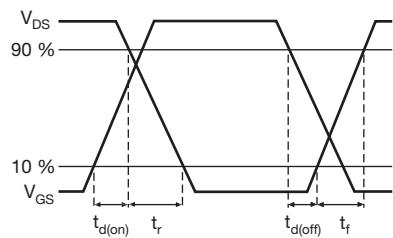


Fig. 14 - Switching Time Waveforms

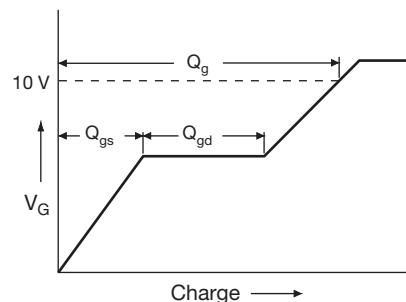


Fig. 17 - Basic Gate Charge Waveform

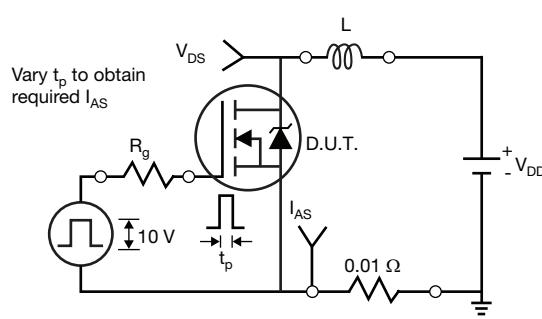


Fig. 15 - Unclamped Inductive Test Circuit

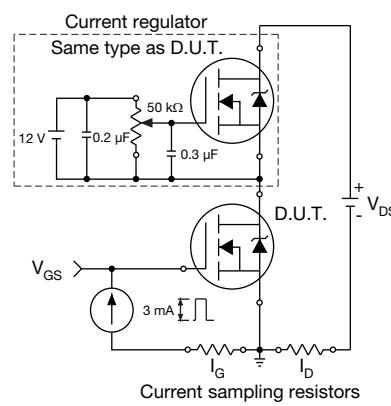


Fig. 18 - Gate Charge Test Circuit

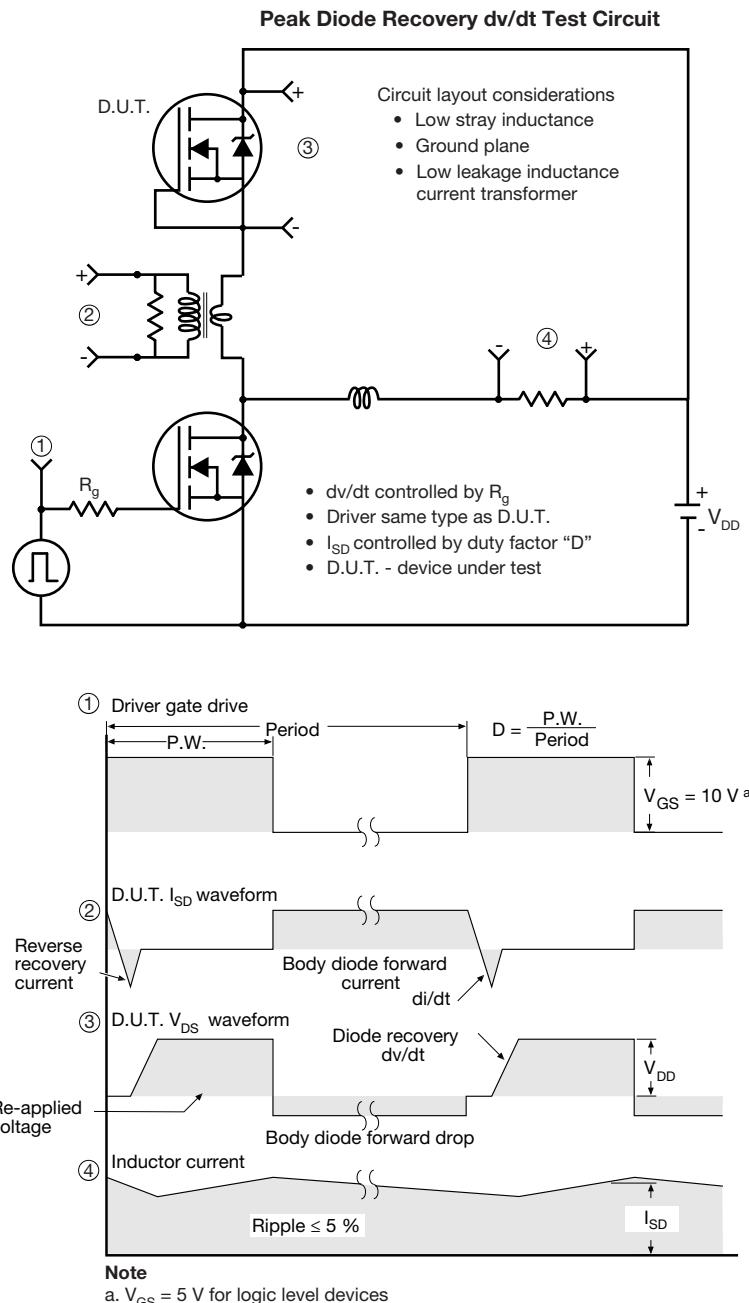


Fig. 19 - For N-Channel

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