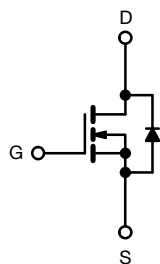
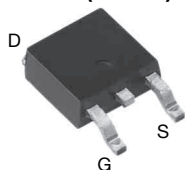


Power MOSFET

DPAK (TO-252)


N-Channel MOSFET

FEATURES

- Low drive current
- Surface-mount
- Fast switching
- Ease of paralleling
- Excellent temperature stability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt capability.

The power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The DPAK (TO-252) surface-mount package brings the advantages of power MOSFET's to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9012, SiHFR9012 is provided on 16 mm tape. The straight lead option IRFU9012, SiHFU9012 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, dc-to-dc converters, and a wide range of consumer products.

PRODUCT SUMMARY

V _{DS} (V)	50	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.20
Q _g (Max.) (nC)	10	
Q _{gs} (nC)	2.6	
Q _{gd} (nC)	4.8	
Configuration	Single	

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)
Lead (Pb)-free and halogen-free	SiHFR010-GE3	SiHFR010TR-GE3	SiHFR010TRL-GE3	IRFR010PbF-BE3
Lead (Pb)-free	IRFR010PbF	IRFR010TRPbF	IRFR010TRLPbF	IRFR010TRRPbF

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	50	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed drain current ^a	I _{DM}	33	
Avalanche current ^b	I _{AS}	1.5	
Linear derating factor		0.20	W/°C
Maximum power dissipation	P _D	25	W
Peak diode recovery dV/dt ^c	dV/dt	2.0	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	

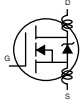

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DD} = 25 V, starting T_J = 25 °C, L = 100 μH, R_g = 25 Ω
- I_{SD} ≤ 8.2 A, dI/dt ≤ 130 A/μs, V_{DD} ≤ 40 V, T_J ≤ 150 °C
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	-	110	°C/W
Case-to-sink	R_{thCS}	-	1.7	-	
Maximum junction-to-case (drain)	R_{thJC}	-	-	5.0	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		50	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 500	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 50 V, V _{GS} = 0 V		-	-	250	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 125 °C		-	-	1000	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 4.6 A ^b	-	0.16	0.20	Ω
Forward transconductance	g _{fs}	V _{DS} ≥ 50 V, I _D = 3.6 A		2.1	3.1	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 10		-	250	-	pF
Output capacitance	C _{oss}			-	150	-	
Reverse transfer capacitance	C _{rss}			-	29	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 7.3 A, V _{DS} = 40 V, see fig. 6 and 13 ^b	-	6.7	10	nC
Gate-source charge	Q _{gs}			-	1.8	2.6	
Gate-drain charge	Q _{gd}			-	3.2	4.8	
Turn-on delay time	t _{d(on)}	V _{DD} = 25 V, I _D = 7.3 A, R _g = 24 Ω, R _D = 3.3 Ω, see fig. 10 ^b		-	11	17	ns
Rise time	t _r			-	33	50	
Turn-off delay time	t _{d(off)}			-	12	18	
Fall time	t _f			-	23	35	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact ^c 		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	8.2	A
Pulsed diode forward current ^a	I _{SM}			-	-	33	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 8.2 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 7.3 A, dI/dt = 100 A/μs ^b		41	86	190	ns
Body diode reverse recovery charge	Q _{rr}			0.15	0.33	0.78	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

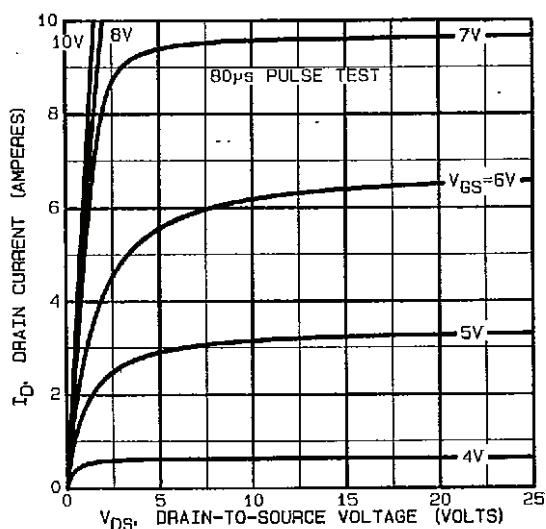


Fig. 1 - Typical Output Characteristics

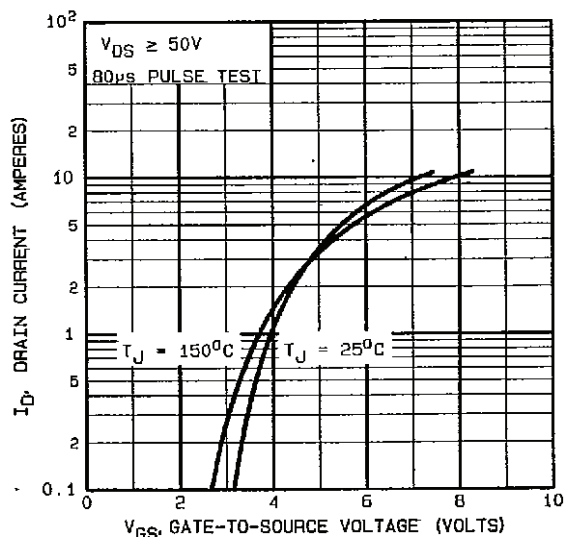


Fig. 2 - Typical Transfer Characteristics

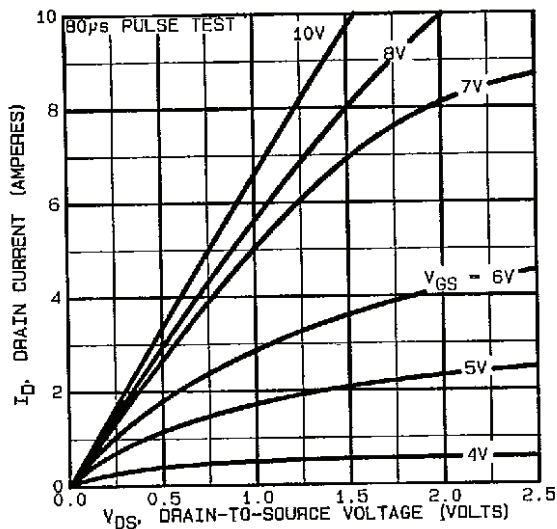


Fig. 1 - Typical Output Characteristics

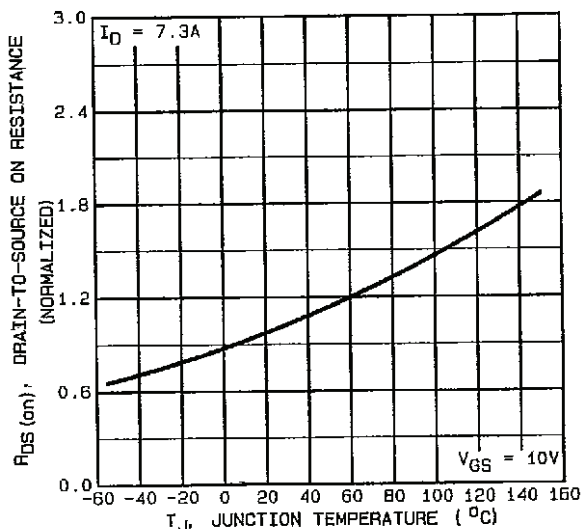


Fig. 3 - Normalized On-Resistance vs. Temperature

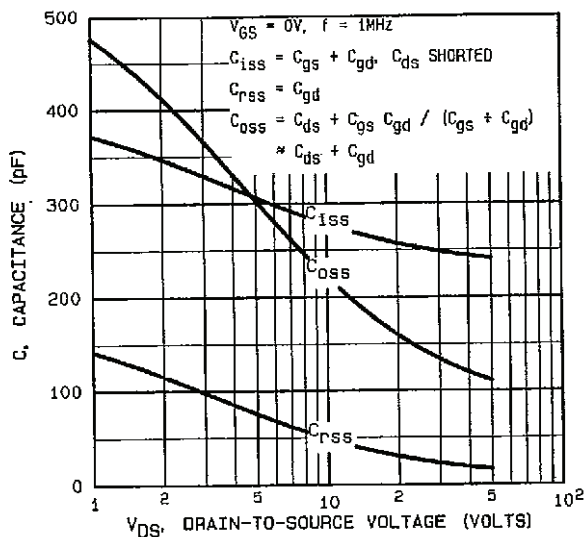


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

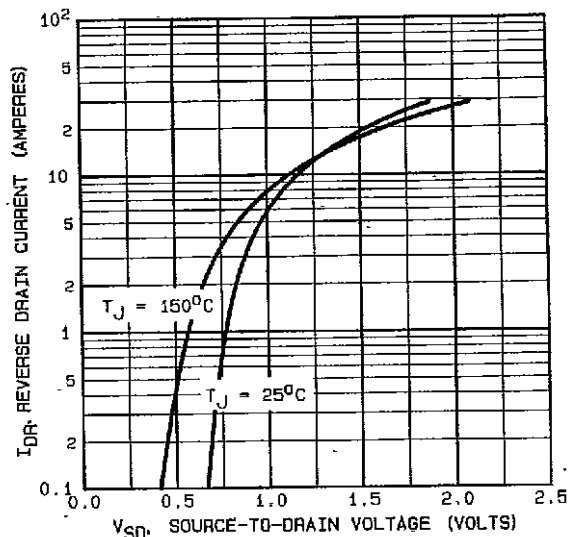


Fig. 6 - Typical Source-Drain Diode Forward Voltage

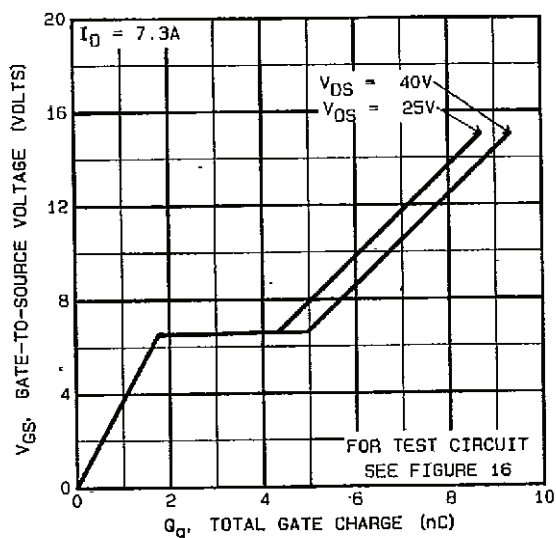


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

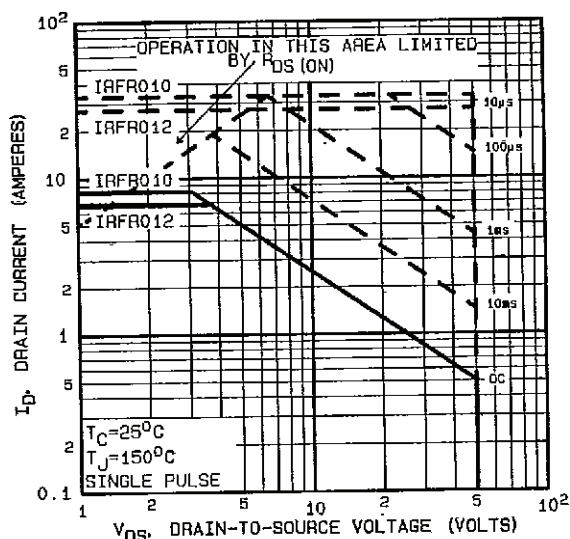
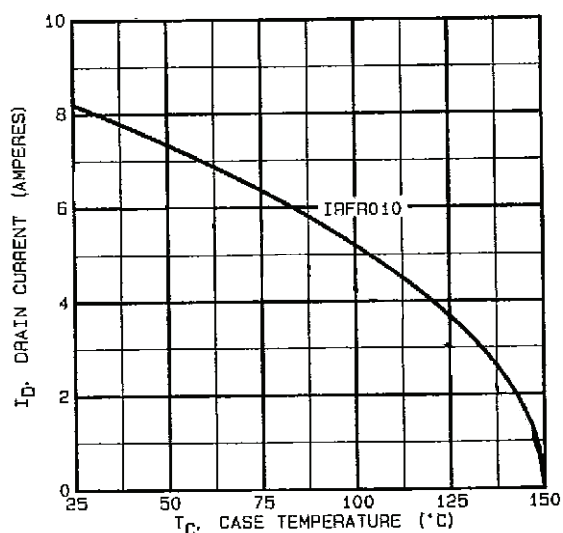
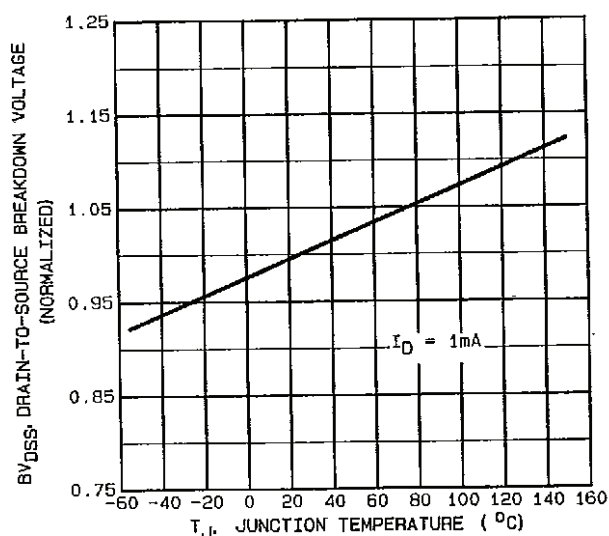
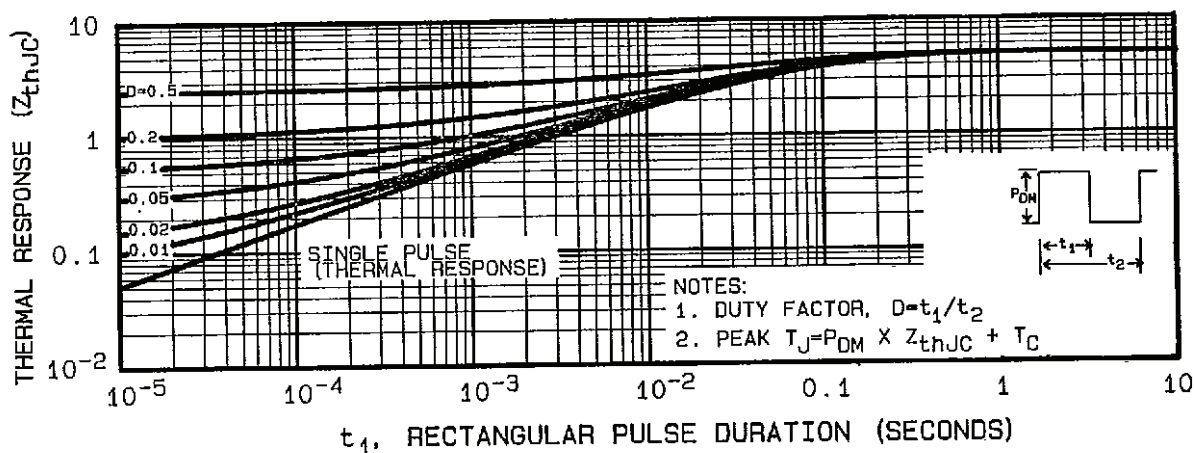
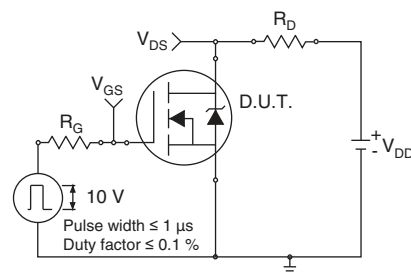
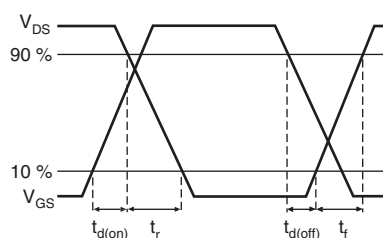


Fig. 7 - Maximum Safe Operating Area


Fig. 8 - Maximum Drain Current vs. Case Temperature

Fig. 9 - Breakdown Voltage vs. Temperature

Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

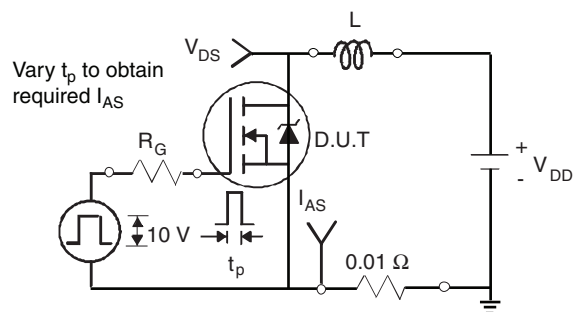
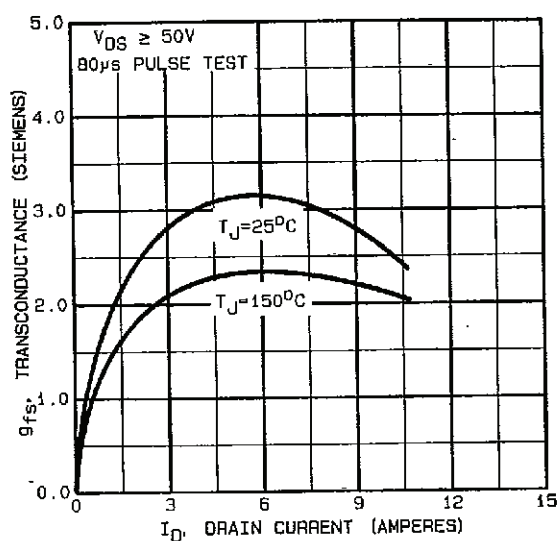
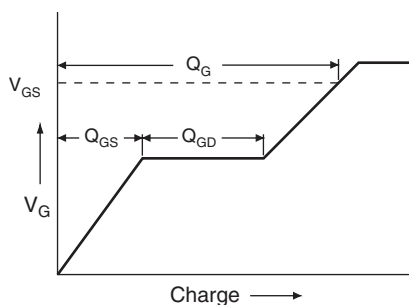
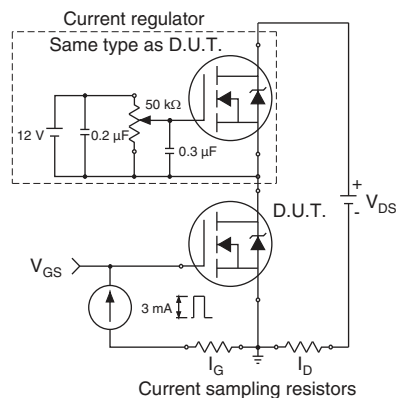
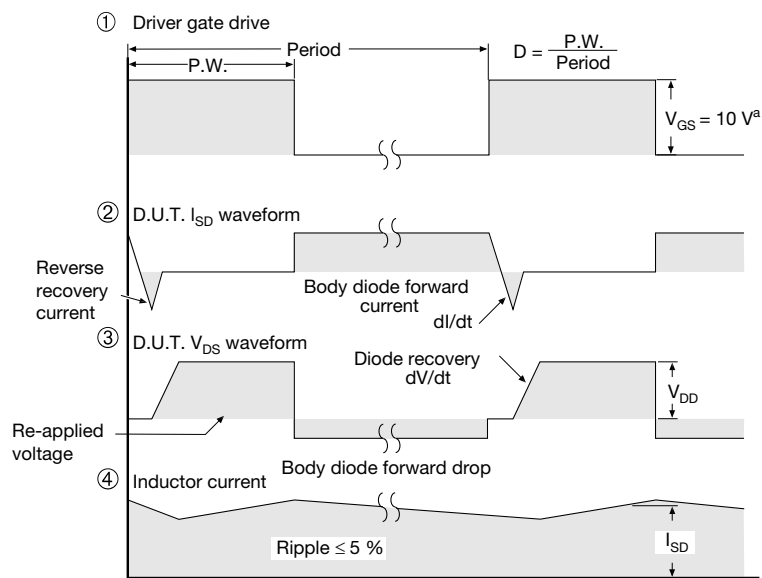
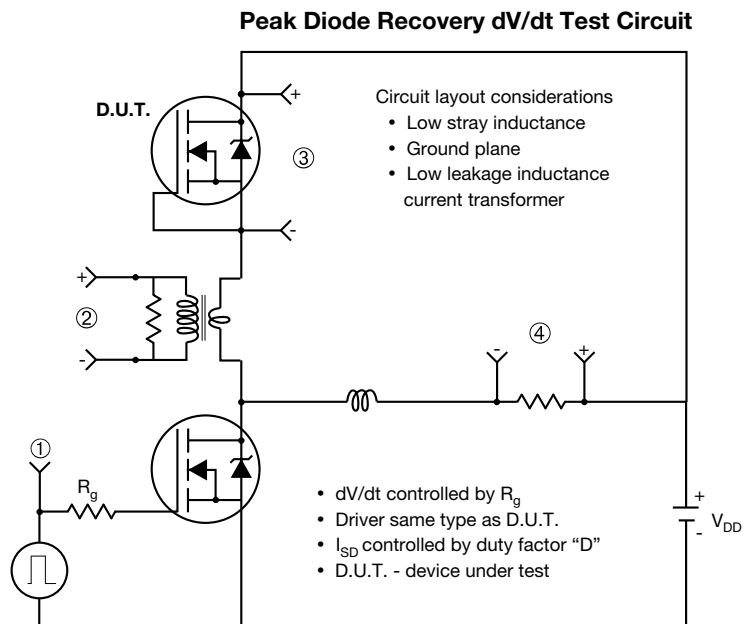

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Typical Transconductance vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit


Note

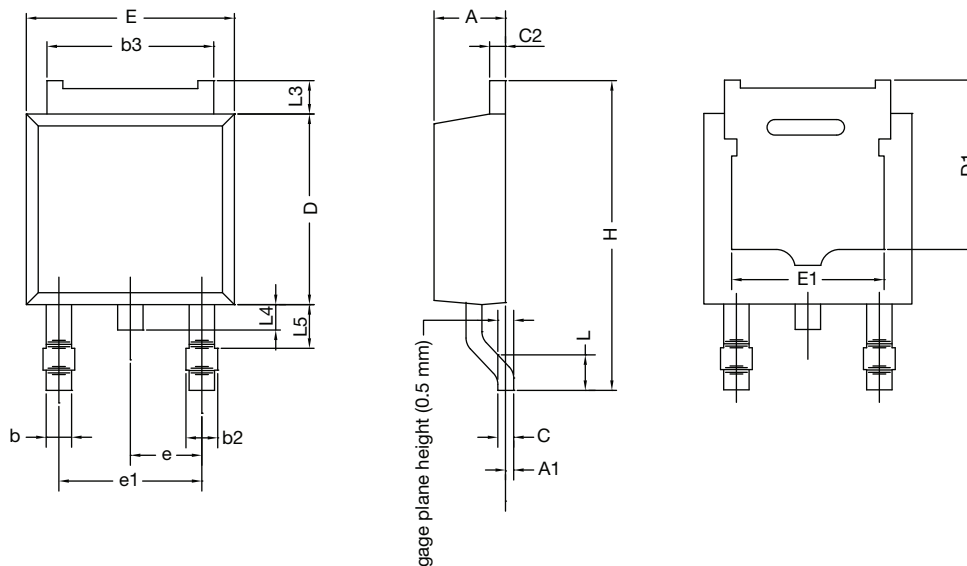
a. $V_{GS} = 5 V$ for logic level devices

Fig. 11 - For N-Channel

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TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

DIM.	MILLIMETERS	
	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
theta	0°	10°
theta1	0°	15°
theta2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E19-0649-Rev. Q, 16-Dec-2019
DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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