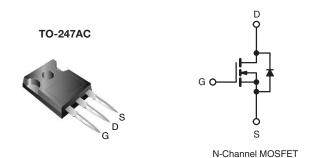


Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	600		
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.58		
Q _g (Max.) (nC)	70		
Q _{gs} (nC)	19		
Q _{gd} (nC)	28		
Configuration	Single		



FEATURES

ullet Low Gate Charge $\mathbf{Q}_{\mathbf{g}}$ Results in Simple Drive Requirement



 Improved Gate, Avalanche and Dynamic dV/dt RoHS Ruggedness

- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss Specified
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGY

PFC Boost

ORDERING INFORMATION	
Package	TO-247AC
Load (Dh) fros	IRFPC50APbF
Lead (Pb)-free	SiHFPC50A-E3
SnPb	IRFPC50A
SIIFU	SiHFPC50A

ABSOLUTE MAXIMUM RATINGS (T _C	·		SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	600	
Gate-Source Voltage			V _{GS}	± 30	V
Outline - Paris Outline	V -140V	T _C = 25 °C		11	
Continuous Drain Current	V _{GS} at 10 V	T _C = 100 °C	I _D	7.0	Α
Pulsed Drain Current ^a			I _{DM}	44	
Linear Derating Factor				1.4	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	920	mJ
Repetitive Avalanche Current ^a			I _{AR}	11	А
Repetitive Avalanche Energy ^a			E _{AR}	18	mJ
Maximum Power Dissipation	T _C =	25 °C	P_{D}	180	W
Peak Diode Recovery dV/dtc			dV/dt	4.9	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) for 10 s				300 ^d	
Marathar Tarra			10	lbf ⋅ in	
Mounting Torque	6-32 or M3 screw			1.1	N·m

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Starting T_J = 25 °C, L = 15 mH, R_g = 25 Ω , I_{AS} = 11 A (see fig. 12).
- c. $I_{SD} \le 11$ Å, $dI/dt \le 126$ A/µs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.
- d. 1.6 mm from case.

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply

IRFPC50A, SiHFPC50A

Vishay Siliconix



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	40	
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.24	-	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.65	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS}	$= 0 \text{ V}, I_D = 250 \mu\text{A}$	600	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I _D = 1 mA	ı	0.65	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V _{DS} :	$= V_{GS}, I_D = 250 \mu A$	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}		$V_{GS} = \pm 30 \text{ V}$	1	-	± 100	nA
Zero Gate Voltage Drain Current		V _{DS} :	= 600 V, V _{GS} = 0 V	ı	-	25	μA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 480 \text{ V}$	V, V _{GS} = 0 V, T _J = 125 °C	-	-	250	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	$I_D = 6.0 \text{ A}^b$	ı	-	0.58	Ω
Forward Transconductance	9fs	V _{DS}	$= 50 \text{ V}, I_D = 6.0 \text{ A}^b$	7.7	-	-	S
Dynamic							
Input Capacitance	C _{iss}		$V_{GS} = 0 V$,	-	2100	-	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ f = 1.0 MHz, see fig. 5		-	270	-	
Reverse Transfer Capacitance	C _{rss}			-	9.7	-	
Output Conscitones	6		V _{DS} = 1.0 V, f = 1.0 MHz	-	2830	-	pF
Output Capacitance	C _{oss}		V _{DS} = 480 V, f = 1.0 MHz	-	74	-	
Effective Output Capacitance	C _{oss} eff.	V _{DS} = 0 V to 480 V ^c		-	81	-	
Total Gate Charge	Q_g			1	-	70	
Gate-Source Charge	Q_{gs}	V _{GS} = 10 V		-	-	19	nC
Gate-Drain Charge	Q_{gd}		and high a dimension	ı	-	28	1
Turn-On Delay Time	$t_{d(on)}$			ı	15	-	
Rise Time	t _r	V _{DD} = 300 V, I _D = 11 A		ı	40	-	ns
Turn-Off Delay Time	$t_{d(off)}$	R _g =	= 6.2 Ω , R _D = 30 Ω see fig. 10 ^b	ı	33	-	115
Fall Time	t _f		g	ı	29	-	
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	11	_
Pulsed Diode Forward Current ^a	I _{SM}			-	-	44	A
Body Diode Voltage	V _{SD}	T _J = 25 °C	C, I _S = 11 A, V _{GS} = 0 V ^b	-	-	1.4	V
Body Diode Reverse Recovery Time	t _{rr}	Т	= 25 °C. Ic = 11 A	-	500	740	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 11 \text{A},$ $dI/dt = 100 \text{A/µs}^{\text{b}}$		-	4.0	6.0	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)			Γυ) 		

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300~\mu s;$ duty cycle $\leq 2~\%.$
- c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

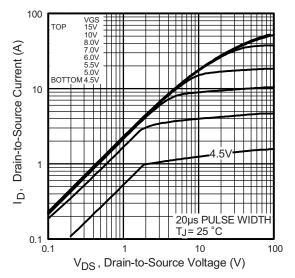


Fig. 1 - Typical Output Characteristics

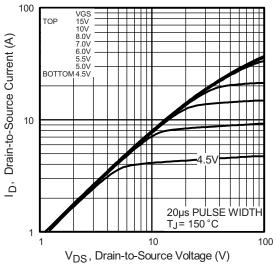


Fig. 2 - Typical Output Characteristics

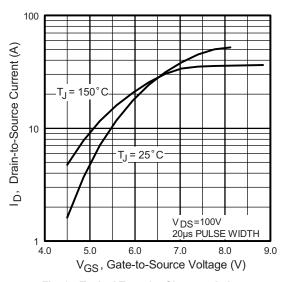


Fig. 3 - Typical Transfer Characteristics

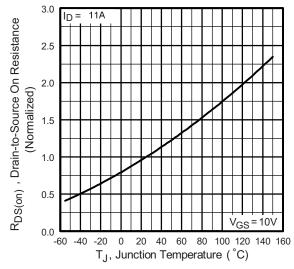


Fig. 4 - Normalized On-Resistance vs. Temperature

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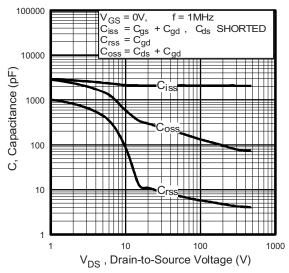


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

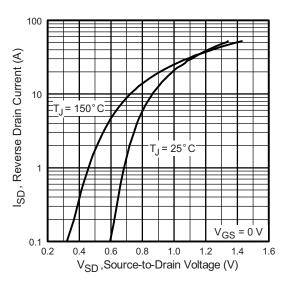


Fig. 7 - Typical Source-Drain Diode Forward Voltage

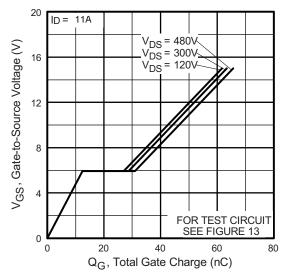


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

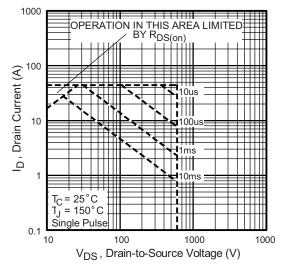


Fig. 8 - Maximum Safe Operating Area





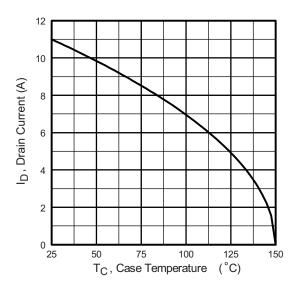


Fig. 9 - Maximum Drain Current vs. Case Temperature

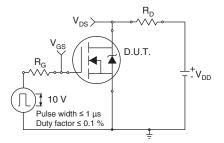


Fig. 10a - Switching Time Test Circuit

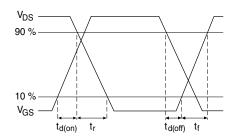


Fig. 10b - Switching Time Waveforms

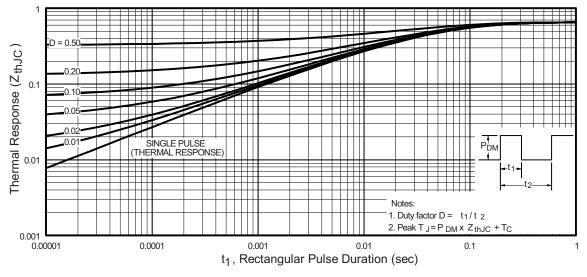


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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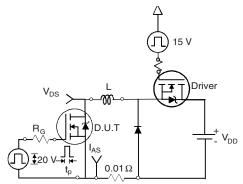


Fig. 12a - Unclamped Inductive Test Circuit

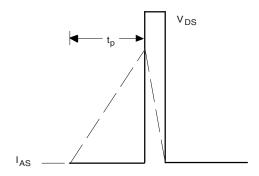


Fig. 12b - Unclamped Inductive Waveforms

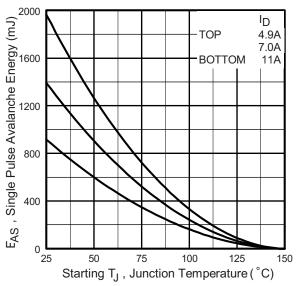


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

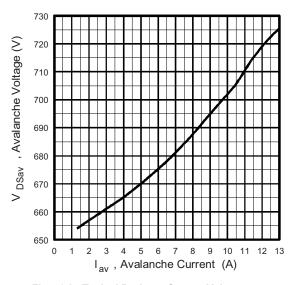


Fig. 12d - Typical Drain-to-Source Voltage vs.
Avalanche Current

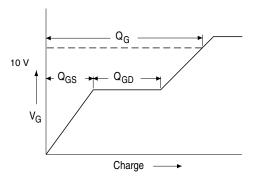


Fig. 13a - Basic Gate Charge Waveform

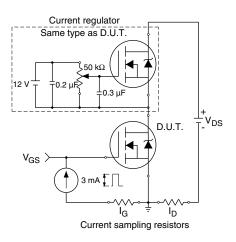
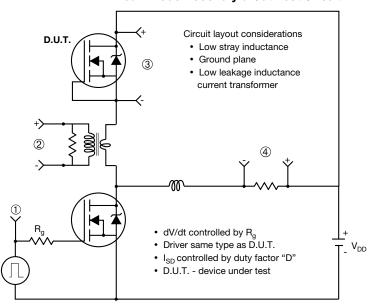


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



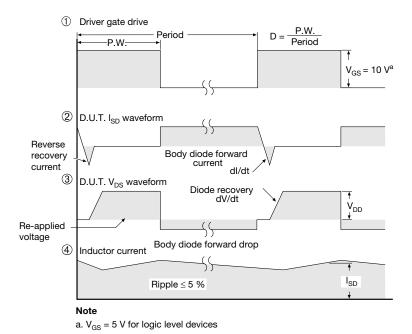


Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91241.



TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9







Section C--C,D--D,E--E

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
Α	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
С	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
е	5.44	BSC	
L	14.90	15.40	
L1	3.96	4.16	6
ØΡ	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	

Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

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VERSION 2: FACILITY CODE = Y



	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
Α	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
С	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

	MILLIN		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.254		
L	14.20	16.25	
L1	3.71	4.29	
ØР	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c

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VERSION 3: FACILITY CODE = N



	MILLIMETERS		
DIM.	MIN.	MAX.	
Α	4.65	5.31	
A1	2.21	2.59	
A2	1.17	1.37	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.65	2.39	
b3	1.65	2.34	
b4	2.59	3.43	
b5	2.59	3.38	
С	0.38	0.89	
c1	0.38	0.84	
D	19.71	20.70	
D1	13.08	-	

	MILLIMETERS		
DIM.	MIN.	MAX.	
D2	0.51	1.35	
E	15.29	15.87	
E1	13.46	-	
е	5.46	BSC	
k	0.254		
L	14.20	16.10	
L1	3.71	4.29	
N	7.62	BSC	
Р	3.56	3.66	
P1	=	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

ECN: E20-0545-Rev. F, 19-Oct-2020

DWG: 5971

Notes

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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