



N-Channel Reduced Q_g, Fast Switching MOSFET

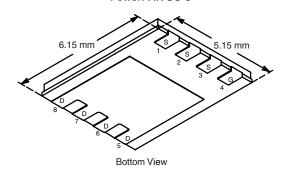
PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$ $I_D(A)$			
30	0.0095 at V _{GS} = 10 V	16		
	0.0125 at V _{GS} = 4.5 V	16		

FEATURES

- Halogen-free According to IEC 61249-2-21 **Available**
- TrenchFET® Power MOSFET
- PWM Optimized for High Efficiency
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 % R_g Tested



PowerPAK SO-8

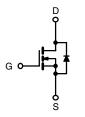


Ordering Information: Si7860ADP-T1-E3 (Lead (Pb)-free)

Si7860ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- **Buck Converter**
 - High Side or Low Side
- Synchronous Rectifier
 - Secondary Rectifier



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	$T_A = 25 ^{\circ}C$, unle	ss otherwise r	noted		
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		V
Continuous Drain Current (T _{.I} = 150 °C) ^a	T _A = 25 °C	I _D	16	11	
Continuous Drain Current (1, = 150 °C)	T _A = 70 °C		13	8	
Pulsed Drain Current		I _{DM}	± 50		Α
Continuous Source Current (Diode Conduction) ^a		I _S	4.1	1.5	
Avalanche Current	L = 0.1 mH	I _{AS}	35 60		
Single Pulse Avalanche Energy	L = 0.111111	E _{AS}			mJ
Marian Para Dissipation	T _A = 25 °C	P _D	4.8	1.8	W
Maximum Power Dissipation ^a	T _A = 70 °C		3.1	1.1	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Manifestor Investigation to Ambient (MOCETT)	t ≤ 10 s	R _{thJA}	21	26	°C/W
Maximum Junction-to-Ambient (MOSFET) ^a	Steady State		56	70	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.9	2.5	

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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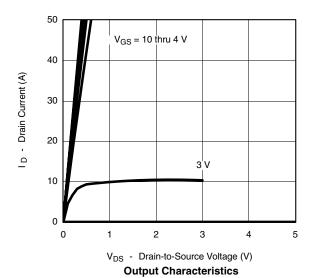
MOSFET SPECIFICATIONS T _J = 25 °C, unless otherwise noted									
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit			
Static									
Gate Threshold Voltage	V _{GS(th)}	$V_{GS(th)}$ $V_{DS} = V_{GS}$, $I_D = 250 \mu A$			3.0	V			
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA			
Zoro Cata Voltago Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	- μΑ			
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			5				
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α			
	B	$V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}$		0.0079	0.0095	Ω			
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 14 \text{ A}$		0.0105	0.0125	22			
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 16 A		60		S			
Diode Forward Voltage ^a	V_{SD}	I _S = 3 A, V _{GS} = 0 V		0.70	1.1	V			
Dynamic ^b			•	"					
Total Gate Charge	Q_g			13	18				
Gate-Source Charge	Q_{gs}	Q_{gs} $V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 16 \text{ A}$		5		nC			
Gate-Drain Charge	Q_{gd}			4.0		<u> </u>			
Gate Resistance	R_g		0.5	1.7	3.2	Ω			
Turn-On Delay Time	t _{d(on)}			18	27				
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		12	18				
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		46	70	ns			
Fall Time	t _f			19	30				
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 3 A, dI/dt = 100 A/μs		40	70				

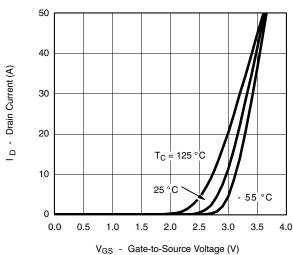
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





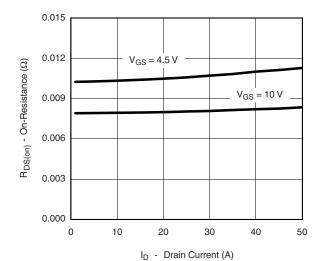
Transfer Characteristics



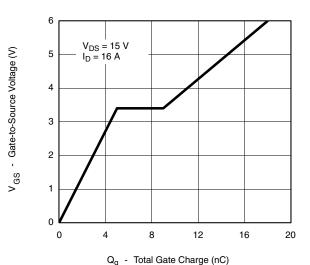




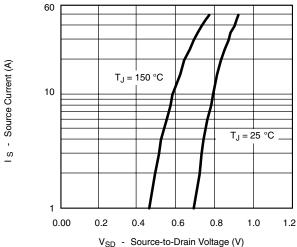
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



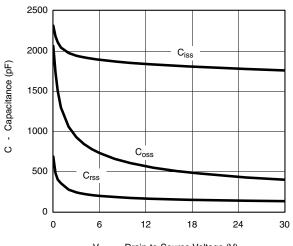
On-Resistance vs. Drain Current



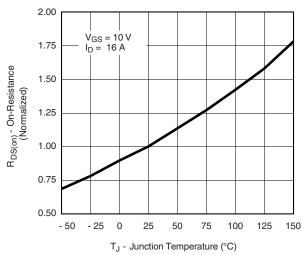
Gate Charge



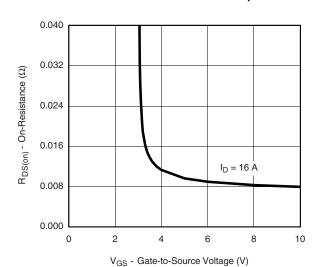
Source-Drain Diode Forward Voltage



V_{DS} - Drain-to-Source Voltage (V) **Capacitance**



On-Resistance vs. Junction Temperature

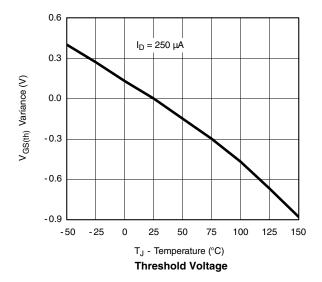


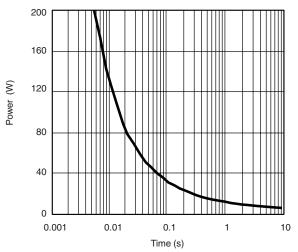
On-Resistance vs. Gate-to-Source Voltage

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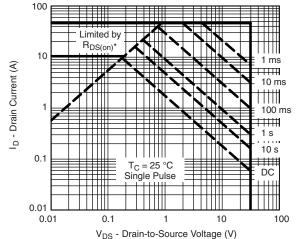
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



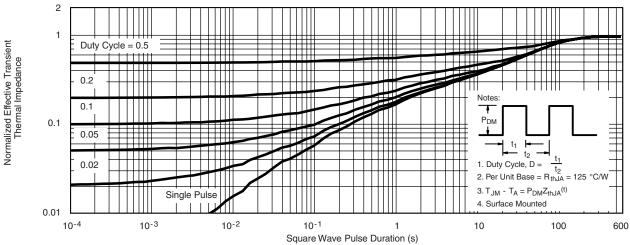


Single Pulse Power, Junction-to-Ambient



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

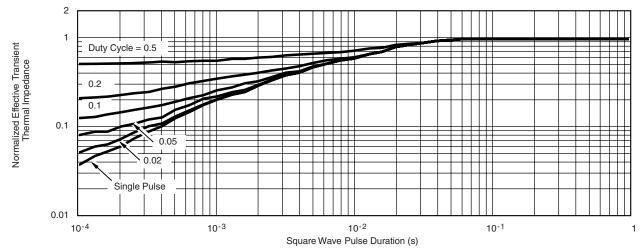
Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

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