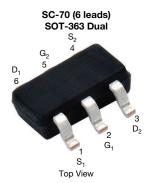


Vishay Siliconix

Dual N-Channel 20 V (D-S) MOSFET



Marking code: PE

PRODUCT SUMMARY				
V _{DS} (V)	20			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.235			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5 \text{ V}$	0.306			
Q _g typ. (nC)	0.9			
I _D (A) ^a	1.1			
Configuration	Dual			

FEATURES

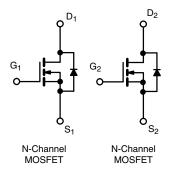
- TrenchFET® power MOSFET
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Load switch and DC/DC converter for portable devices
- · High speed switching



ORDERING INFORMATION	
Package	SC-70
Lead (Pb)-free and halogen-free	Si1902CDL-T1-GE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	20	V	
Gate-source voltage		V _{GS}	± 12	V	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		1.1		
	T _C = 70 °C	1 ,	0.9		
	T _A = 25 °C	I _D	1 b, c		
	T _A = 70 °C		0.8 b, c	A	
Pulsed drain current (t = 300 μs)		I _{DM}	2	7	
Continuous source-drain diode current	T _C = 25 °C		0.35		
	T _A = 25 °C	ls ===	0.25 b, c		
Maximum power dissipation	T _C = 25 °C		0.42		
	T _C = 70 °C		0.27	14/	
	T _A = 25 °C	P _D	0.30 b, c	W	
	T _A = 70 °C		0.23 b, c		
Operating junction and storage temperature ra	inge	T _J , T _{stq}	-55 to +150	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient b, d	t ≤ 5 s	R _{thJA}	290	350	°C/W	
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	250	300		

Notes

- a. Based on T_C = 25 °C
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 5 s
- d. Maximum under steady state conditions is 410 $^{\circ}\text{C/W}$



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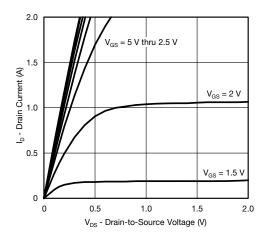
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static					•		
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	J 050 ·· A	-	25	-	mV/°C	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-2.6	-		
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.6	-	1.5	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	-	-	± 100	nA	
Zana mata walta na aluaina awanant		V _{DS} = 20 V, V _{GS} = 0 V	-	-	1	μА	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V, T _J = 85 °C	-	-	10		
On-state drain current a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	2	-	-	Α	
Drain-source on-state resistance a	_	$V_{GS} = 4.5 \text{ V}, I_D = 1 \text{ A}$	-	0.195	0.235		
	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, I_D = 0.3 \text{ A}$	-	0.255	0.306	Ω	
Forward transconductance	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ A}$	-	3	-	ms	
Dynamic ^b							
Input capacitance	C _{iss}		-	62	-	pF	
Output capacitance	C _{oss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	20	-		
Reverse transfer capacitance	C _{rss}		-	7	-		
Total colonia de co	0	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 1 \text{ A}$	-	2	3		
Total gate charge	Q_g		-	0.9	1.4	nC	
Gate-source charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 1 \text{ A}$	-	0.2	-		
Gate-drain charge	Q _{gd}		-	0.2	-		
Gate resistance	R_g	f = 1 MHz	2.4	12	24	Ω	
Turn-on delay time	t _{d(on)}		-	4	8		
Rise time	t _r	$V_{DD} = 10 \text{ V}, R_1 = 12.5 \Omega$	-	13	20	- - -	
Turn-off delay time	t _{d(off)}	$I_D \cong 0.8 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	11	20		
Fall time	t _f		-	9	18		
Turn-on delay time	t _{d(on)}		-	6	12		
Rise time	t _r	$V_{DD} = 10 \text{ V}, R_{I} = 12.5 \Omega$	-	16	24	ns	
Turn-off delay time	t _{d(off)}	$I_D \cong 0.8 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	13	20		
Fall time	t _f		-	10	20		
Drain-Source Body Diode Characterist	ics		1		•	I	
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	0.35	_	
Pulse diode forward current ^a	I _{SM}	-		-	2	A	
Body diode voltage	V _{SD}	I _S = 0.8 A	-	0.8	1.2	V	
Body diode reverse recovery time	t _{rr}		-	2	4	nC	
Body diode reverse recovery charge	Q _{rr}		-	8	16		
Reverse recovery fall time	t _a	$I_F = 0.8 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	-	5	-	ns	
Reverse recovery rise time	t _b		-	3	_		

Notes

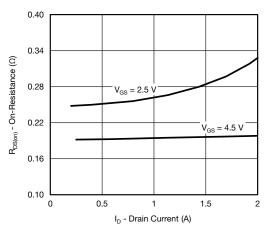
- a. Pulse test; pulse width $\leq 300~\mu s,\,duty~cycle \leq 2\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

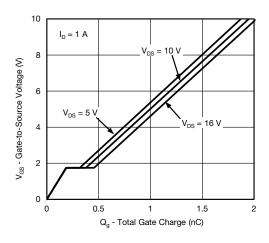




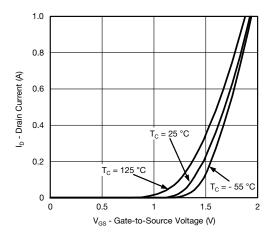
Output Characteristics



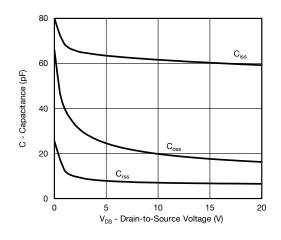
On-Resistance vs. Drain Current and Gate Voltage



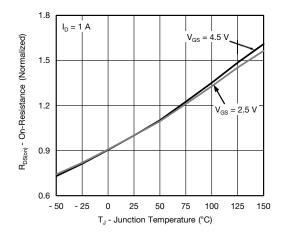
Gate Charge



Transfer Characteristics

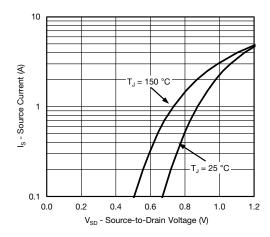


Capacitance

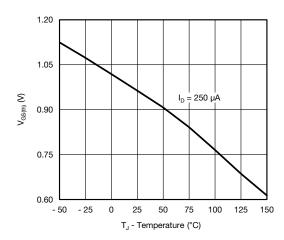


On-Resistance vs. Junction Temperature

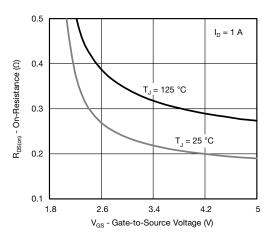




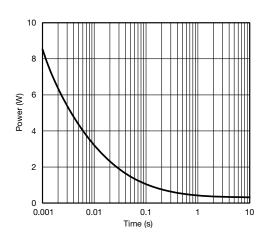
Source-Drain Diode Forward Voltage



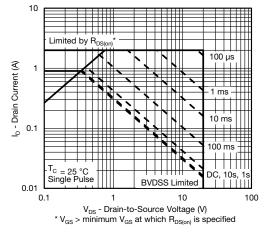
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

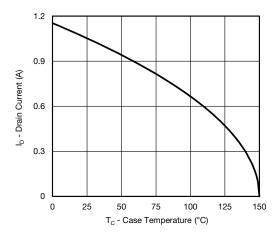


Single Pulse Power (Junction-to-Ambient)

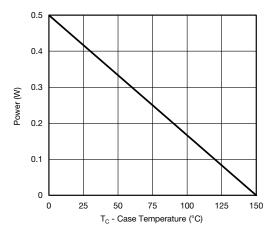


Safe Operating Area, Junction-to-Ambient

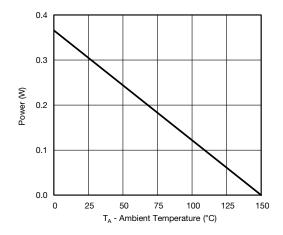




Current Derating a



Power Derating, Junction-to-Foot

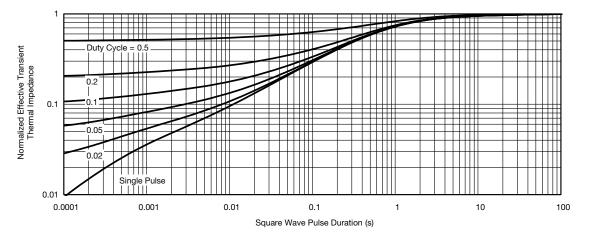


Power Derating, Junction-to-Ambient

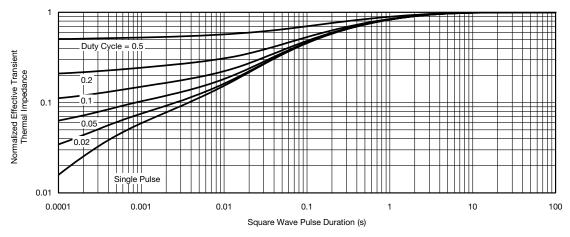
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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