High-Speed Quad CMOS Analog Switch

Features

- Fast Switching Action—t_{ON}: 30 ns
- Low On-Resistance—$r_{DS(on)}$: 20 Ω
- Single-Supply Operation
- Low Charge Injection
- TTL and CMOS Logic Compatible

Benefits

- Improved Data Throughput
- Reduced Switching Errors
- Simplified Power Supply
- Reduced Switching Transients
- Simplified Interfacing
- High Reliability

Applications

- Hard Disk Drives
- Fast Sample-and-Hold Circuits
- Precision Instrumentation
- Computer Peripherals
- Low Noise Op Amp Gain Switching
- High-Rel Systems

Description

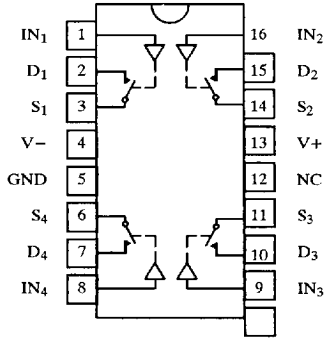
The DG601 is a high performance quad SPST CMOS analog switch intended for applications where fast switching, low charge injection and low on-resistance are required. The DG601 features single-supply operation, and is TTL-compatible with either a single 12-V supply, a single 5-V supply, or with ±5-V supplies.

Applications for the DG601 include 12-V systems requiring TTL or 5-V logic levels, such as disk drives and other computer peripherals. The fast switching time and low charge injection make the DG601 ideal for high speed data acquisition applications such as sample and hold amplifiers, channel selection and gain ranging.

The DG601 is built on the Siliconix proprietary PolyMOS process, allowing low parasitic capacitance to facilitate high speed switching.

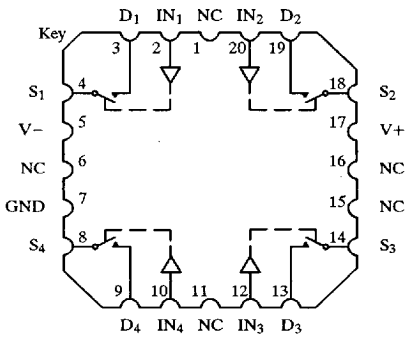
Functional Block Diagram and Pin Configuration

Dual-In-Line and SOIC



Top View

LCC



Top View

Ordering Information

Temp Range	Package	Part Number
40 to 85°C	16-Pin Plastic DIP	DG601DJ
	16-Pin Narrow SOIC	DG601DY
−55 to 125°C	16-Pin CerDIP	DG601AK
		DG601AK/883
	LCC-20	DG601AZ/883

Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V
Switches Shown for Logic "1" Input

Absolute Maximum Ratings

Voltages Referenced to V−
V+ ..... 22 V
GND ..... 13 V
Digital Inputs[a], V_S, V_D ..... (V−) −2 V to (V+) plus 2 V or 30 mA, whichever occurs first
Current (any terminal) ..... 30 mA
Current S or D (Pulsed 1 ms at 10% duty cycle) ..... 100 mA
Storage Temperature (AK, AZ Suffixes) ..... −65 to 150°C
(DJ, DY Suffixes) ..... −65 to 125°C
Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin SOIC[d] ..... 900 mW
16-Pin CerDIP[e] ..... 900 mW
LCC-20[e] ..... 1200 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 25°C
d. Derate 7.7 mW/°C above 25°C
e. Derate 12 mW/°C above 75°C

Specifications[a] for Single 12-V Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 10.8 V, I_S = 10 mA, V_D = 2 V, 10 V	Room Full	20		35 50			Ω
On-Resistance Matching[g]	$\Delta r_{DS(on)}$		Room Full	2.2		6 10		6 10	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 13.2 V, V− = 0 V, V_D = 12.2 V, 1 V, V_S = 1 V, 12.2 V	Room Full	±0.01	−4 −100	4 100	−4 −100	4 100	nA
	$I_{D(off)}$		Room Full	±0.01	−4 −100	4 100	−4 −100	4 100	
Channel On Leakage Current	$I_{D(on)}$	V+ = 13.2 V, V− = 0 V, V_S, V_D = 1 V, 12.2 V	Room Full	±0.1	−4 −200	4 200	−4 −200	4 200	
Digital Control									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0 V	Full	-10^{-5}	−10		−10		µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 5 V	Full	10^{-5}		10		10	
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF, See Figure 2	Room	30		45		45	ns
Turn-Off Time	t_{OFF}		Room	14		30		30	
Charge Injection	Q	C_L = 1,000 pF, V_{gen} = 6 V, R_{gen} = 0 Ω, See Figure 3	Room	13					pC
Off Isolation Reject Ratio	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	69					dB
Crosstalk	X_{TALK}		Room	88					
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 6 V	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	20					
Power Supplies									
Positive Supply Current	I+	V+ = 13.2 V, V− = 0 V, V_{IN} = 0 V or 5 V	Room Full	2.2		4 6		4 6	mA
Negative Supply Current	I−		Room Full	−2.1	−4 −6		−4 −6		

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Specifications[a] for Dual Supplies

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−5	5	−5	5	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 4.5 V, V− = −4.5 V I_S = −10 mA, V_D = ±3.5 V	Room Full	27		40 60		40 60	Ω
On-Resistance Matching[g]	$\Delta r_{DS(on)}$		Room Full	2		6 10		6 10	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 5.5 V, V− = −5.5 V V_D = ∓4.5 V, V_S = ±4.5 V	Room	0.01					nA
	$I_{D(off)}$		Room	0.01					
Channel On Leakage Current	$I_{D(on)}$	V+ = 5.5 V, V− = 5.5 V V_S = V_D = ±4.5 V	Room	0.1					
Digital Control									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0 V All Other = 5 V	Room	−10					pA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 5 V All Other = 0 V	Room	10					
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 2	Room	34					ns
Turn-Off Time	t_{OFF}		Room	20					
Charge Injection	Q	V_{gen} = 0 V, R_{gen} = 0 Ω C_L = 1 nF, See Figure 3	Room	11					pC
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	21					
Power Supplies									
Positive Supply Current	I+	V+ = 5.5 V, V− = −5.5 V V_{IN} = 0 V or 5 V	Room	1.8					mA
Negative Supply Current	I−		Room	−1.8					

Specifications[a] for Single 5-V Supply

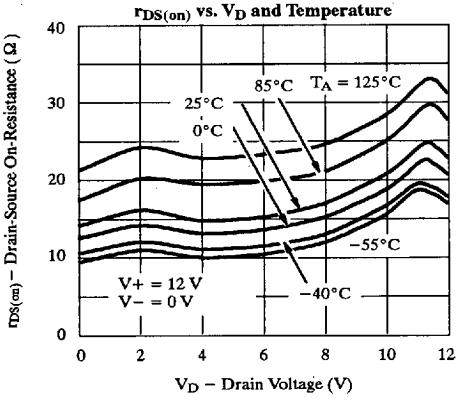
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = 0 V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	5	0	5	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 4.5 V, I_S = −10 mA V_D = 2 V, 3.5 V	Room Full	50		100 140		100 140	Ω
On-Resistance Matching[g]	$\Delta r_{DS(on)}$		Room Full	2		10 15		10 15	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 5.5 V V_D = 1 V, V_S = 4.5 V	Room	±0.01					nA
	$I_{D(off)}$	V+ = 5.5 V V_D = 4.5 V, V_S = 1 V	Room	±0.01					
Channel On Leakage Current	$I_{D(on)}$	V+ = 5.5 V V_S = V_D = 4.5 V, 1 V	Room	±0.1					

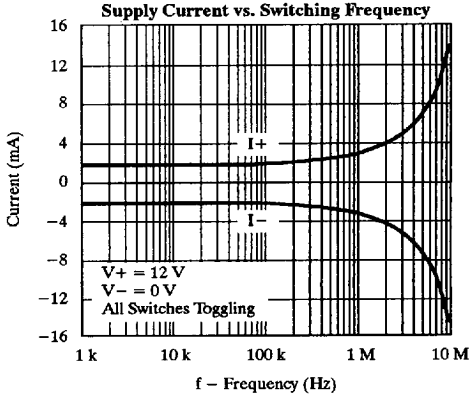
Specifications[a] for Single 5-V Supply (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Digital Control									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0 V	Room	−10					pA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 5 V	Room	10					
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 2	Room	32					ns
Turn-Off Time	t_{OFF}		Room	25					
Charge Injection	Q	V_{gen} = 2.5 V, R_{gen} = 0 Ω, C_L = 1 nF, See Figure 3	Room	6					pC
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 2.5 V	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	22					
Power Supplies									
Positive Supply Current	I+	V+ = 5.5 V, V_{IN} = 0 V or 5 V	Room	1.2					mA
Negative Supply Current	I−		Room	−0.8					

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta r_{DS(on)}$ compares on-resistance at the specified V_D values.

Typical Characteristics





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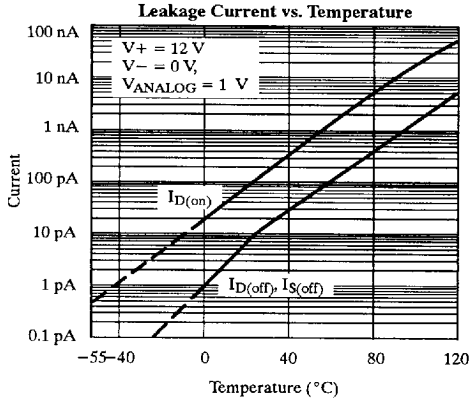

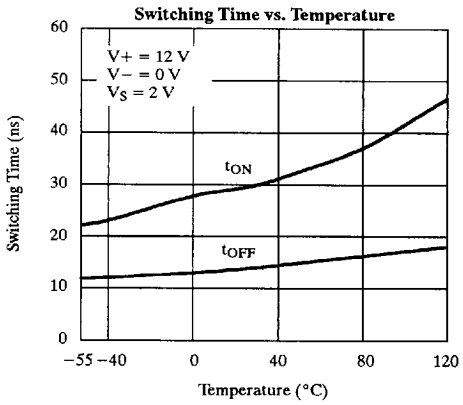

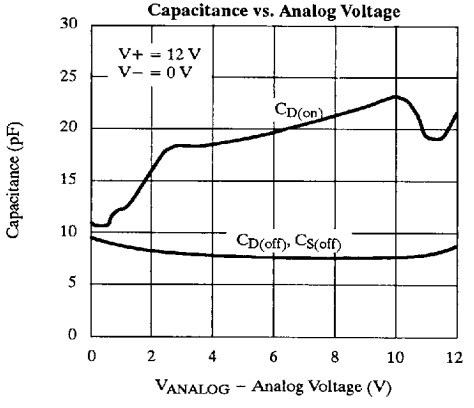

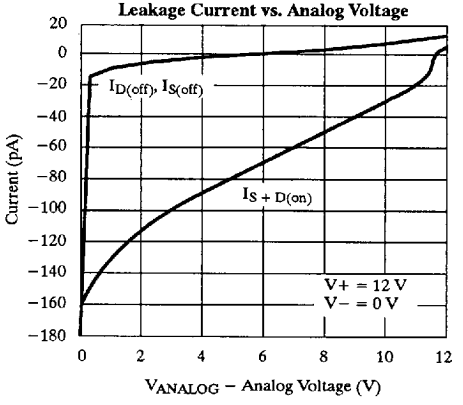

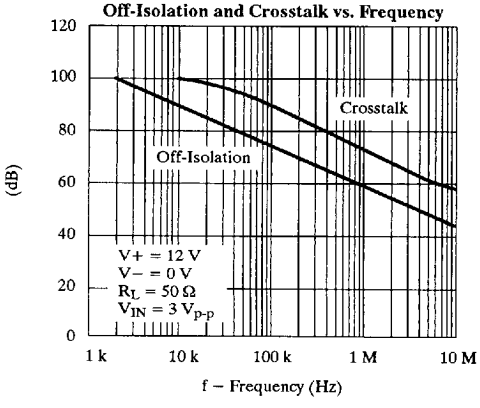

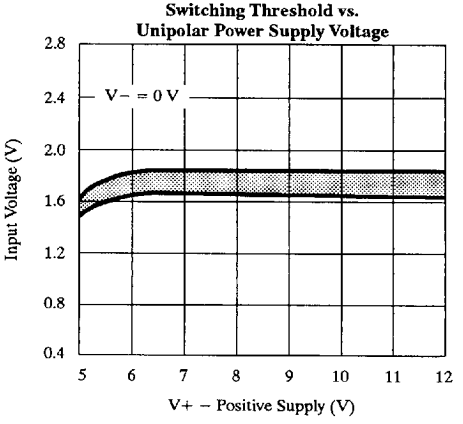

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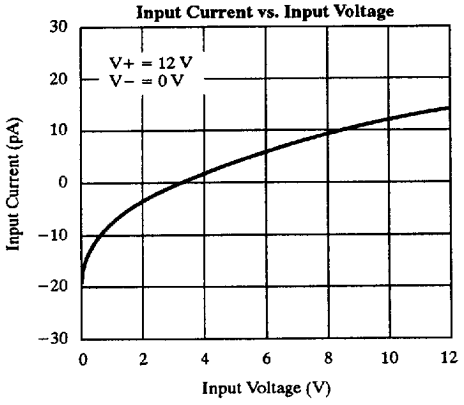
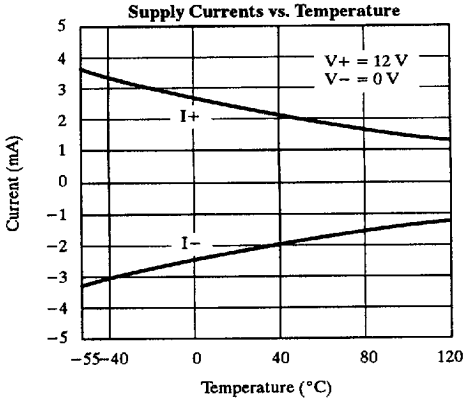
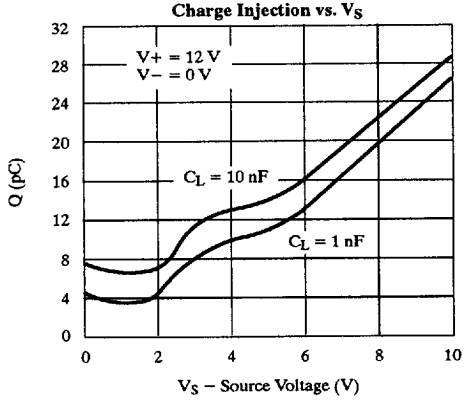
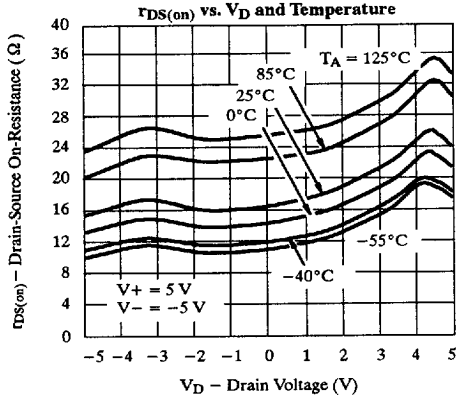
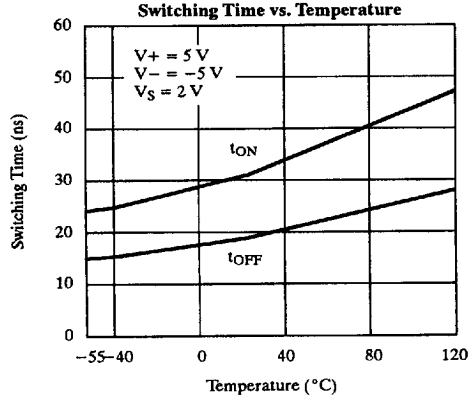
Typical Characteristics (Cont'd)

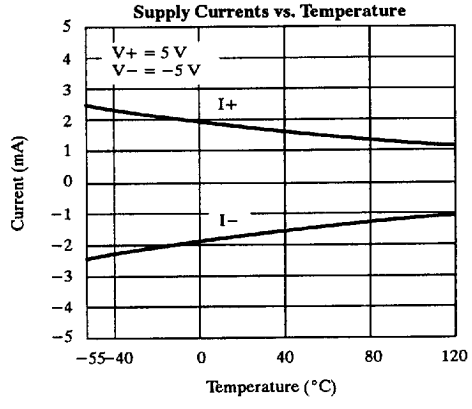












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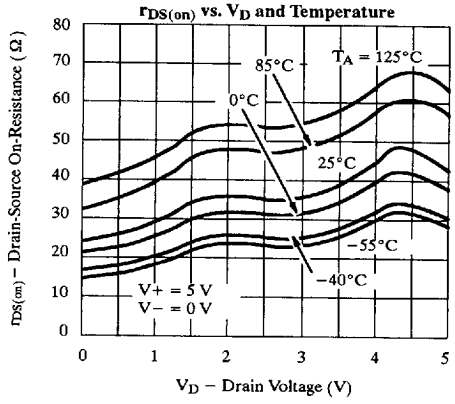
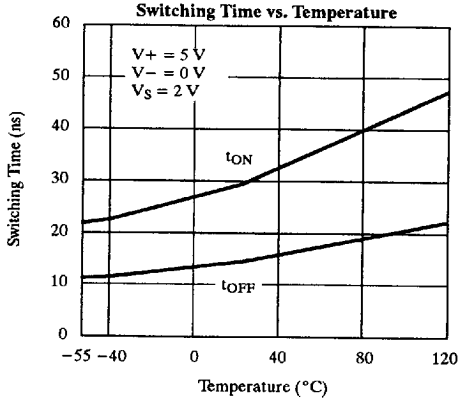
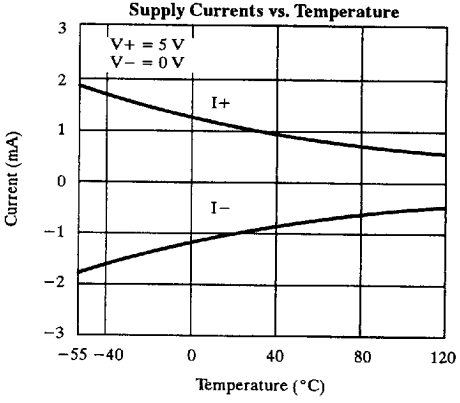
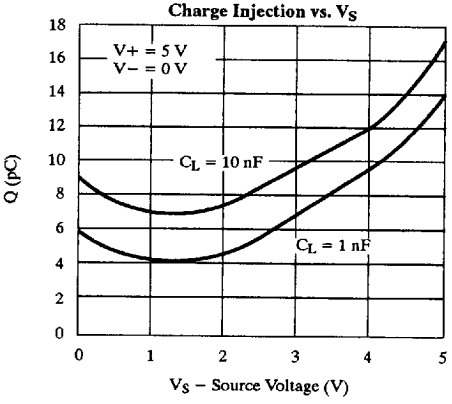








Schematic Diagram (Typical Channel)

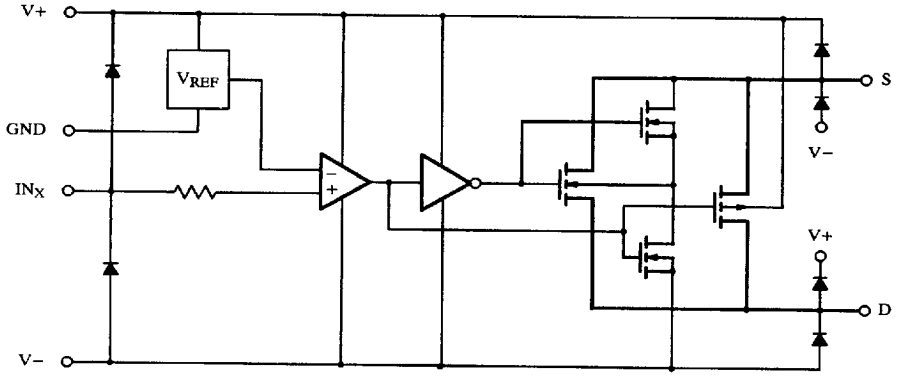
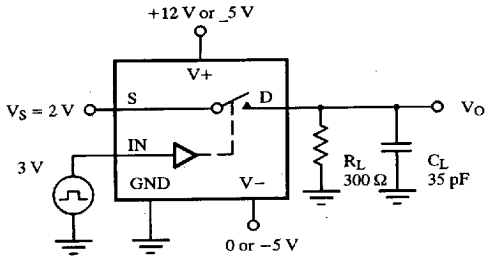
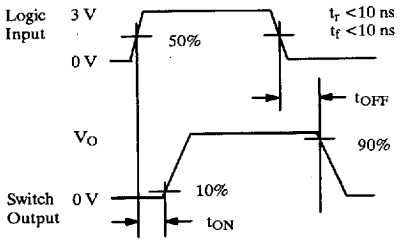


Figure 1

Test Circuits

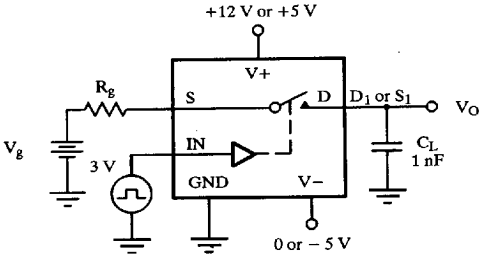




C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2 Switching Time



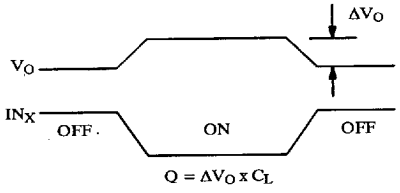
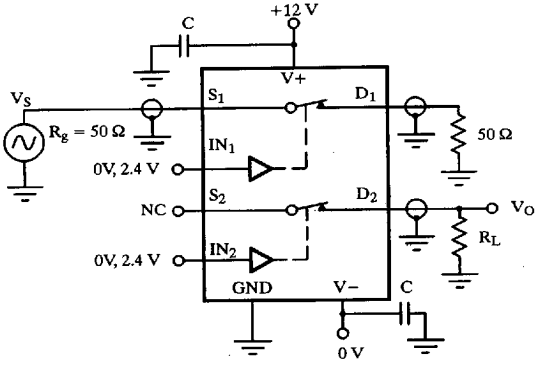


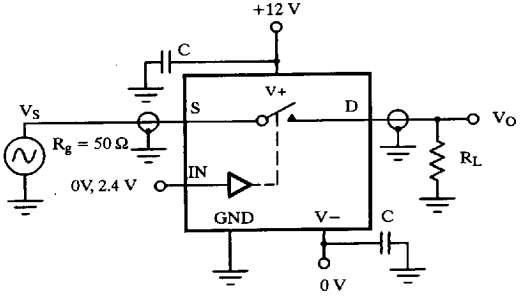
Figure 3 Charge Injection



X_{TALK} Isolation = 20 log $\left|\frac{V_S}{V_O}\right|$

C = RF bypass

Figure 4 Crosstalk



Off Isolation = 20 log $\left|\frac{V_S}{V_O}\right|$

C = RF bypass

Figure 5 Off Isolation

Test Circuits (Cont'd)

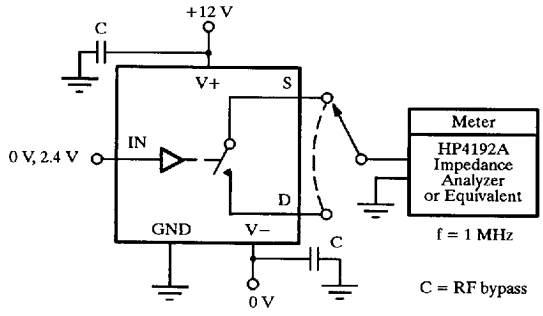


Figure 6 Source/Drain Capacitances

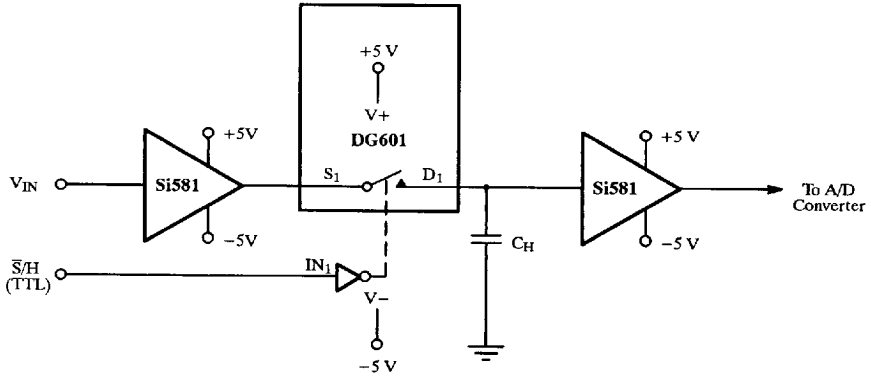


Figure 7 Simple High-Speed Sample-and-Hold Circuit for Data Acquisition System Front Ends

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Applications

Application Examples

Analog switches are found in a variety of applications. The DG601 is useful in applications that require low-supply voltages, high-speed switching, and/or low on-resistance. Computer peripherals, such as disk drives, are an example of single-supply (12-V or 5-V) systems that use analog switches for sampling, signal conditioning, signal routing, and level translation. High-speed data acquisition systems typically use ±5-V supplies for the flash converters, and they require very fast, accurate switches for the input sample-and-hold amplifiers.

Sample-and-Hold Amplifiers

Figure 7 shows a sample-and-hold amplifier that provides a very fast sample acquisition time with the ±5-V power supplies that are required for high-speed A/D converters. The circuit is controlled by the sample-and-hold input, which is a TTL (5-V CMOS) control line. When a logic "0" is applied to the sample-and-hold input, the switch is turned on. A sample of the input signal is acquired by charging up the hold capacitor (C_H) to the value of the input signal. When a logic "1" is applied, the switch is turned off. The value of the input signal at the time the switch is turned off is held in C_H. The sample-and-hold amplifier is designed for the following features:

Sample-and-Hold Amplifiers (Cont'd)

1. ±5-V Operation

   The DG601 and Si581 buffer are both rated for ±5-V operation.

2. Low Pedestal Error

   This is a result of the low charge injection of the DG601. Pedestal error can be reduced even further by using other switches in the quad to cancel out the injected charge (Figure 8).

3. Fast Acquisition Time

   Sample-and-hold amplifiers take advantage of the fast switching time of the DG601 with a (+5-V supply, t_{ON} is typically 50 ns) and the high slew rate (800 V/μs) of the Si581.

   The 20-μA bias current for the Si581 will result in a 20-mV/μs droop rate, which is adequate for 8-bit operation at a 1-MHz sampling rate. Better droop rate can be achieved with a lower input-bias current buffer, such as a FET input device.

4. TTL-Compatible Operation

Precision Signal Routing

The low on-resistance of the DG601 makes it an ideal choice for digitally controlled analog signal conditioning applications, such as channel selection and gain ranging in low-voltage systems. High-voltage switches (like the DG201A) suffer increased on-resistance and logic incompatibility when operated at lower supply voltages like +12 V. The 30-Ω on-resistance of the DG601 helps to maintain low impedance levels and reduce switch resistance-induced offsets and noise.

Level Translation Applications

The DG601 makes an excellent level translator for use with MOSPOWER drivers, relay drivers, JFET drivers, GaAs FET drivers, DMOS drivers, and other circuits that require high-speed 5-V logic compatibility and an output range up to 12 V. Figure 9 shows one-half of a DG601 acting as the interface between the TTL and the Si9950 half-bridge driver. The Si9950 has a 1000-pF input capacitance, which is difficult to drive from a standard logic gate. The DG601 delivers a fast level translation from a TTL signal to provide 12 V of enhancement on the Si9950. A 180-Ω resistor is placed in series with the Si9950 input to limit the current through the DG601 to 100 mA (worst case). This prevents the current from exceeding the absolute maximum current rating. Increased gate drive current can be handled by connecting two sets of switches in parallel.

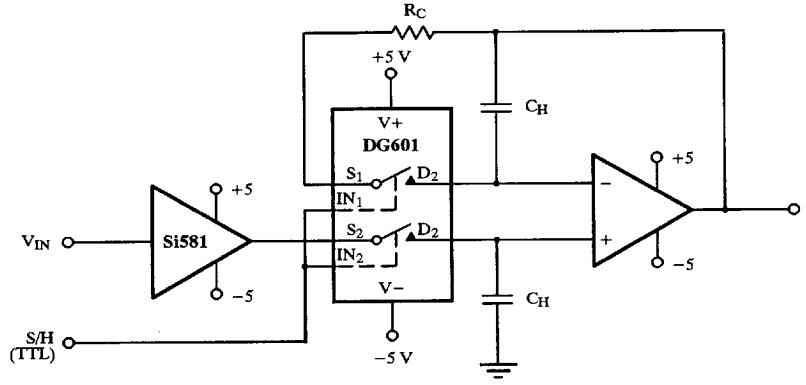

Figure 8 Using On-Board Switches to Cancel Out Charge Ingection

Conclusion

The DG601 has many applications in low-voltage systems, having been designed and specified for 12-V, TTL-compatible operation. It is also excellent in ±5-V and single 5-V supply applications where fast switching speed, low charge injection, and low on-resistance are required. This data sheet highlights some typical applications to assist the design engineer in getting optimum performance in low-voltage mixed analog/digital systems.

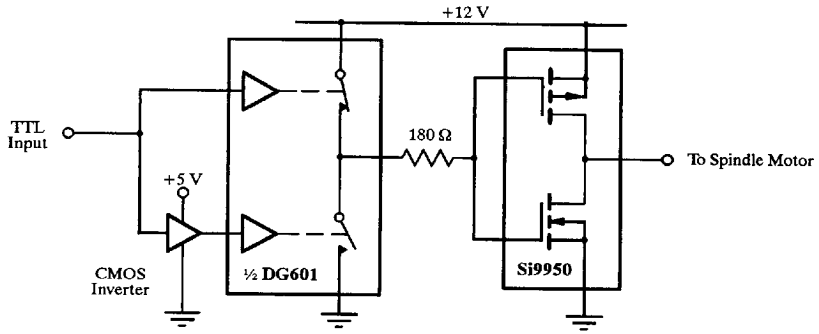

Figure 9 DG601 Provides Level Translation for MOSFET Gate Drive

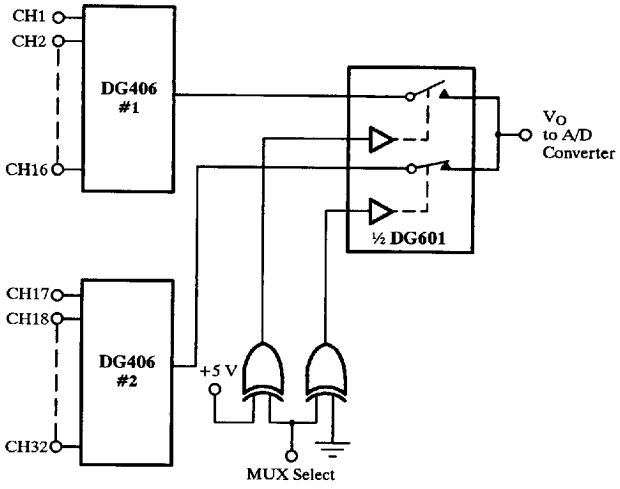

Figure 10 Super Multiplexing Improves Settling Times

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