Low-Voltage, Low R_{ON}, Dual DPDT Analog Switch

DESCRIPTION

The DG3015 is a dual double-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG3015 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG3015 is built on Vishay Siliconix's low voltage JI2 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- Low Voltage Operation (2.7 V to 3.3 V)
- Low On-Resistance - R_{ON}: 0.8 Ω
- 3 dB Loss at 100 MHz
- Fast Switching: t_{ON} = 40 ns, t_{OFF} = 35 ns
- MICRO FOOT® Package
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free
RoHS COMPLIANT

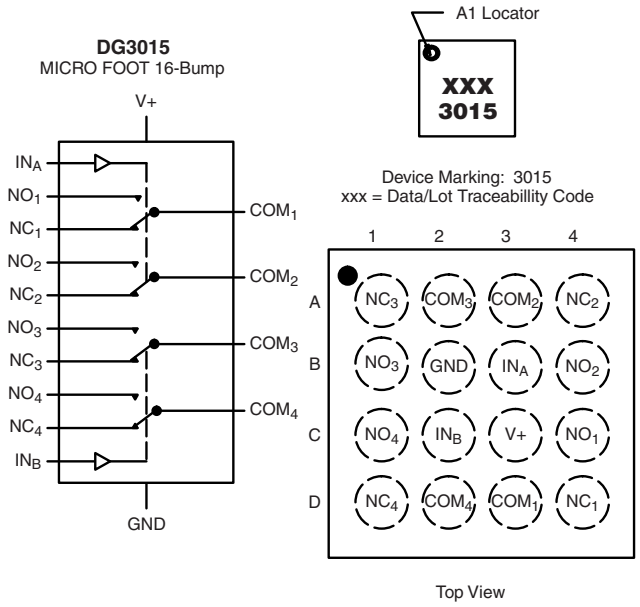
BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- TTL/1.8 V Logic Compatible
- High Bandwidth

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	**NC1, 2, 3 and 4**	**NO1, 2, 3 and 4**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
- 40 °C to 85 °C	MICRO FOOT: 16 Bump (4 x 4, 0.5 mm Pitch, 238 µm Bump Height)	DG3015DB-T2-E1

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ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
Parameter		**Limit**	**Unit**
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3 V)	
Current (Any terminal except NO, NC or COM)		30	mA
Continuous Current (NO, NC or COM)		± 150	
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 250	
Storage Temperature	(D Suffix)	- 65 to 150	°C
Package Solder Reflow Conditions[b]	IR/Convection	250	
Power Dissipation (Packages)[c]	MICRO FOOT: 16 Bump (4 x 4 mm)[d]	719	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. Refer to IPC/JEDEC (J-STD-020B)
c. All bumps welded or soldered to PC Board.
d. Derate 9 mW/°C above 70 °C.

Permanent damage to the device may occur when the "Absolute Maximum Ratings" are exceeded. These stress ratings do not indicate conditions for which the device is intended to be functional. Functionality is only guaranteed to the conditions specified by the parametric table within the document.

SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 2 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.80	1.2 1.3	Ω
R_{ON} Flatness	R_{ON} Flatness	V+ = 2.7 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 100 mA	Room		0.16		
R_{ON} Match	ΔR_{ON}		Room		0.15		
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 1 V/3 V, V_{COM} = 3 V/1 V	Room Full	- 2 - 20		2 20	nA
	$I_{COM(off)}$		Room Full	- 2 - 20		2 20	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V/3 V	Room Full	- 2 - 20		2 20	
Digital Control							
Input High Voltage	V_{INH}		Full	2			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2 V, R_L = 300 Ω, C_L = 35 pF	Room Full		40	65 67	ns
Turn-Off Time	t_{OFF}		Room Full		35	60 62	
Break-Before-Make Time	t_d		Full	1	3		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		7		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 67		dB
Crosstalk[d]	X_{TALK}		Room		- 70		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		63		pF
	$C_{NC(off)}$		Room		67		
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		200		
	$C_{NC(on)}$		Room		196		

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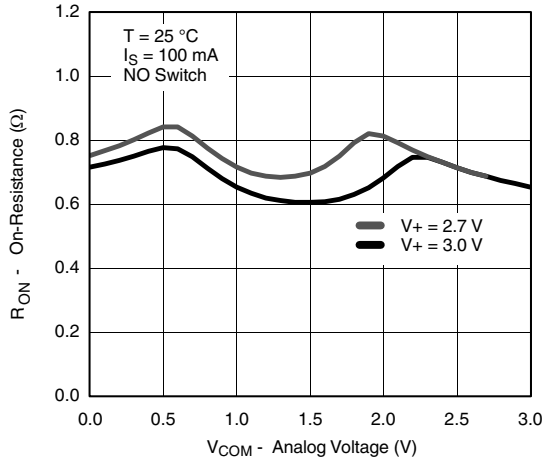
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full			1	µA

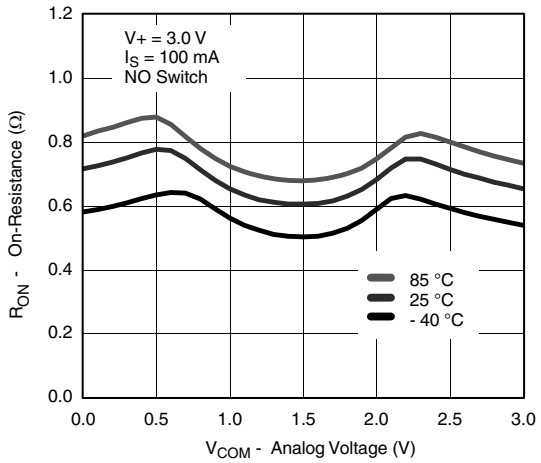
Notes:
a. Room = 25 °C, full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

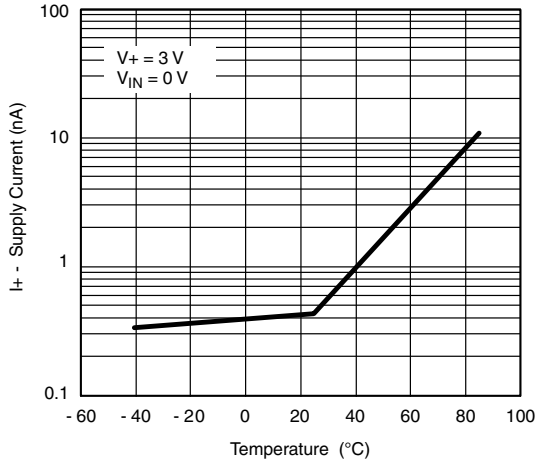
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



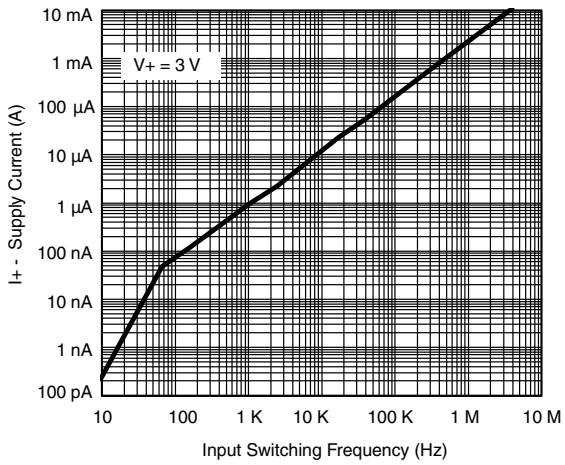
R_{ON} vs. V_{COM} and SIngle Supply Voltage



R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

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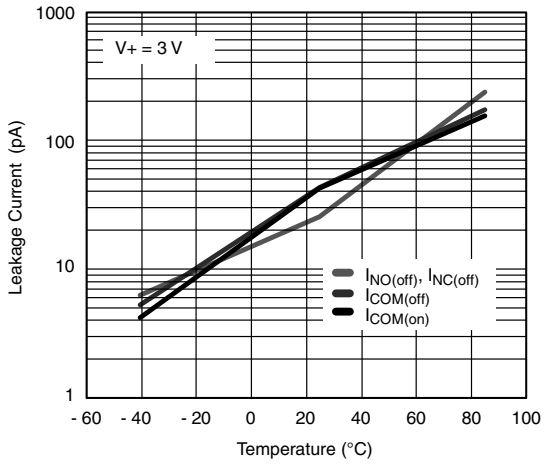
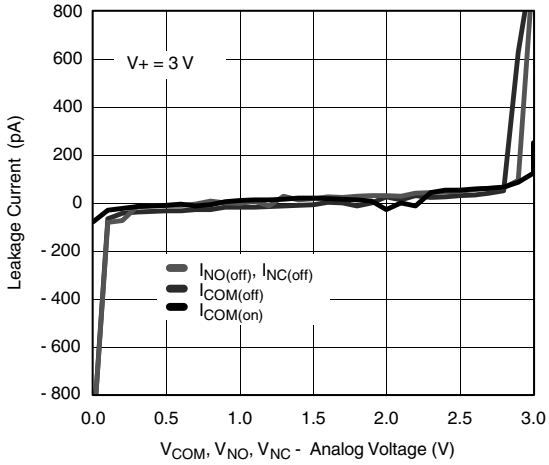
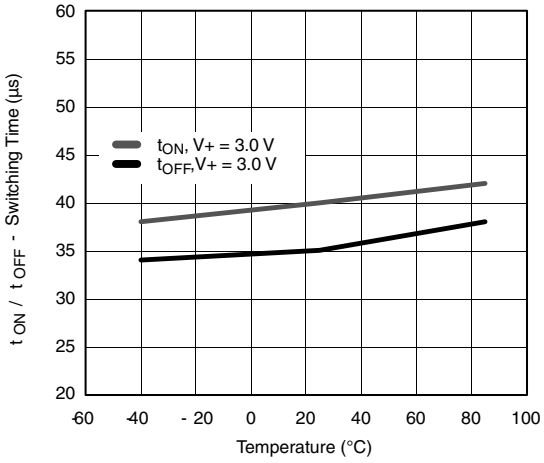
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



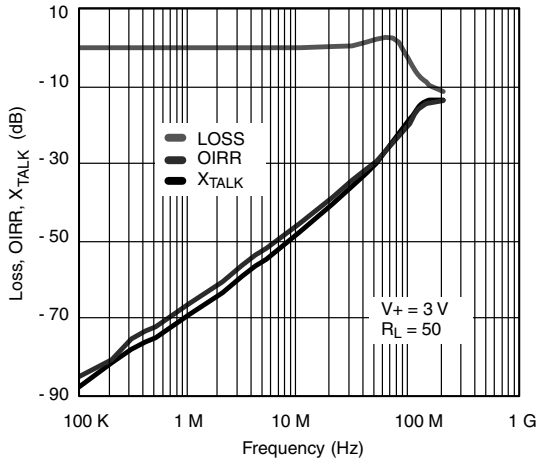
Leakage Current vs. Temperature



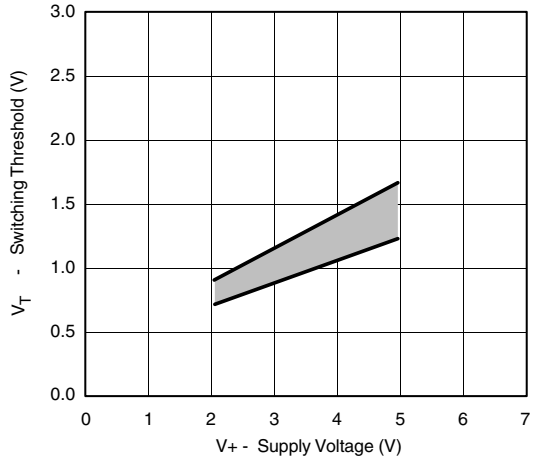
Leakage vs. Analog Voltage



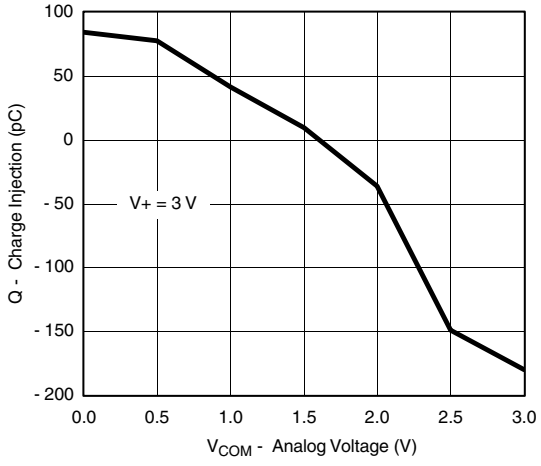
Switching Time vs. Temperature



Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

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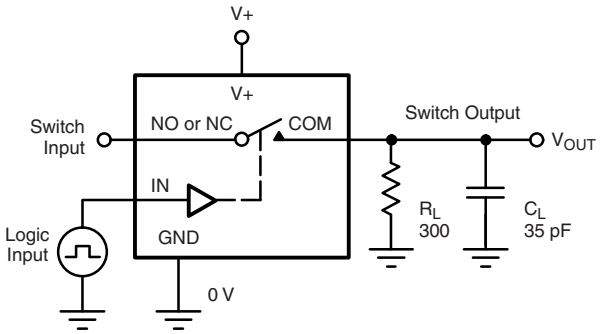
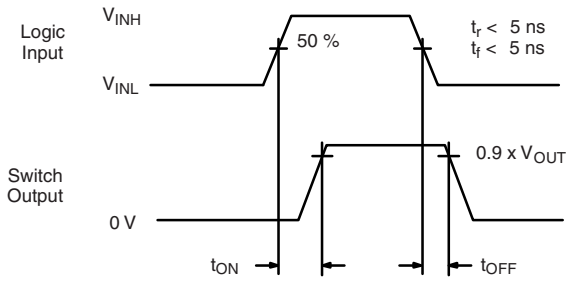
TEST CIRCUITS



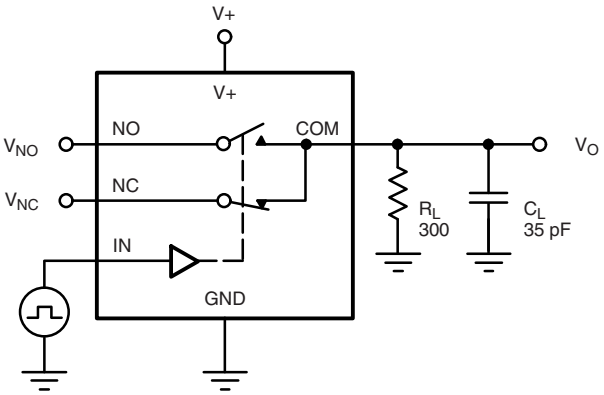
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

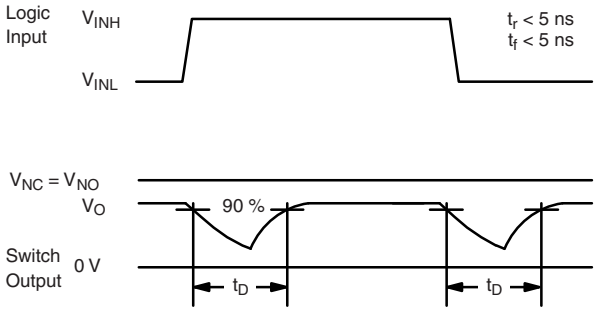
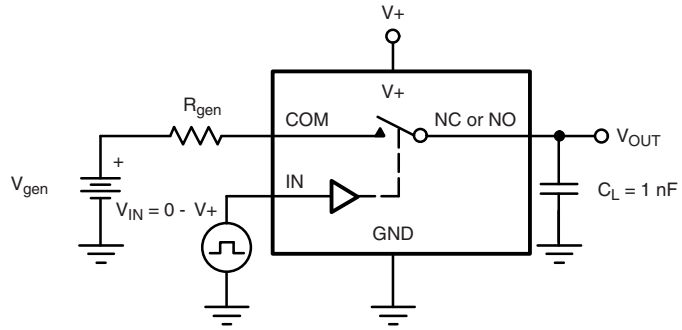
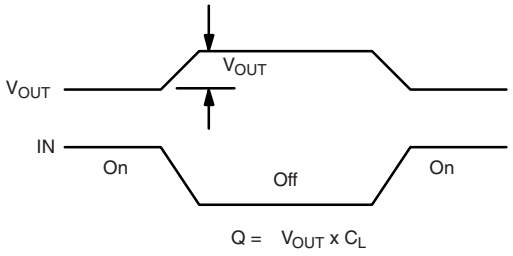


Figure 2. Break-Before-Make Interval





Q = V_{OUT} x C_L

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

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TEST CIRCUITS

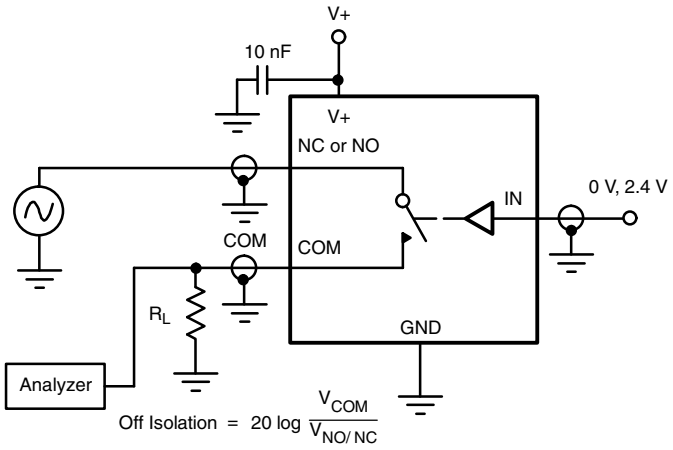

Figure 4. Off-Isolation

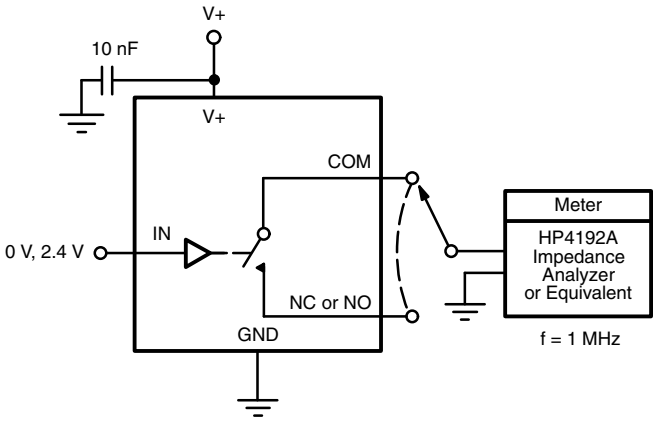

Figure 5. Channel Off/On Capacitance

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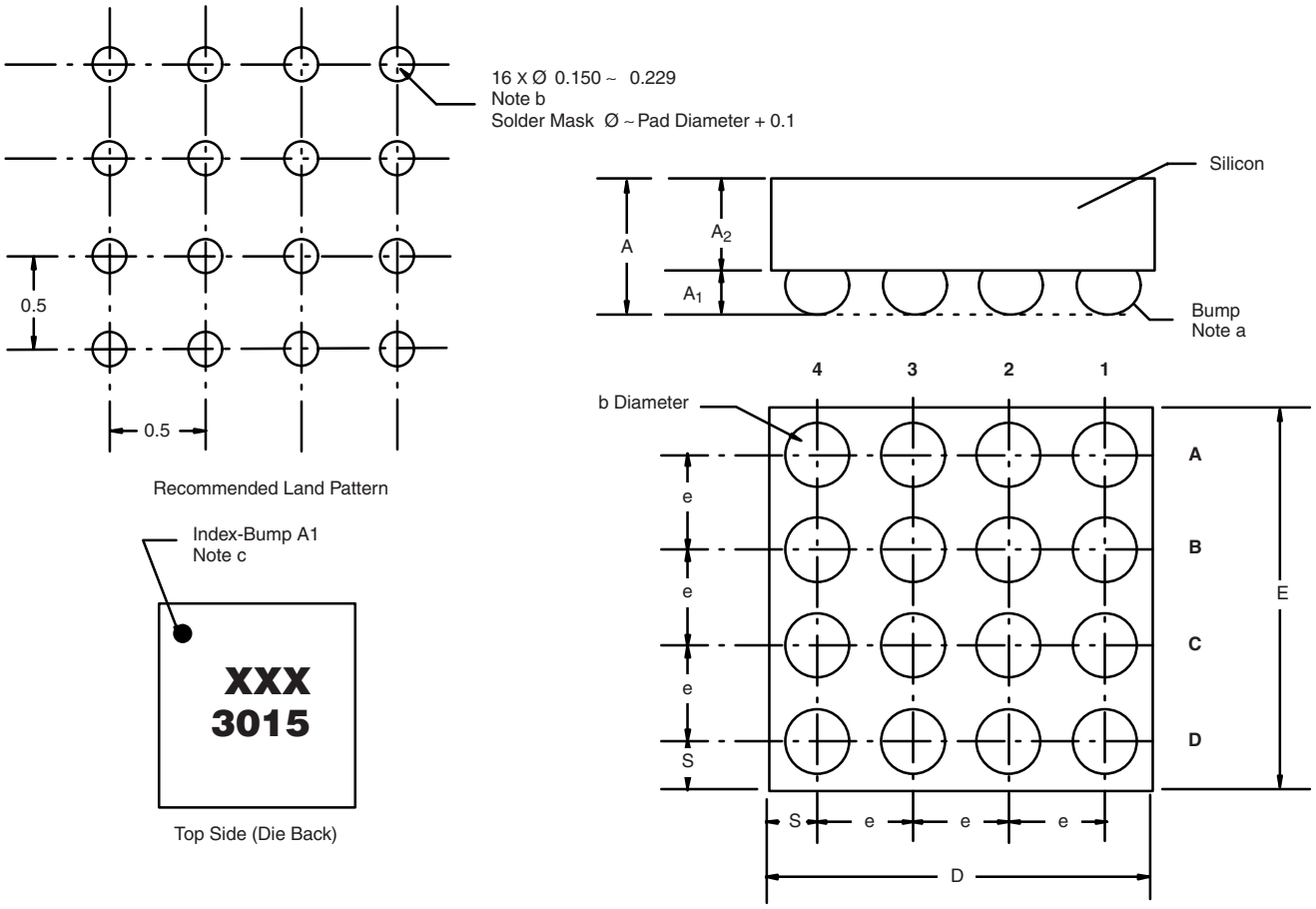
PACKAGE OUTLINE

MICRO FOOT: 16 BUMP (4 x 4, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Notes (Unless Otherwise Specified):
a. Bump is Lead (Pb)-free Sn/Ag/Cu.
b. Non-solder mask defined copper landing pad.
c. Laser Mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

Dim.	Millimeters[a]		Inches	
	Min.	Max.	Min.	Max.
A	0.688	0.753	0.0271	0.0296
A_1	0.218	0.258	0.0086	0.0102
A_2	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.980	2.020	0.0780	0.0795
E	1.980	2.020	0.0780	0.0795
e	0.5 BASIC		0.0197 BASIC	
S	0.230	0.270	0.0091	0.0106

Notes:
a. Use millimeters as the primary measurement.

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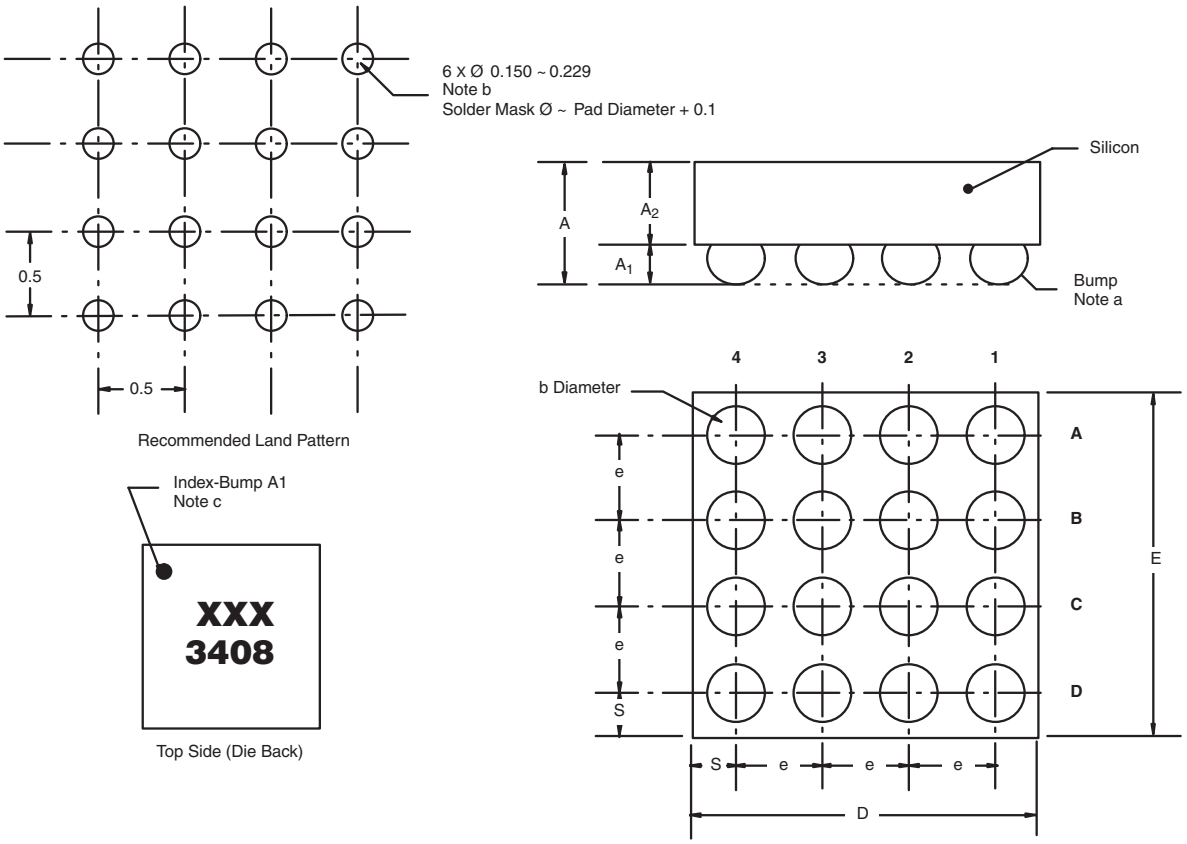
MICRO FOOT: 16-BUMP (4 mm x 4 mm, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



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ECN: S11-1065-Rev. A, 13-Jun-11
DWG: 6000

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