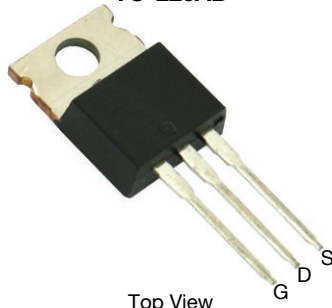


## N-Channel 60 V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ ) MAX.	$I_D$ (A) <sup>d</sup>	$Q_g$ (TYP.)
60	0.0024 at $V_{GS} = 10$ V	120	128 nC
	0.0027 at $V_{GS} = 7.5$ V	120	

**TO-220AB**


Top View

### Ordering Information:

SUP50020E-GE3 (lead (Pb)-free and halogen-free)

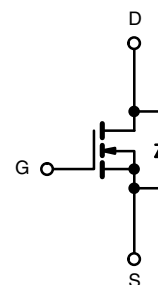
### FEATURES

- TrenchFET® power MOSFET
- Maximum 175 °C junction temperature
- $Q_{gd}/Q_{gs}$  ratio < 0.25
- Operable with logic-level gate drive
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Power supply
  - Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	120 <sup>d</sup>	A
		120 <sup>d</sup>	
Pulsed Drain Current ( $t = 100$ $\mu$ s)	$I_{DM}$	300	
Avalanche Current	$I_{AS}$	75	
Single Avalanche Energy <sup>a</sup>	$E_{AS}$	281	mJ
Maximum Power Dissipation <sup>a</sup>	$P_D$	375 <sup>b</sup>	W
		125 <sup>b</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	°C

### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient (PCB Mount) <sup>c</sup>	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	0.4	

### Notes

- Duty cycle  $\leq 1$  %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR4 material).
- Package limited.

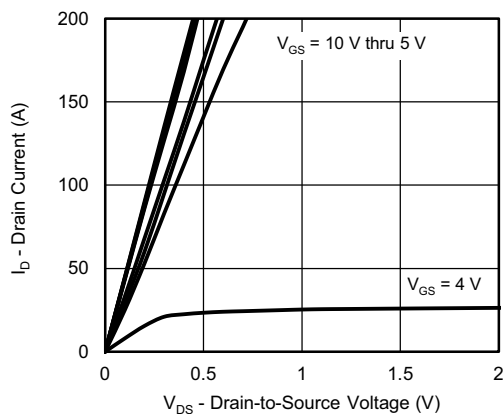
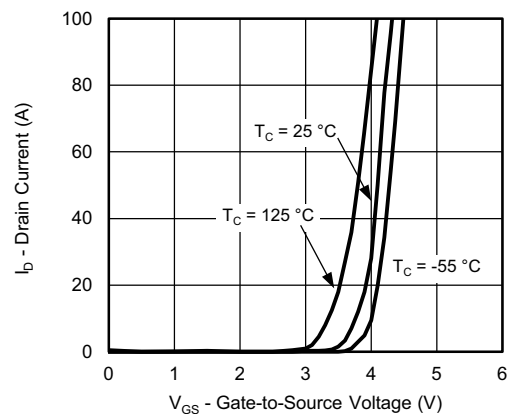
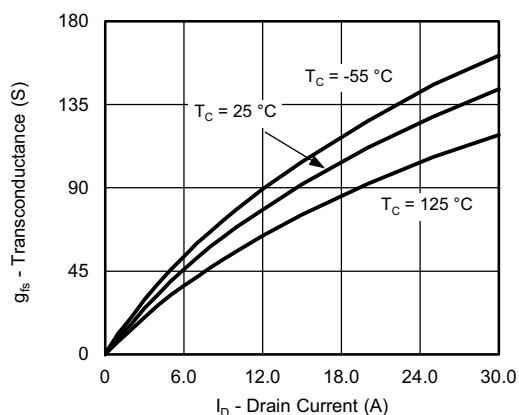
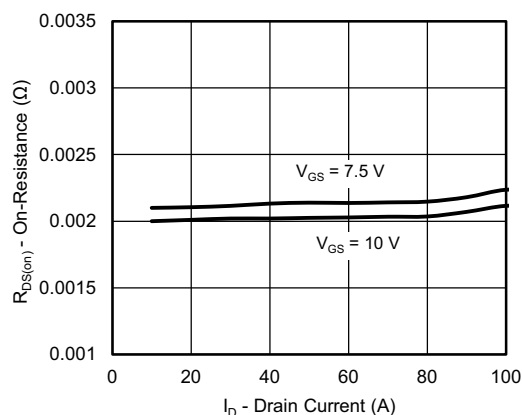
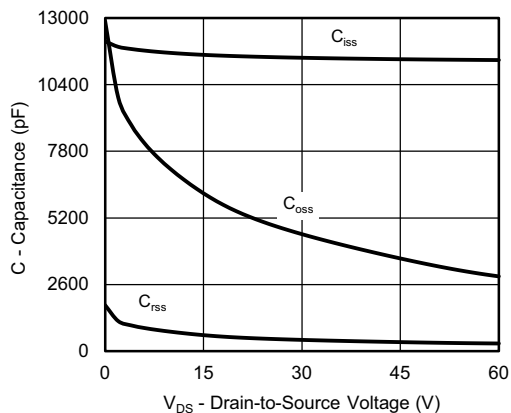
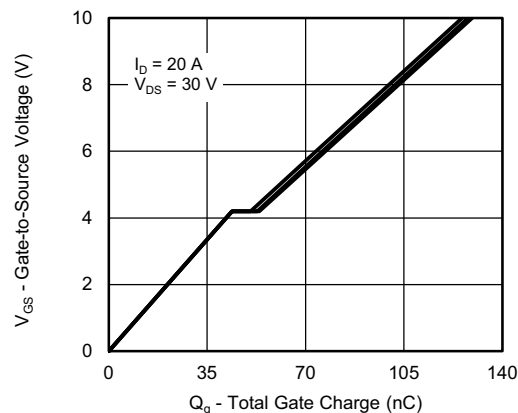


SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	-	4	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 250	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	150	
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	-	5	mA
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 10 V, V <sub>GS</sub> = 10 V	120	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A	-	0.0020	0.0024	Ω
		V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 20 A	-	0.0022	0.0027	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A	-	145	-	S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V, f = 1 MHz	-	11 150	-	pF
Output Capacitance	C <sub>oss</sub>		-	4255	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	420	-	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	128	-	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>		-	44	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>		-	9	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.32	1.6	3.2	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 5 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	18	36	ns
Rise Time <sup>c</sup>	t <sub>r</sub>		-	20	40	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>		-	55	100	
Fall Time <sup>c</sup>	t <sub>f</sub>		-	23	35	
Drain-Source Body Diode Ratings and Characteristics <sup>b</sup> (T <sub>C</sub> = 25 °C)						
Pulsed Current (t = 100 μs)	I <sub>SM</sub>		-	-	300	A
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.8	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 39 A, di/dt = 100 A/μs	-	120	180	ns
Peak Reverse Recovery Charge	I <sub>RM(REC)</sub>		-	5.5	11	A
Reverse Recovery Charge	Q <sub>rr</sub>		-	0.320	0.480	μC

**Notes**

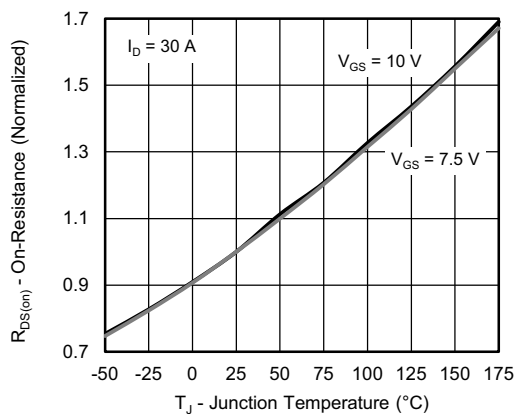
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

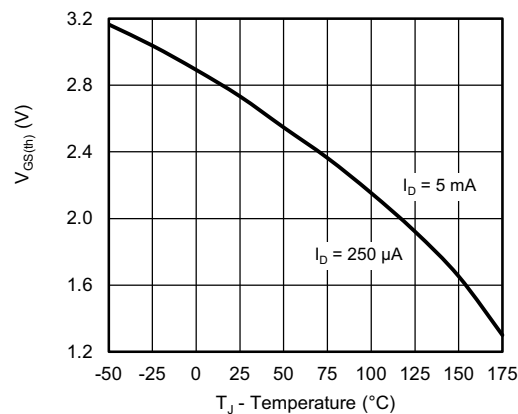
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**



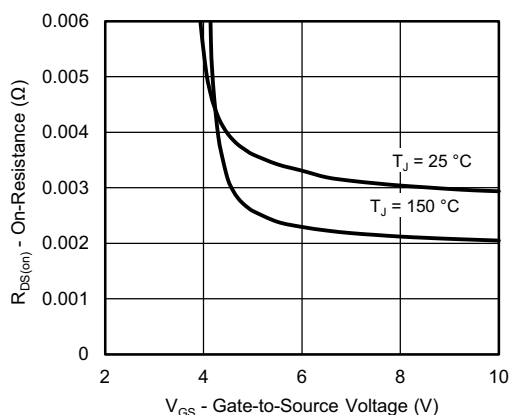
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



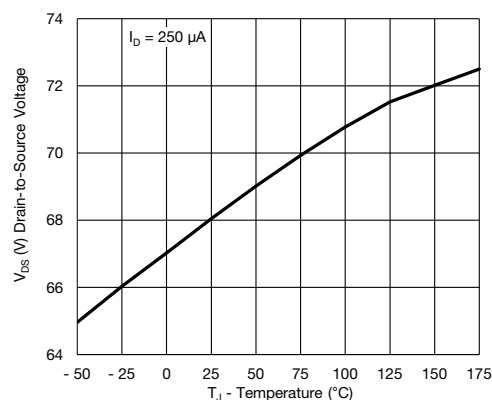
**On-Resistance vs. Junction Temperature**



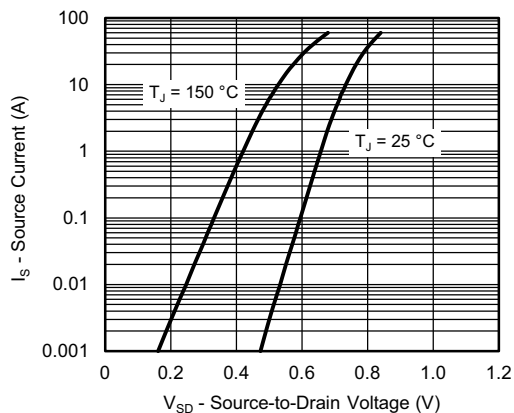
**Threshold Voltage**



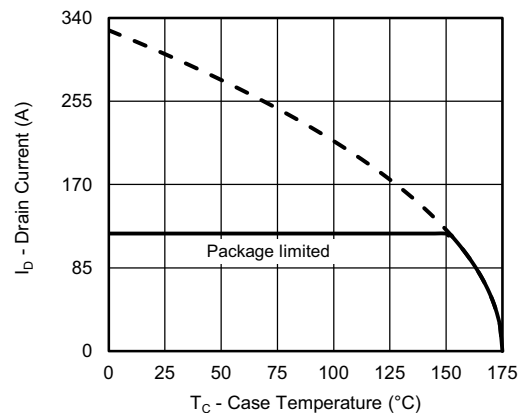
**On-Resistance vs. Gate-to-Source Voltage**



**Drain Source Breakdown vs. Junction Temperature**



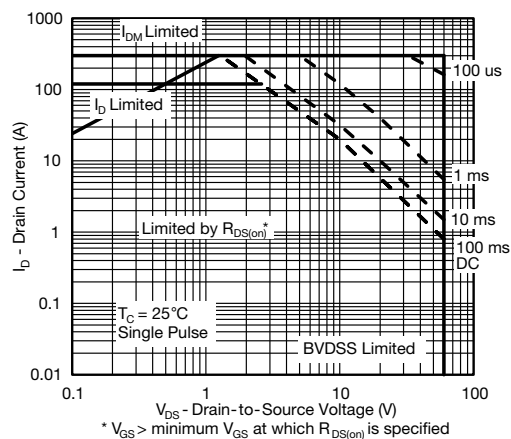
**Source Drain Diode Forward Voltage**



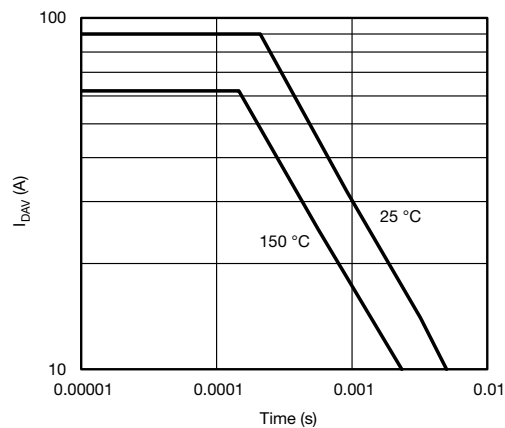
**Current De-rating**



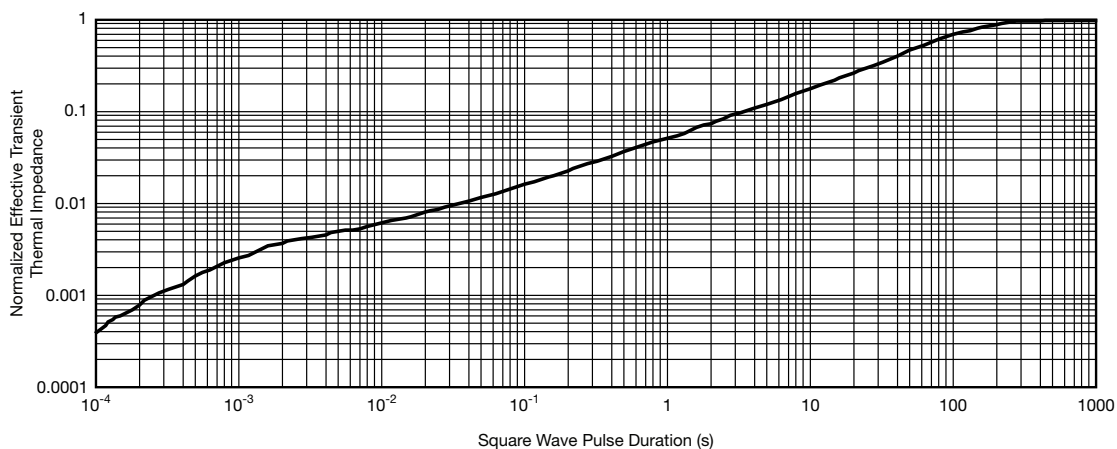
**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



Safe Operating Area



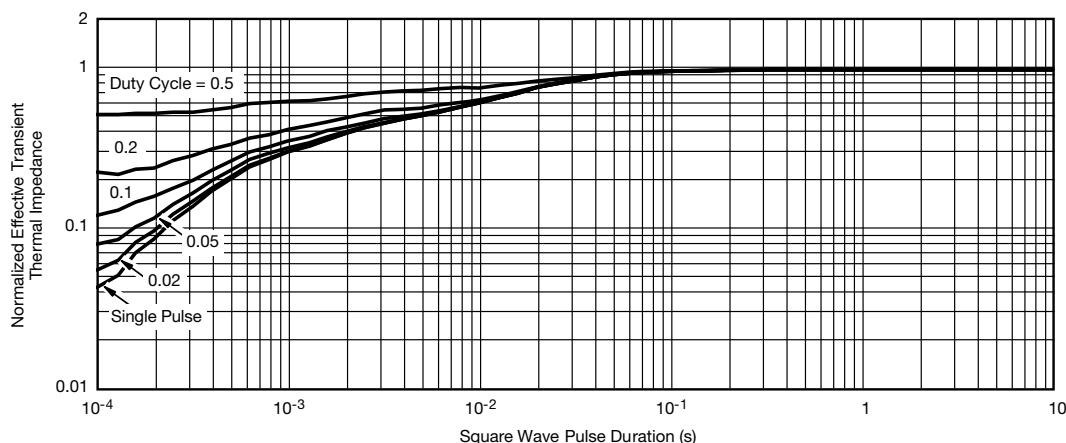
Single Pulse Avalanche Current Capability vs. Time



Normalized Thermal Transient Impedance, Junction-to-Ambient



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction to Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction to Case ( $25\text{ }^{\circ}\text{C}$ )are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?74901](http://www.vishay.com/ppg?74901).



## TO-220AB

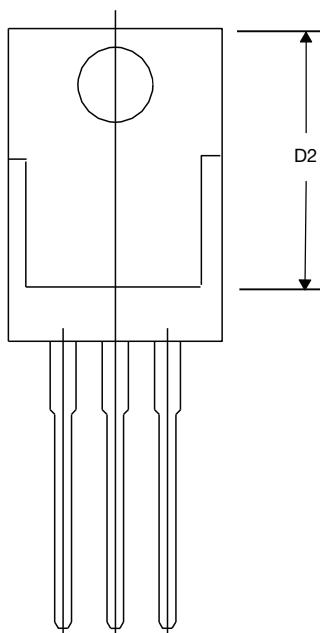


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
D2	12.19	12.70	0.480	0.500
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: T14-0413-Rev. P, 16-Jun-14  
DWG: 5471

### Note

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM





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