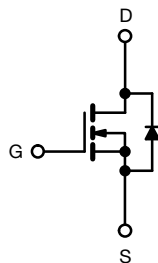
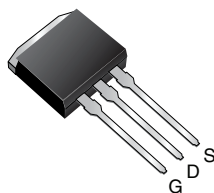


Power MOSFET

I²PAK (TO-262)


N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.75
Q_g max. (nC)	49	
Q_{gs} (nC)	13	
Q_{gd} (nC)	20	
Configuration	Single	

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche, and dynamic dv/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN
FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptable power supply
- High speed power switching
- This device is only for through-hole application

APPLICABLE OFF LINE SMPS TOPOLOGIES

- Active clamped forward
- Main switch

ORDERING INFORMATION

Package	I ² PAK (TO-262)
Lead (Pb)-free and halogen-free	SiHFSL9N60A-GE3
Lead (Pb)-free	IRFSL9N60APbF

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V_{DS}	600	V	
Gate-source voltage			V_{GS}	± 30		
Continuous drain current	$V_{GS} \text{ at } 10\text{ V}$	$T_C = 25\text{ }^\circ\text{C}$	I_D	9.2	A	
		$T_C = 100\text{ }^\circ\text{C}$		5.8		
Pulsed drain current ^a			I_{DM}	37		
Linear derating factor				1.3	W/ $^\circ\text{C}$	
Single pulse avalanche energy ^b			E_{AS}	290	mJ	
Repetitive avalanche current ^a			I_{AR}	9.2	A	
Repetitive avalanche energy ^a			E_{AR}	17	mJ	
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$		P_D	170	W	
Peak diode recovery dv/dt ^c			dv/dt	5.0	V/ns	
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Soldering recommendations (peak temperature) ^d	For 10 s			300		

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 6.8\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 9.2\text{ A}$ (see fig. 12)
- $I_{SD} \leq 9.2\text{ A}$, $di/dt \leq 50\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mounted, steady-state)	R_{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.75	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250\text{ }\mu\text{A}$	600	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}^b$	-	-	0.75	Ω
Forward transconductance	g_{fs}	$V_{DS} = 25\text{ V}$, $I_D = 3.1\text{ A}^b$	5.5	-	-	S
Dynamic						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	1400	-	pF
Output capacitance	C_{oss}		-	180	-	
Reverse transfer capacitance	C_{rss}		-	7.1	-	
Output capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	1957	pF
Effective output capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 480\text{ V}$, $f = 1.0\text{ MHz}$	-	49	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 0\text{ V to } 480\text{ V}^c$	-	96	nC
Gate-source charge	Q_{gs}		$I_D = 9.2\text{ A}$, $V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^b	-	49	
Gate-drain charge	Q_{gd}			-	13	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 300\text{ V}$, $I_D = 9.2\text{ A}$, $R_g = 9.1\text{ }\Omega$, $R_D = 35.5\text{ }\Omega$, see fig. 10 ^b	-	13	-	ns
Rise time	t_r		-	25	-	
Turn-off delay time	$t_{d(off)}$		-	30	-	
Fall time	t_f		-	22	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	9.2	A
Pulsed diode forward current ^a	I_{SM}		-	-	37	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 9.2\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = 9.2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}^b$	-	530	800	ns
Body diode reverse recovery charge	Q_{rr}		-	3.0	4.4	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80% V_{DS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

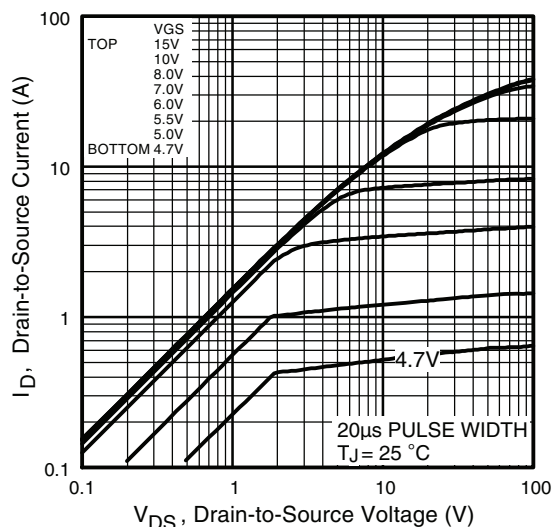


Fig. 1 - Typical Output Characteristics

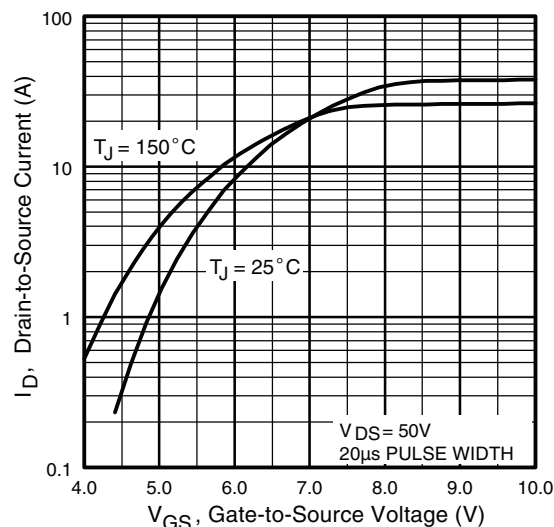


Fig. 3 - Typical Transfer Characteristics

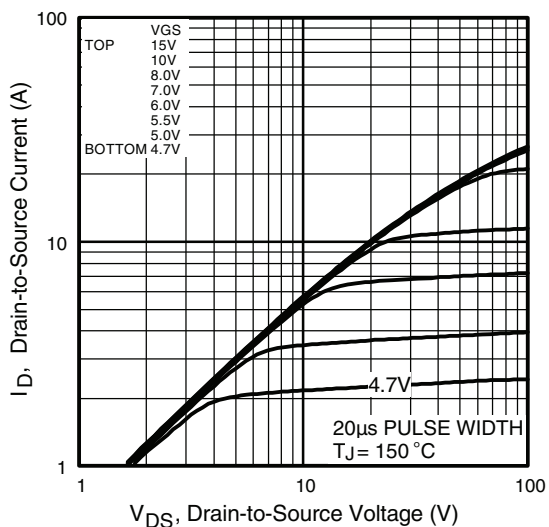


Fig. 2 - Typical Output Characteristics

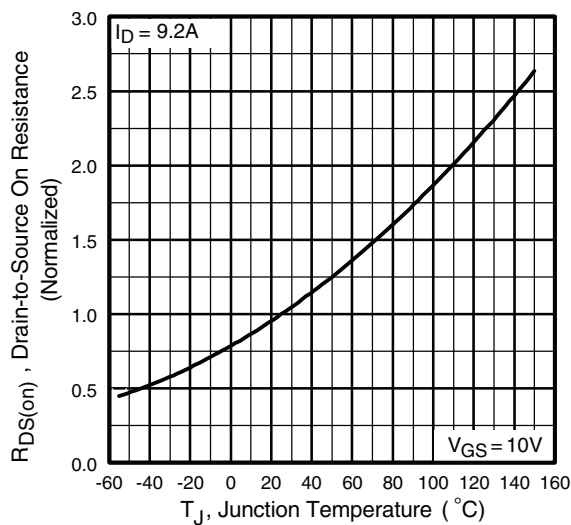
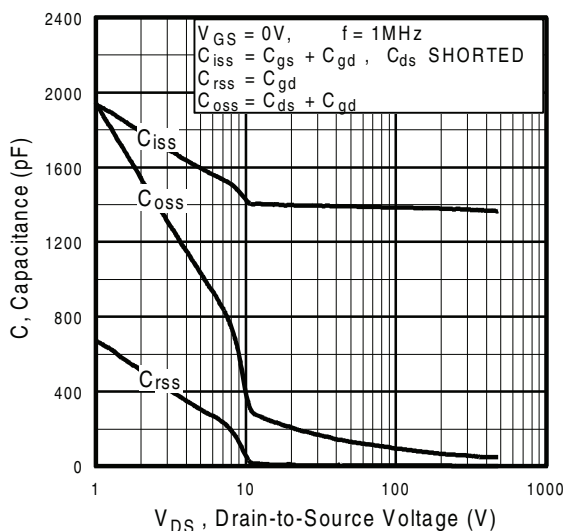
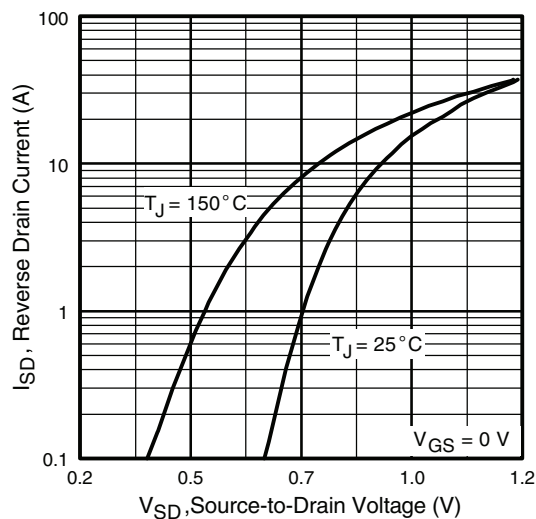
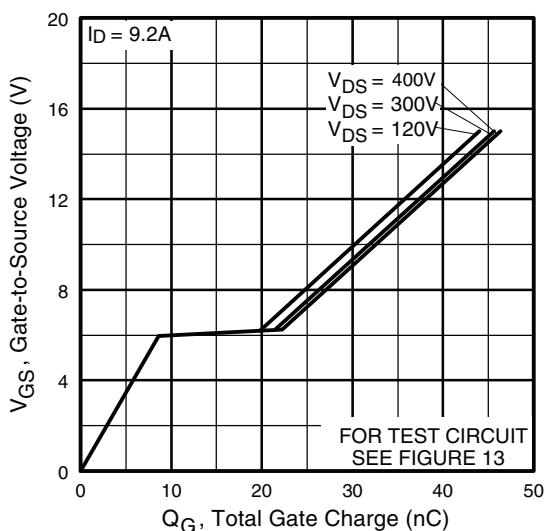
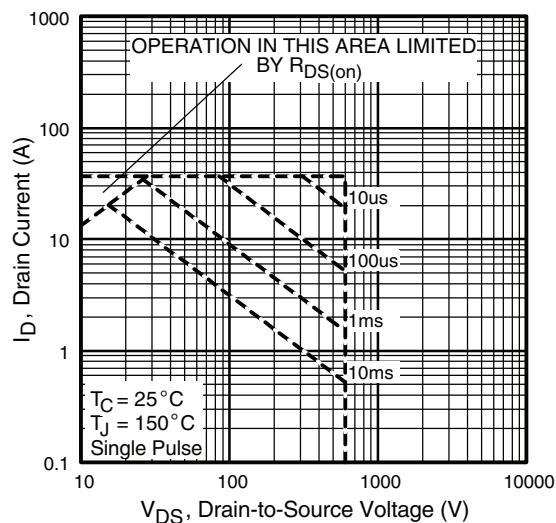


Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area

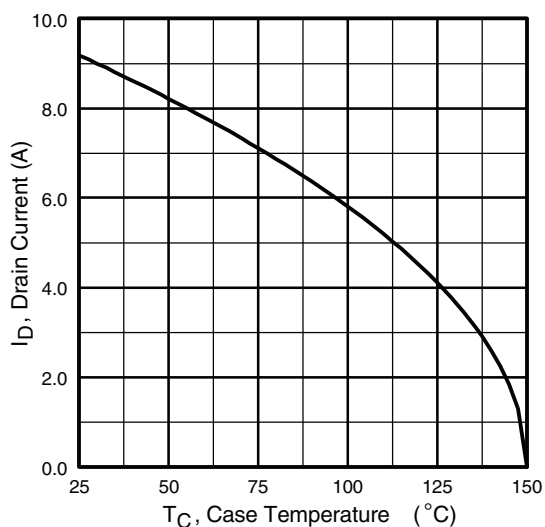
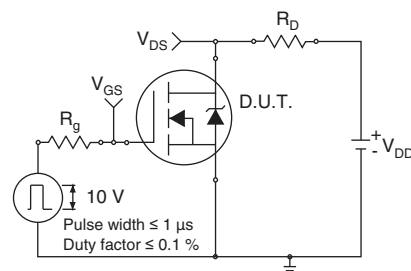
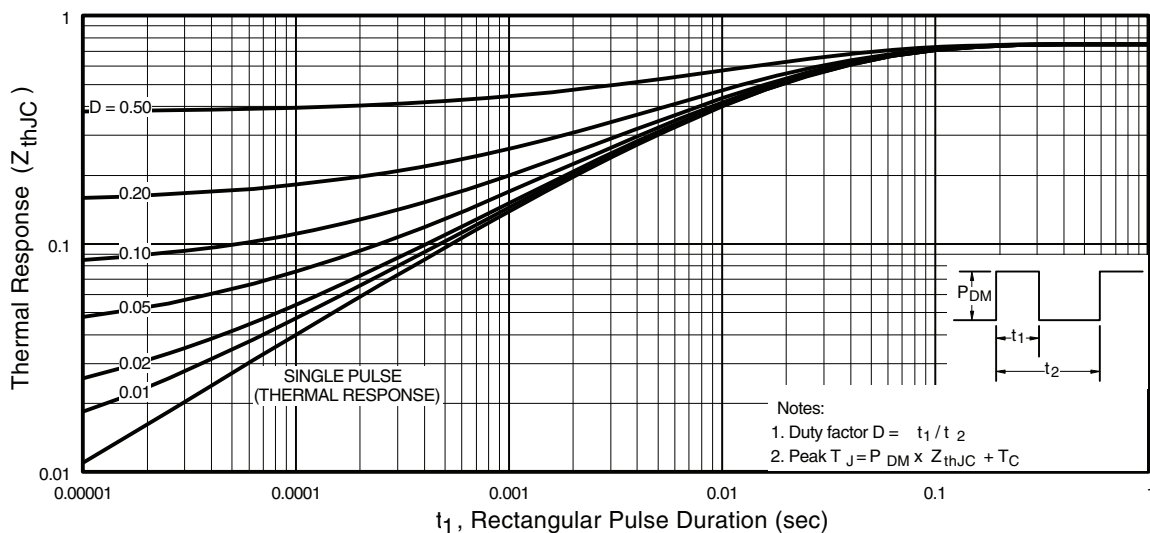
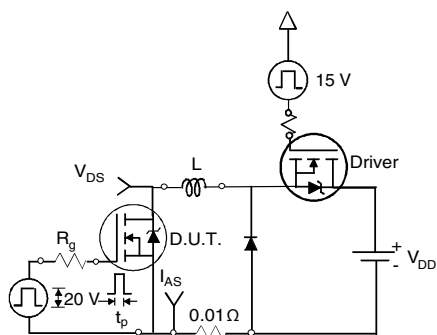
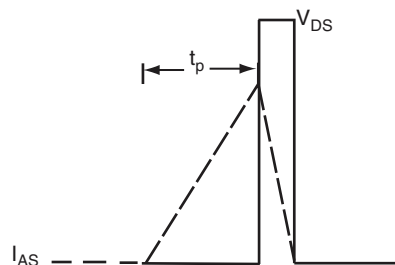
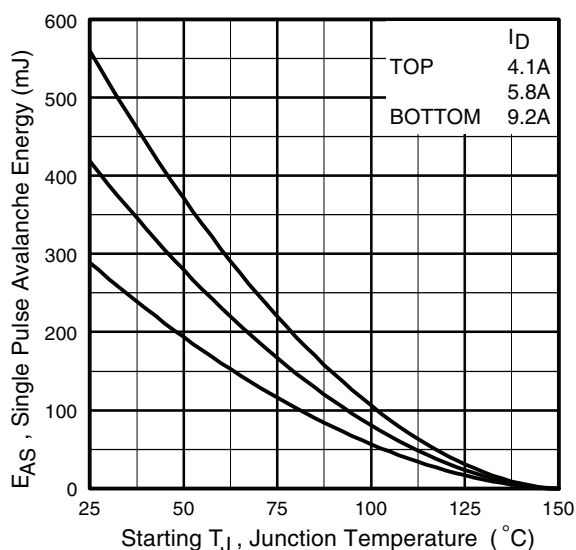
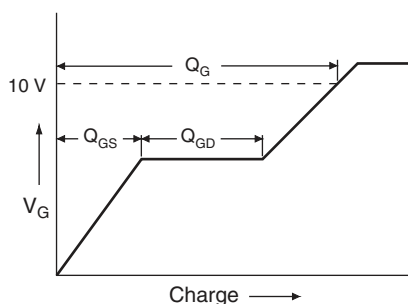
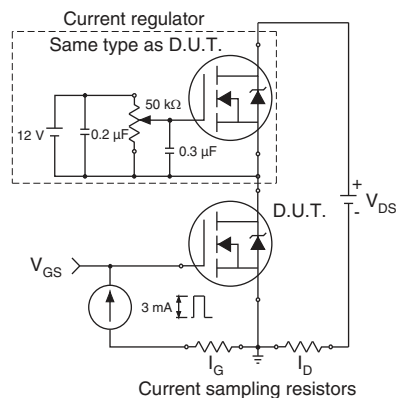
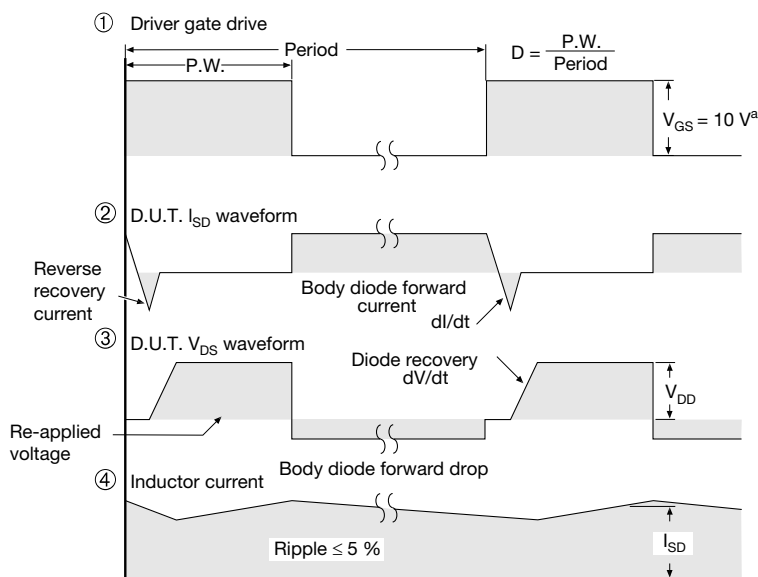
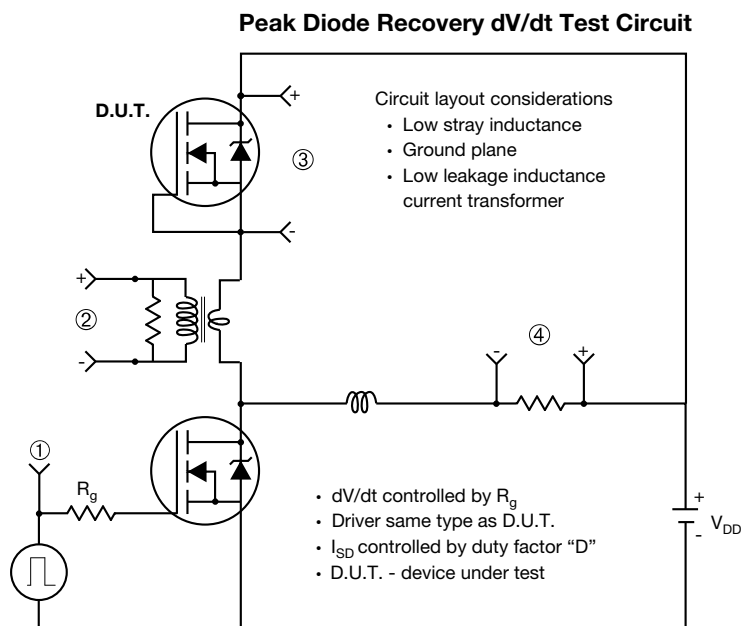

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit


Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



I²PAK (TO-262) (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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