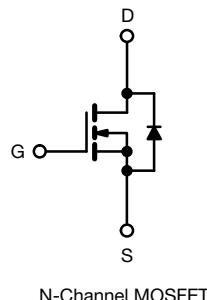


## E Series Power MOSFET with Fast Body Diode

**Thin-Lead TO-220 FULLPAK**

**FEATURES**

- Fast body diode MOSFET using E series technology
- Reduced  $t_{rr}$ ,  $Q_{rr}$ , and  $I_{RRM}$
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Low switching losses due to reduced  $Q_{rr}$
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

**APPLICATIONS**

- Telecommunications
  - Server and telecom power supplies
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Consumer and computing
  - ATX power supplies
- Industrial
  - Welding
  - Battery chargers
- Renewable energy
  - Solar (PV inverters)
- Switch mode power supplies (SMPS)
- Applications using the following topologies
  - LCC
  - Phase shifted bridge (ZVS)
  - 3-level inverter
  - AC/DC bridge

**PRODUCT SUMMARY**

$V_{DS}$ (V) at $T_J$ max.	700	
$R_{DS(on)}$ max. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.18
$Q_g$ max. (nC)	106	
$Q_{gs}$ (nC)	14	
$Q_{gd}$ (nC)	33	
Configuration	Single	

**ORDERING INFORMATION**

Package	Thin-Lead TO-220 FULLPAK
Lead (Pb)-free	SiHA21N65EF-E3
Lead (Pb)-free and halogen-free	SiHA21N65EF-GE3

**ABSOLUTE MAXIMUM RATINGS** ( $T_C = 25$  °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	650	V
Gate-source voltage		$\pm 30$	
Continuous drain current ( $T_J = 150$ °C) <sup>e</sup>	$I_D$	21	A
$V_{GS}$ at 10 V		13	
Pulsed drain current <sup>a</sup>	$I_{DM}$	53	
Linear derating factor		0.28	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	367	mJ
Maximum power dissipation	$P_D$	35	W
Operating junction and storage temperature range	$T_J$ , $T_{stg}$	-55 to +150	°C
Drain-source voltage slope	$dV/dt$	37	V/ns
Reverse diode $dV/dt$ <sup>d</sup>		31	
Soldering recommendations (peak temperature) <sup>c</sup>	for 10 s	300	°C
Mounting torque	M3 screw	0.6	Nm

**Notes**

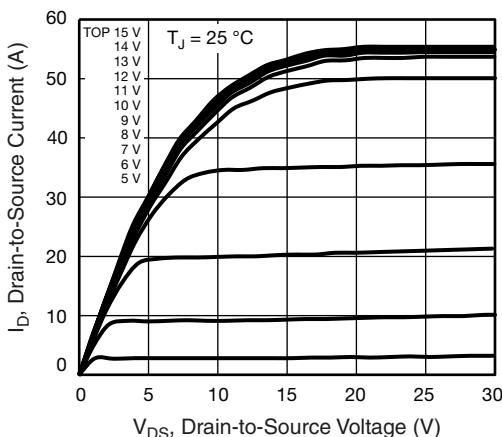
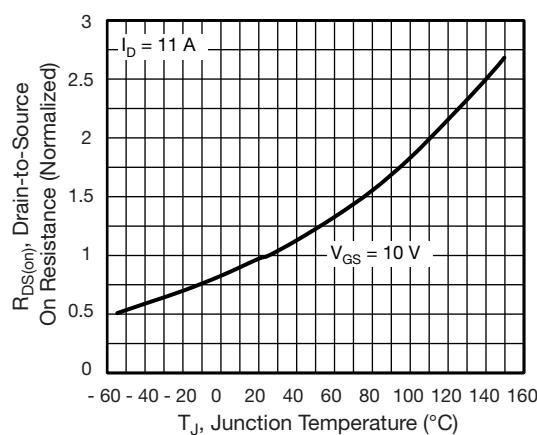
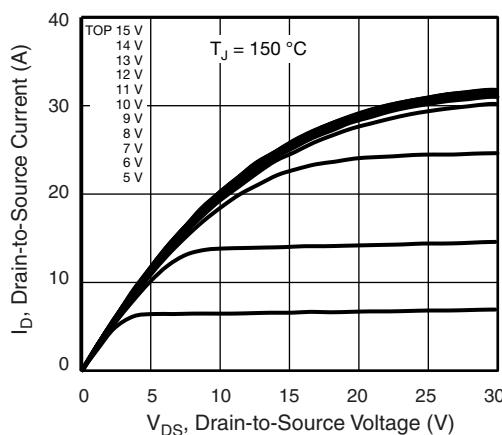
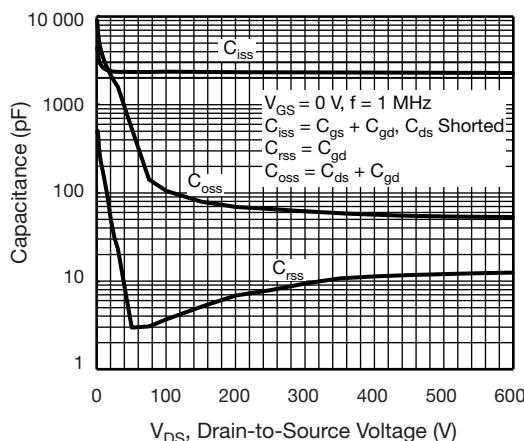
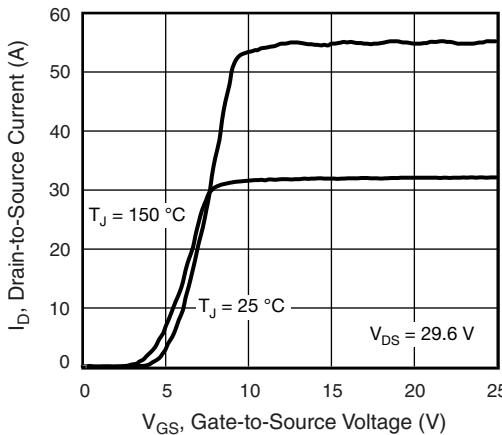
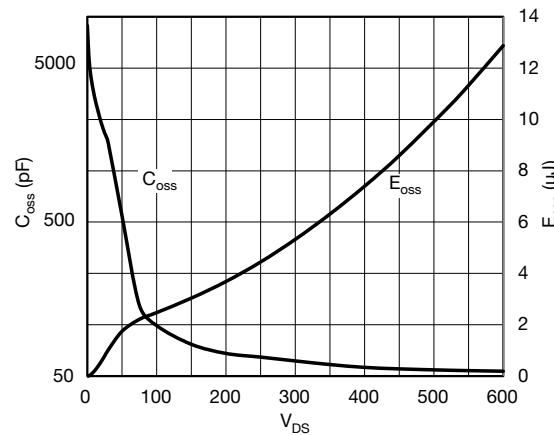
- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$  Ω,  $I_{AS} = 5.1$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/μs, starting  $T_J = 25$  °C
- Limited by maximum junction temperature

<b>THERMAL RESISTANCE RATINGS</b>				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	65	
Maximum junction-to-case (drain)	$R_{thJC}$	-	3.6	°C/W

<b>SPECIFICATIONS</b> ( $T_J = 25$ °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ μA		650	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1$ mA		-	0.67	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ μA		2	-	4	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20$ V		-	-	± 100	nA
		$V_{GS} = \pm 30$ V		-	-	± 1	μA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 520$ V, $V_{GS} = 0$ V		-	-	1	
		$V_{DS} = 520$ V, $V_{GS} = 0$ V, $T_J = 125$ °C		-	-	500	μA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 11$ A	-	0.15	0.18	Ω
Forward transconductance	$g_{fs}$	$V_{DS} = 30$ V, $I_D = 11$ A		-	7.0	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0$ V, $V_{DS} = 100$ V, $f = 1$ MHz		-	2322	-	pF
Output capacitance	$C_{oss}$			-	105	-	
Reverse transfer capacitance	$C_{rss}$			-	4	-	
Effective output capacitance, energy related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0$ V to 520 V, $V_{GS} = 0$ V		-	84	-	
Effective output capacitance, time related <sup>b</sup>	$C_{o(tr)}$			-	293	-	
Total gate charge	$Q_g$	$V_{GS} = 10$ V	$I_D = 11$ A, $V_{DS} = 520$ V	-	71	106	nC
Gate-source charge	$Q_{gs}$			-	14	-	
Gate-drain charge	$Q_{gd}$			-	33	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 520$ V, $I_D = 11$ A, $V_{GS} = 10$ V, $R_g = 9.1$ Ω		-	22	44	ns
Rise time	$t_r$			-	34	68	
Turn-off delay time	$t_{d(off)}$			-	68	102	
Fall time	$t_f$			-	42	84	
Gate input resistance	$R_g$	$f = 1$ MHz, open drain		-	0.78	-	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	21	A
Pulsed diode forward current	$I_{SM}$			-	-	53	
Diode forward voltage	$V_{SD}$	$T_J = 25$ °C, $I_S = 11$ A, $V_{GS} = 0$ V		-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$T_J = 25$ °C, $I_F = I_S = 11$ A, $dl/dt = 100$ A/μs, $V_R = 25$ V		-	160	-	ns
Reverse recovery charge	$Q_{rr}$			-	1.2	-	μC
Reverse recovery current	$I_{RRM}$			-	14	-	A

**Notes**

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$   
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**

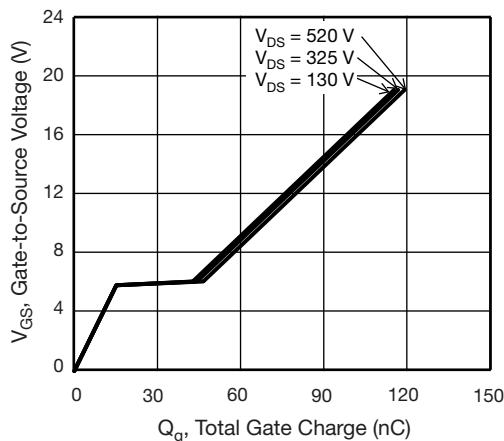


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

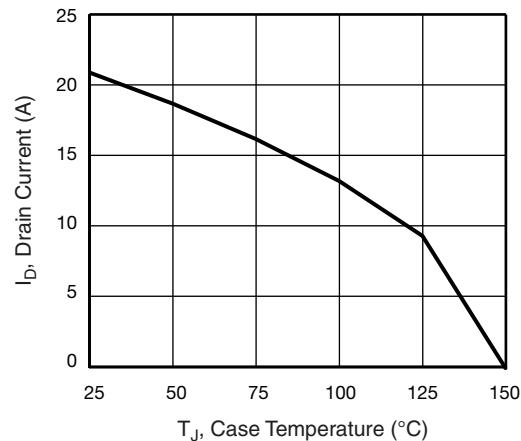


Fig. 10 - Maximum Drain Current vs. Case Temperature

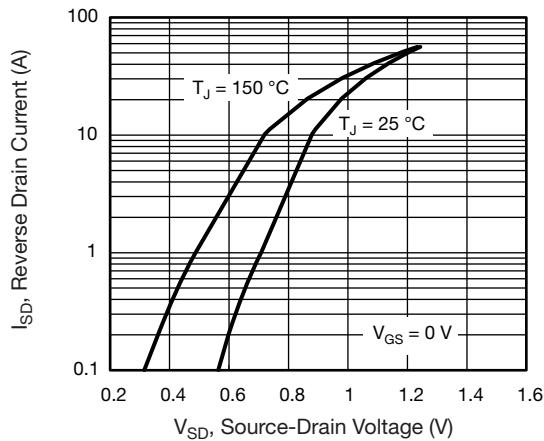


Fig. 8 - Typical Source-Drain Diode Forward Voltage

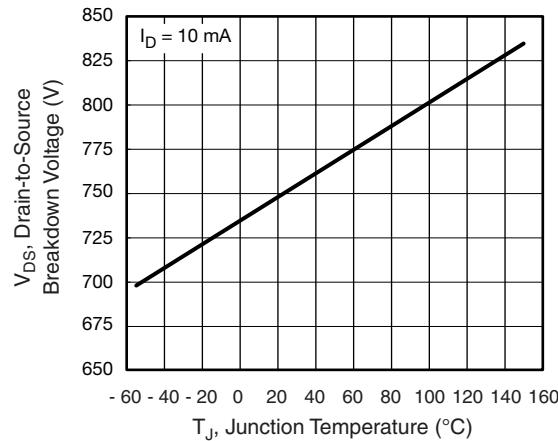


Fig. 11 - Temperature vs. Drain-to-Source Voltage

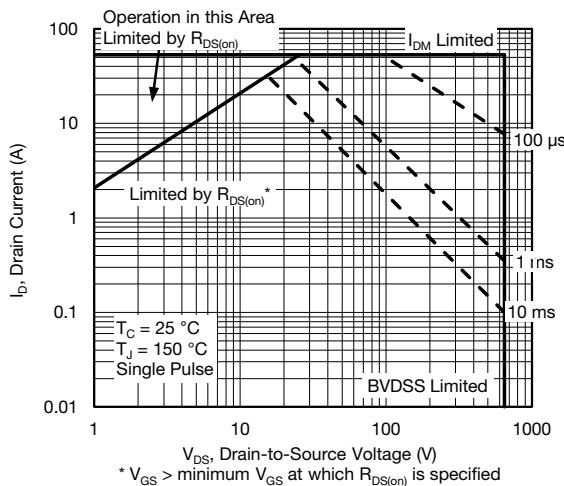
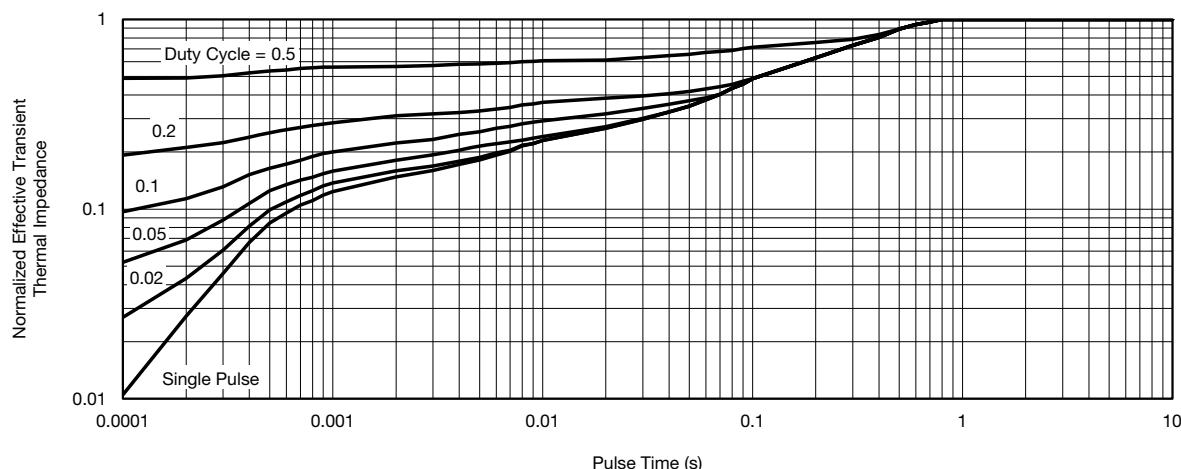
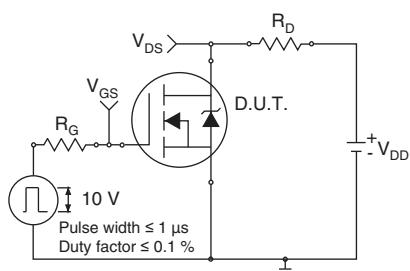


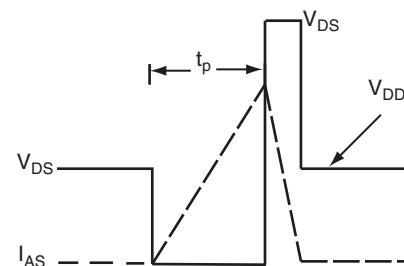
Fig. 9 - Maximum Safe Operating Area



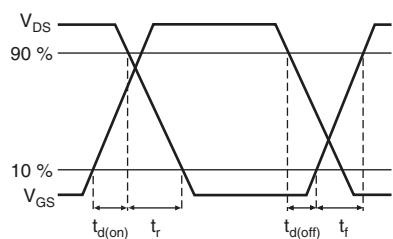
**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**



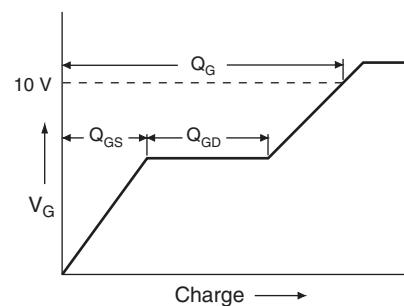
**Fig. 13 - Switching Time Test Circuit**



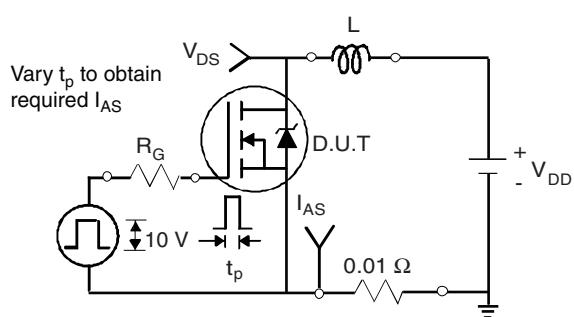
**Fig. 16 - Unclamped Inductive Waveforms**



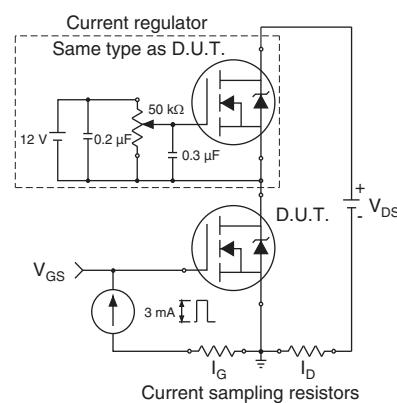
**Fig. 14 - Switching Time Waveforms**



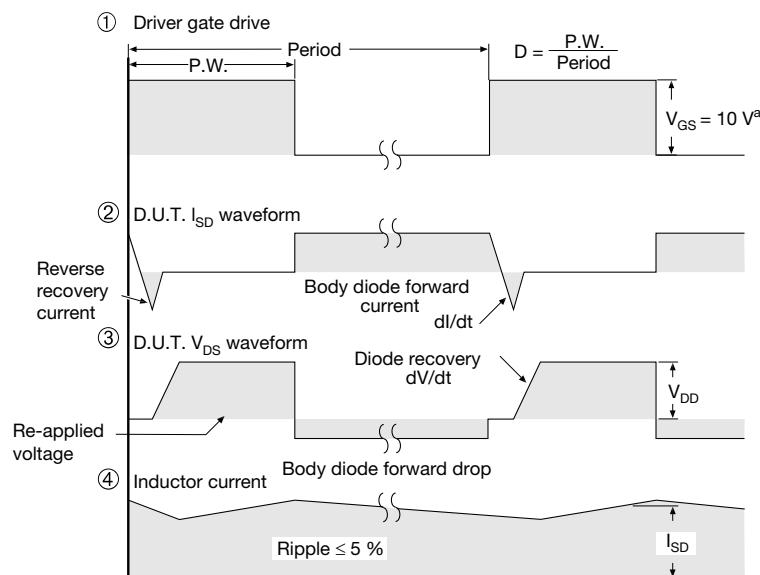
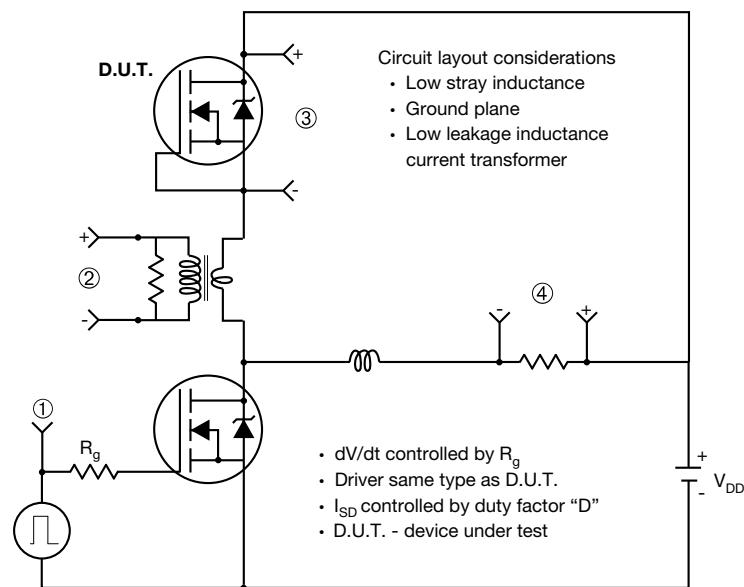
**Fig. 17 - Basic Gate Charge Waveform**



**Fig. 15 - Unclamped Inductive Test Circuit**



**Fig. 18 - Gate Charge Test Circuit**

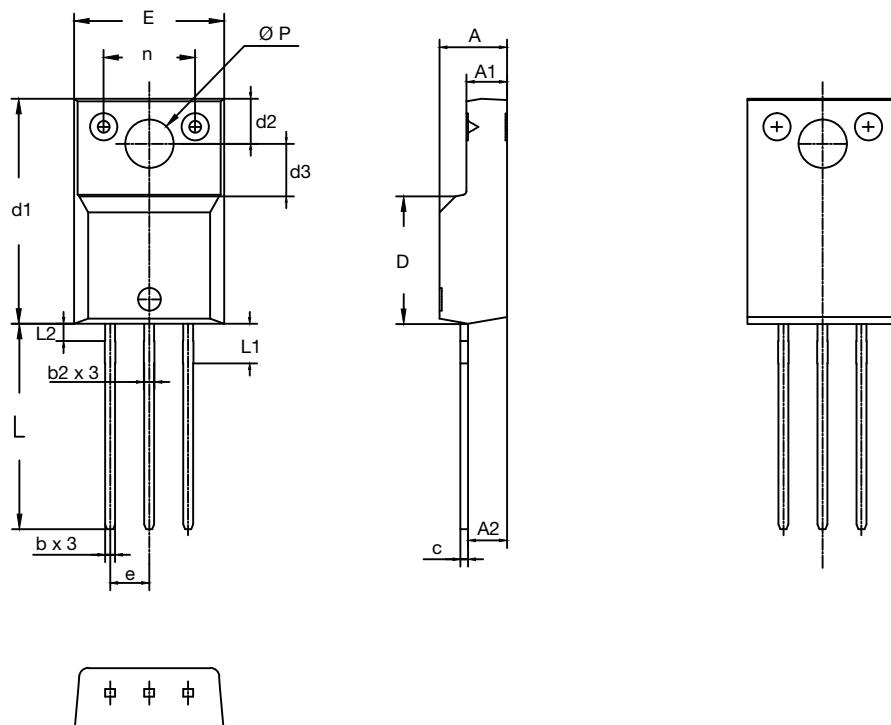
**Peak Diode Recovery dV/dt Test Circuit**

**Note**

a.  $V_{GS} = 5 \text{ V}$  for logic level devices

**Fig. 19 - For N-Channel**

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## TO-220 FULLPAK Thin Lead



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.30	4.70	0.169	0.185
A1	2.50	2.90	0.098	0.114
A2	2.50	2.70	0.098	0.106
b	0.60	0.80	0.024	0.031
b2	0.60	0.90	0.024	0.035
c	-	0.60	-	0.024
D	8.30	8.70	0.327	0.342
d1	14.70	15.30	0.579	0.602
d2	2.90	3.10	0.114	0.122
d3	3.40	3.60	0.134	0.142
E	9.70	10.30	0.382	0.406
e	2.50	2.70	0.098	0.106
L	13.40	13.80	0.528	0.543
L1	2.50	2.80	0.098	0.110
L2	-	1.20	-	0.047
n	6.05	6.15	0.238	0.242
ØP	3.00	3.40	0.118	0.134

ECN: T16-0549-Rev. C, 12-Sep-16  
DWG: 6021

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