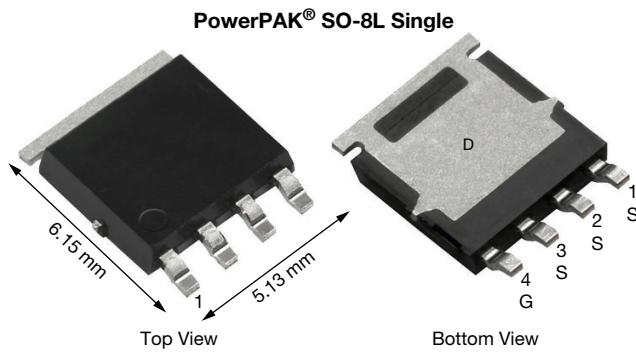


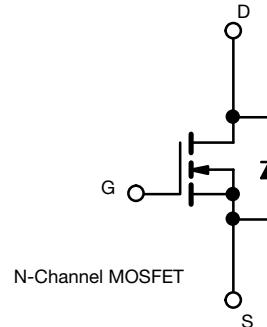
Automotive N-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.014
I_D (A)	48
Configuration	Single
Package	PowerPAK SO-8L



FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified ^d
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_C = 25$ °C	I_D	48	
	$T_C = 125$ °C		27	
Continuous Source Current (Diode Conduction) ^a		I_S	60	A
Pulsed Drain Current ^b		I_{DM}	160	
Single Pulse Avalanche Current	$L = 0.1$ mH	I_{AS}	36	mJ
Single Pulse Avalanche Energy		E_{AS}	65	
Maximum Power Dissipation ^b	$T_C = 25$ °C	P_D	68	W
	$T_C = 125$ °C		22	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	°C
Soldering Recommendations (Peak Temperature) ^{e, f}			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	68	°C/W
Junction-to-Case (Drain)		R_{thJC}	2.2	

Notes

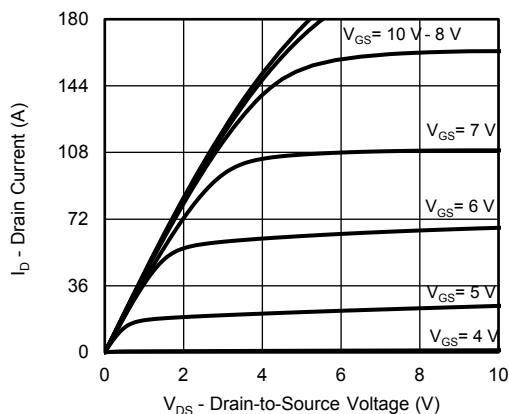
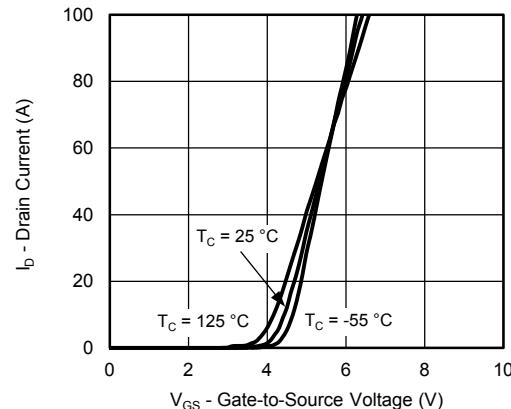
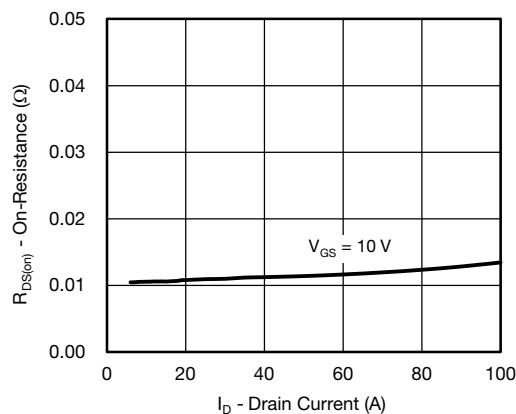
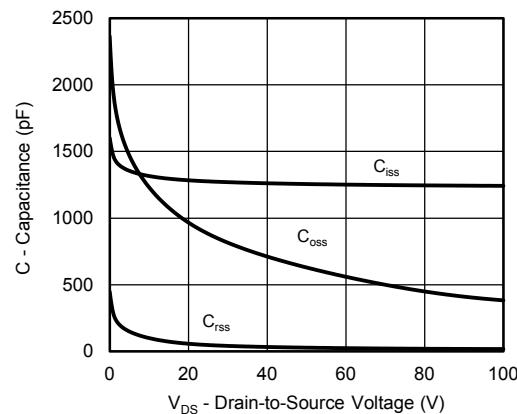
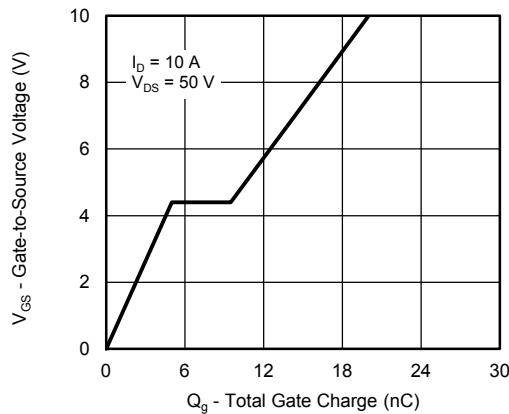
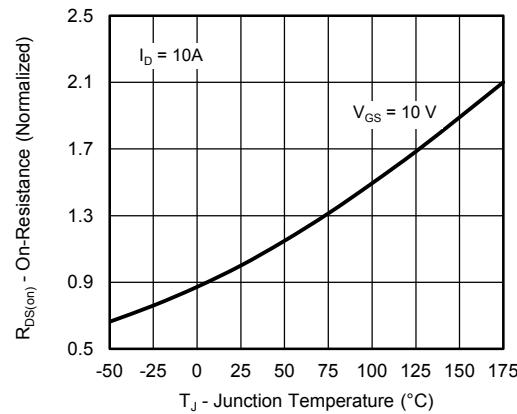
- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

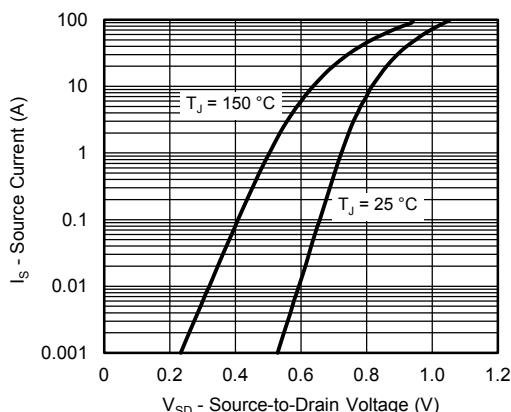
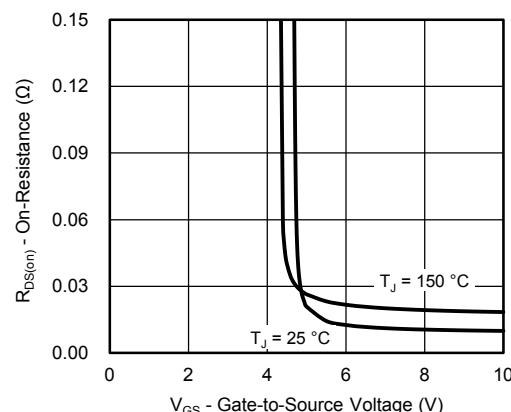
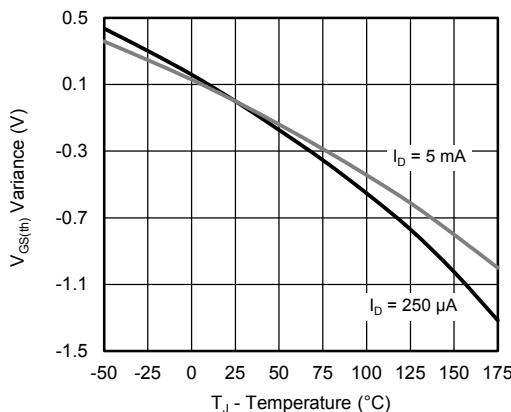
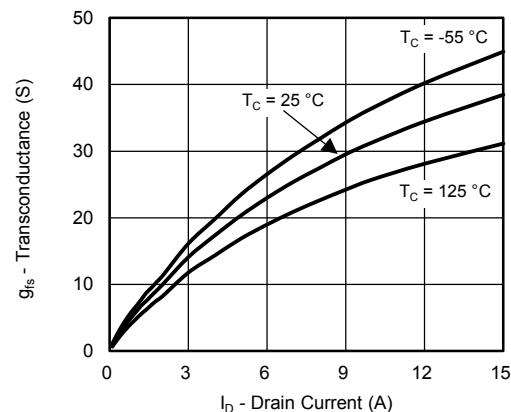
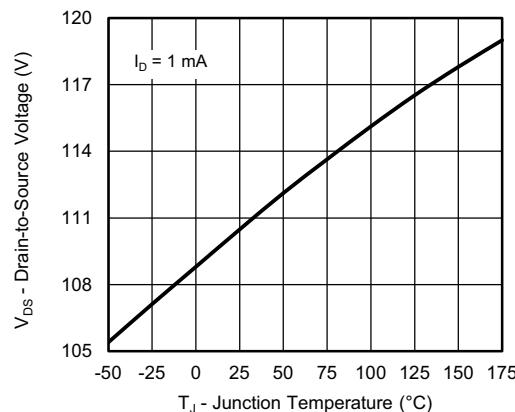
SPECIFICATIONS ($T_C = 25^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250 \mu\text{A}$		100	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2.5	3.0	3.5		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0 \text{ V}$	$V_{DS} = 100 \text{ V}$	-	-	1	μA	
		$V_{GS} = 0 \text{ V}$	$V_{DS} = 100 \text{ V}$, $T_J = 125^\circ\text{C}$	-	-	50		
		$V_{GS} = 0 \text{ V}$	$V_{DS} = 100 \text{ V}$, $T_J = 175^\circ\text{C}$	-	-	150		
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{GS} = 10 \text{ V}$	$V_{DS} \geq 5 \text{ V}$	30	-	-	A	
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$	$I_D = 10 \text{ A}$	-	0.011	0.014	Ω	
		$V_{GS} = 10 \text{ V}$	$I_D = 10 \text{ A}$, $T_J = 125^\circ\text{C}$	-	-	0.024		
		$V_{GS} = 10 \text{ V}$	$I_D = 10 \text{ A}$, $T_J = 175^\circ\text{C}$	-	-	0.030		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 10 \text{ A}$		-	31	-	S	
Dynamic ^b								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$	-	1276	1700	pF	
Output Capacitance	C_{oss}			-	889	1200		
Reverse Transfer Capacitance	C_{rss}			-	48	70		
Total Gate Charge ^c	Q_g	$V_{GS} = 10 \text{ V}$	$V_{DS} = 50 \text{ V}$, $I_D = 20 \text{ A}$	-	20	35	nC	
Gate-Source Charge ^c	Q_{gs}			-	5	-		
Gate-Drain Charge ^c	Q_{gd}			-	4.5	-		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		0.45	1.06	1.70	Ω	
Turn-On Delay Time ^c	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$, $R_L = 10 \Omega$ $I_D \geq 5 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$		-	9	15	ns	
Rise Time ^c	t_r			-	19	35		
Turn-Off Delay Time ^c	$t_{d(\text{off})}$			-	16	25		
Fall Time ^c	t_f			-	19	35		
Source-Drain Diode Ratings and Characteristics ^b								
Pulsed Current ^a	I_{SM}			-	-	160	A	
Forward Voltage	V_{SD}	$I_F = 15 \text{ A}$, $V_{GS} = 0$		-	0.85	1.2	V	

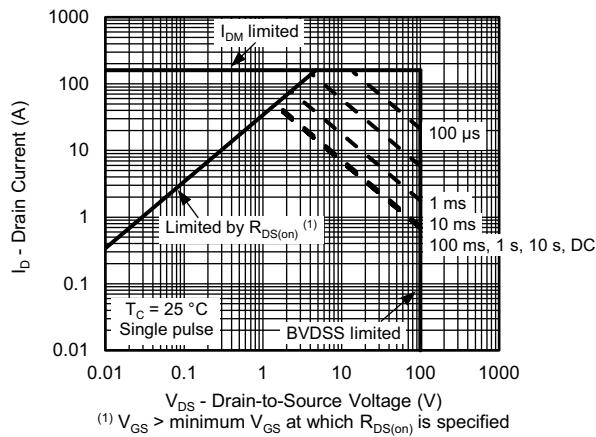
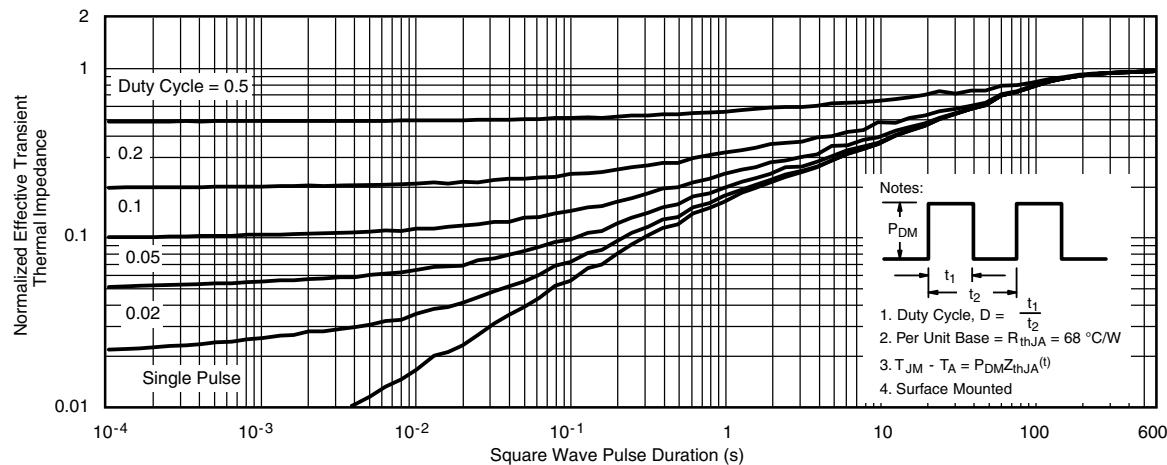
Notes

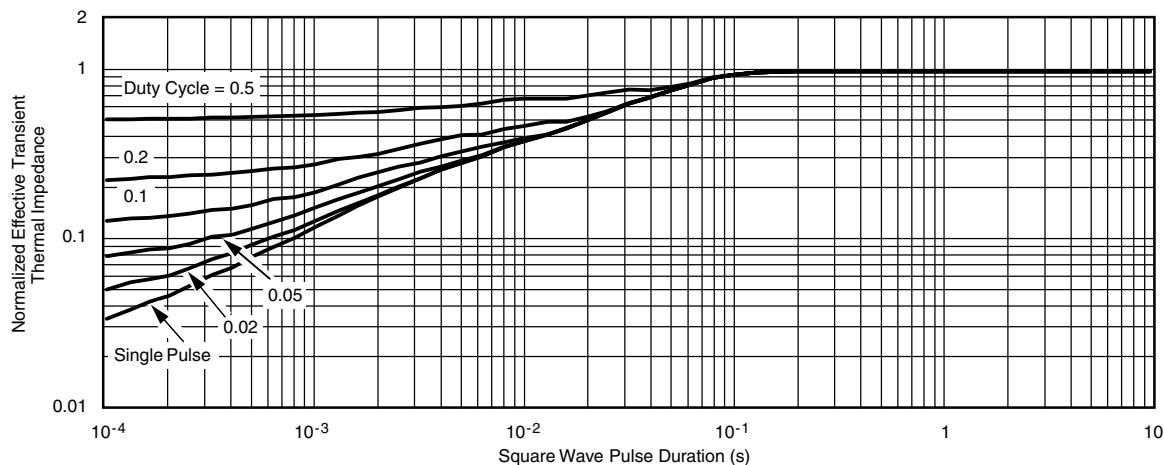
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to Source Voltage

Threshold Voltage

Transconductance

Drain Source Breakdown vs. Junction Temperature

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Case
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

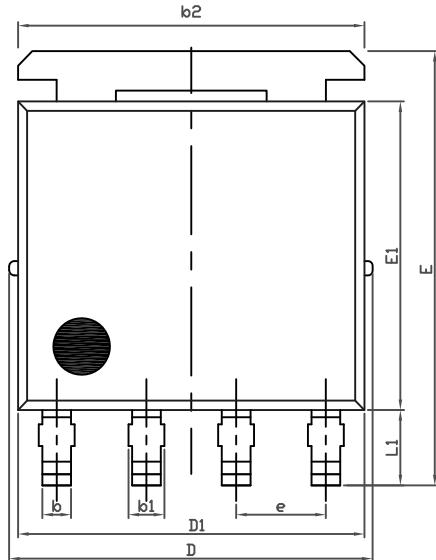
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75958.

REVISION HISTORY ^a		
REVISION	DATE	DESCRIPTION OF CHANGE
B	25-Feb-16	<ul style="list-style-type: none">• Standardized switching and gate charge test conditions

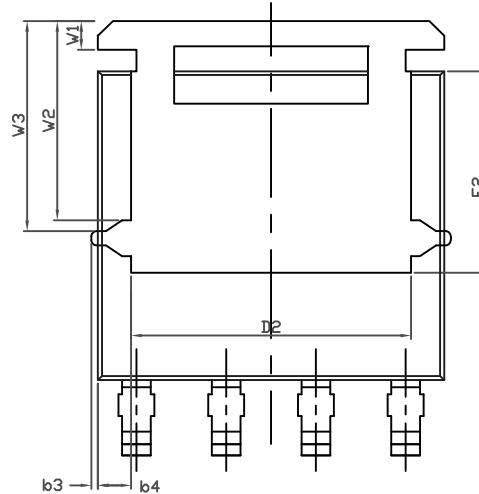
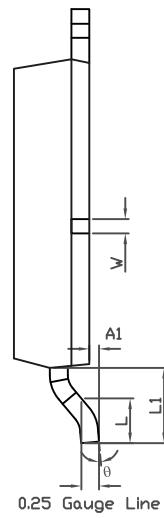
Note

a. As of April 2014

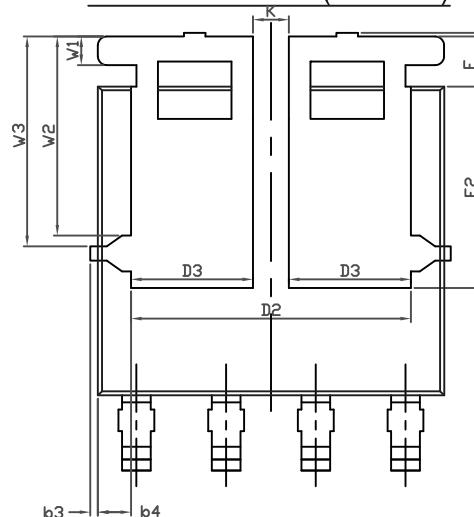
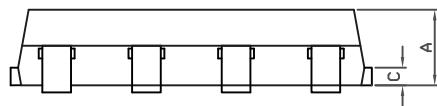
PowerPAK® SO-8L Case Outline for AI Parts



TOPSIDE VIEW



BACKSIDE VIEW(SINGLE)



BACKSIDE VIEW(DUAL)

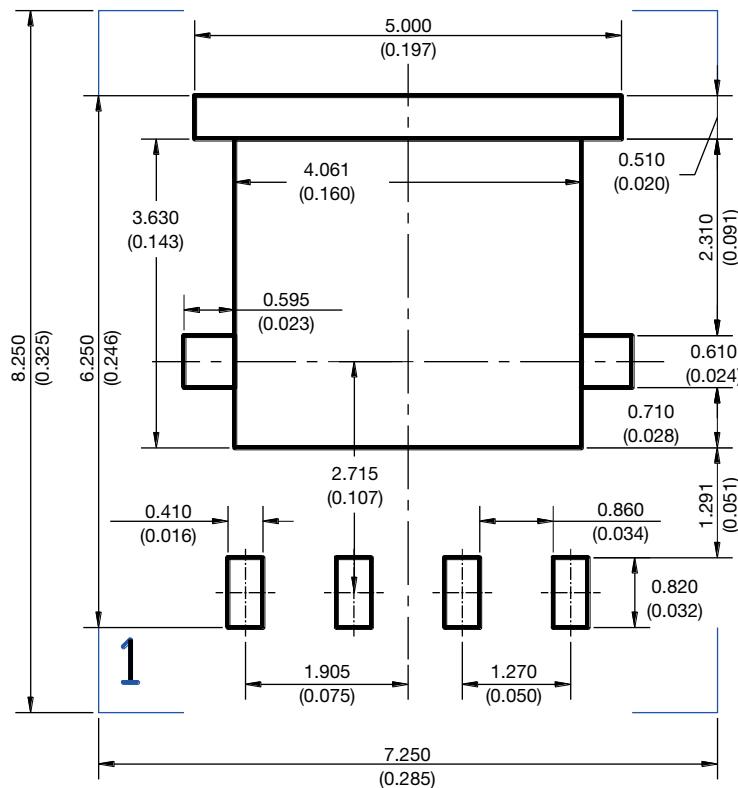
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
q	0°	-	10°	0°	-	10°

ECN: C15-1203-Rev. A, 07-Sep-15

DWG: 6044

Note

- Millimeters will govern

RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE


Recommended Minimum Pads
Dimensions in mm (inches)

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