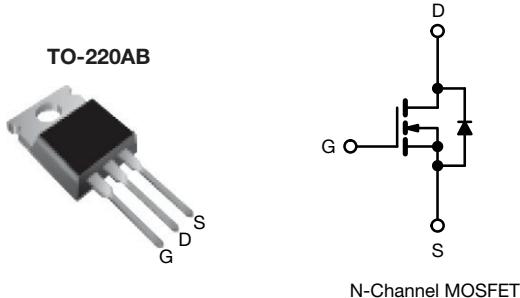


## E Series Power MOSFET with Fast Body Diode

PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	700
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V 0.102
$Q_g$ max. (nC)	146
$Q_{gs}$ (nC)	21
$Q_{gd}$ (nC)	43
Configuration	Single



### FEATURES

- Fast body diode MOSFET using E series technology
- Reduced  $t_{rr}$ ,  $Q_{rr}$ , and  $I_{RRM}$
- Low figure-of-merit (FOM):  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Low switching losses due to reduced  $Q_{rr}$
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

- Telecommunications
  - Server and telecom power supplies
- Lighting
  - High intensity discharge (HID)
  - Light emitting diodes (LEDs)
- Consumer and computing
  - ATX power supplies
- Industrial
  - Welding
  - Battery chargers
- Renewable energy
  - Solar (PV inverters)
- Switch mode power suppliers (SMPS)
- Applications using the following topologies
  - LLC
  - Phase shifted bridge (ZVS)
  - 3-level inverter
  - AC/DC bridge

ORDERING INFORMATION			
Package		TO-220AB	
Lead (Pb)-free and halogen-free		SiHP28N65EF-GE3	

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	650	
Gate-source voltage		$V_{GS}$	$\pm 30$	V
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	28	
		$T_C = 100$ °C	18	A
Pulsed drain current <sup>a</sup>		$I_{DM}$	87	
Linear derating factor			2	W/°C
Single pulse avalanche energy <sup>b</sup>		$E_{AS}$	427	mJ
Maximum power dissipation		$P_D$	250	W
Operating junction and storage temperature range		$T_J$ , $T_{stg}$	-55 to +150	°C
Drain-source voltage slope	$T_J = 125$ °C	$dV/dt$	70	V/ns
Reverse diode $dV/dt$ <sup>d</sup>			11	
Soldering recommendations (peak temperature) <sup>c</sup>	for 10 s		300	°C

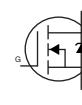
### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$  Ω,  $I_{AS} = 5.5$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/μs, starting  $T_J = 25$  °C

**THERMAL RESISTANCE RATINGS**

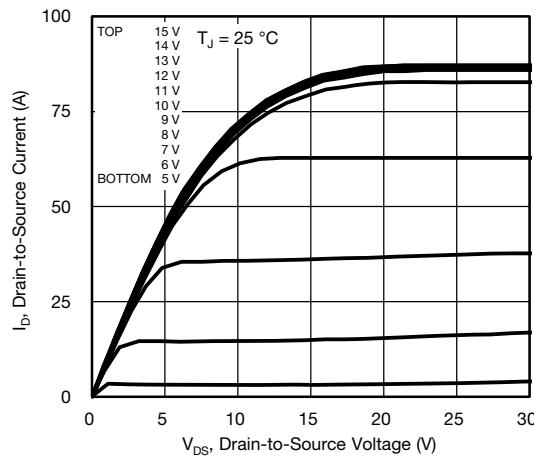
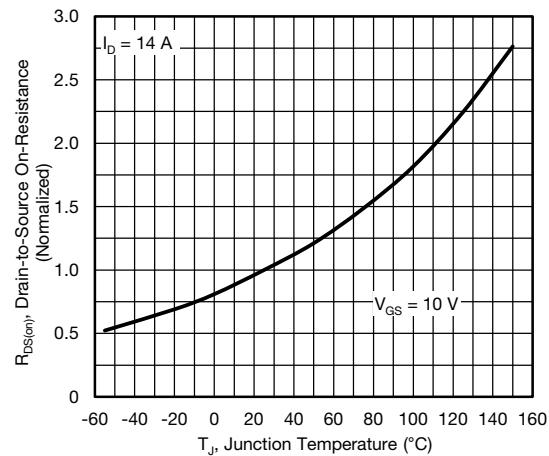
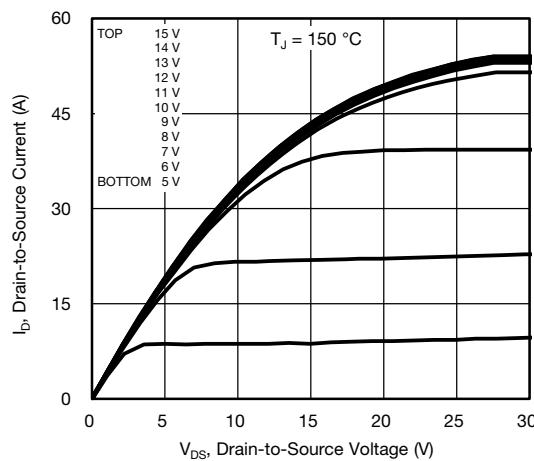
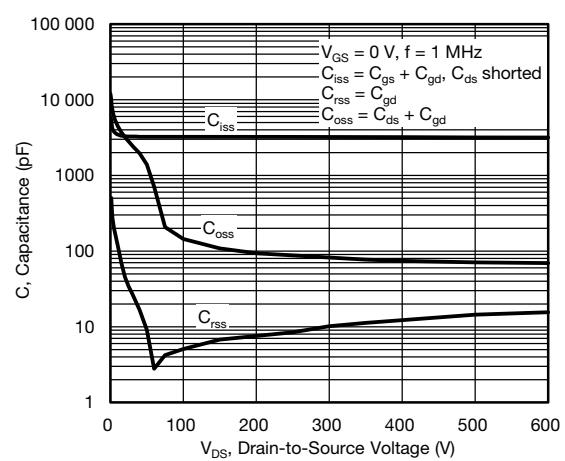
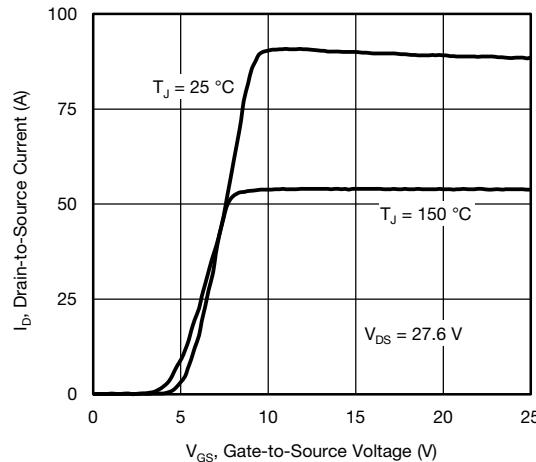
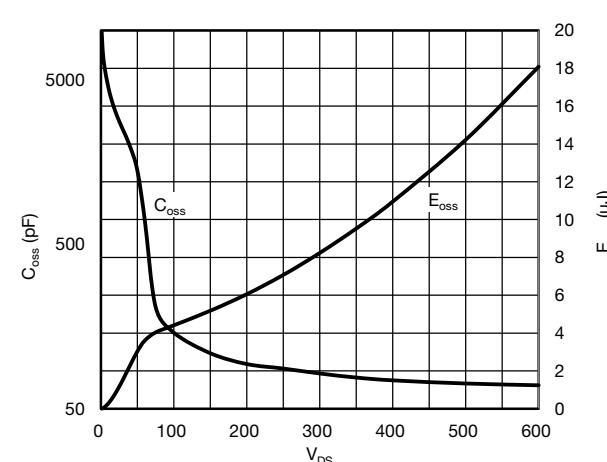
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.5	

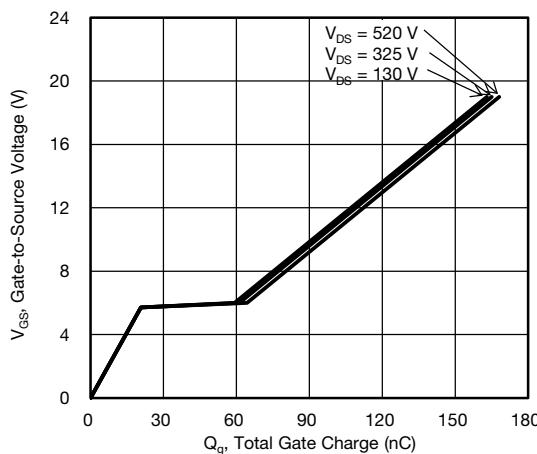
**SPECIFICATIONS (T<sub>J</sub> = 25 °C, unless otherwise noted)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$		650	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 10 \text{ mA}$		-	0.74	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30 \text{ V}$		-	-	± 1	μA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 520 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	1	μA
		$V_{DS} = 520 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125 \text{ °C}$		-	-	500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 14 \text{ A}$	-	0.102	0.117	Ω
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 30 \text{ V}$ , $I_D = 14 \text{ A}$		-	11	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 100 \text{ V}$ , $f = 1 \text{ MHz}$		-	3249	-	pF
Output capacitance	$C_{oss}$			-	145	-	
Reverse transfer capacitance	$C_{rss}$			-	5	-	
Effective output capacitance, energy related <sup>a</sup>	$C_{o(er)}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 0 \text{ V}$ to 520 V		-	105	-	pF
Effective output capacitance, time related <sup>b</sup>	$C_{o(tr)}$		-	441	-		
Total gate charge	$Q_g$	$V_{GS} = 10 \text{ V}$	$I_D = 14 \text{ A}$ , $V_{DS} = 520 \text{ V}$	-	97	146	nC
Gate-source charge	$Q_{gs}$			-	21	-	
Gate-drain charge	$Q_{gd}$			-	43	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 520 \text{ V}$ , $I_D = 14 \text{ A}$ $R_g = 9.1 \Omega$ , $V_{GS} = 10 \text{ V}$		-	29	58	ns
Rise time	$t_r$			-	44	88	
Turn-off delay time	$t_{d(off)}$			-	93	140	
Fall time	$t_f$			-	51	102	
Gate input resistance	$R_g$	$f = 1 \text{ MHz}$ , open drain		0.25	0.5	1.0	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	28	A
Pulsed diode forward current	$I_{SM}$			-	-	87	
Diode forward voltage	$V_{SD}$	$T_J = 25 \text{ °C}$ , $I_S = 11 \text{ A}$ , $V_{GS} = 0 \text{ V}$		-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$T_J = 25 \text{ °C}$ , $I_F = I_S = 14 \text{ A}$ , $dl/dt = 100 \text{ A}/\mu\text{s}$ , $V_R = 400 \text{ V}$		-	174	308	ns
Reverse recovery charge	$Q_{rr}$			-	1.1	2.4	μC
Reverse recovery current	$I_{RRM}$			-	15	-	A

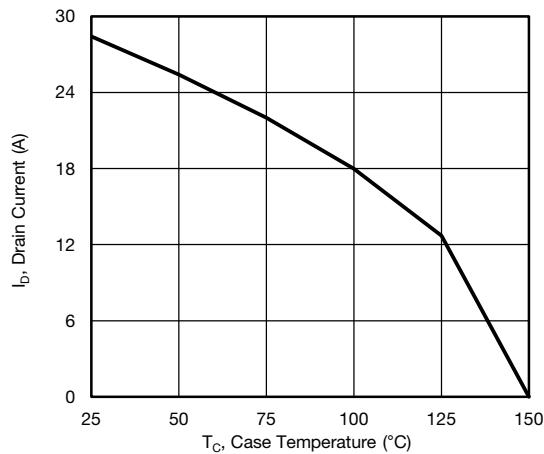
**Notes**

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$   
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$

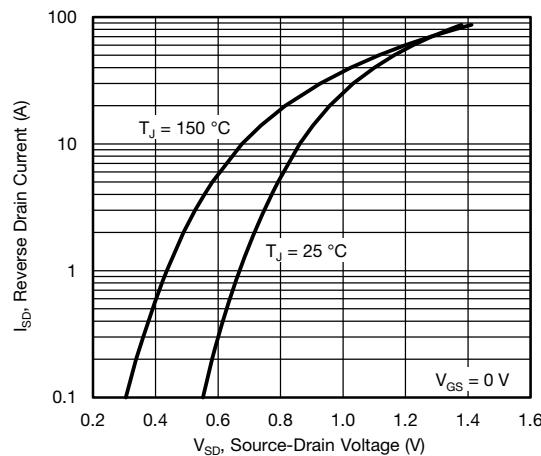
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**



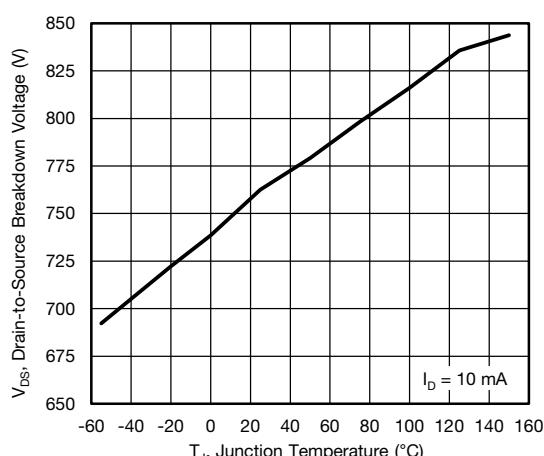
**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**



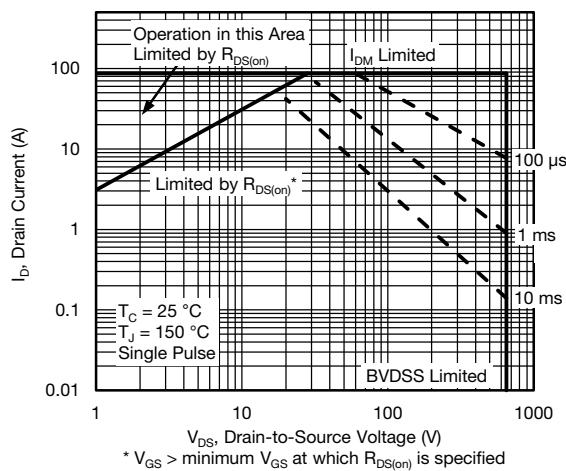
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



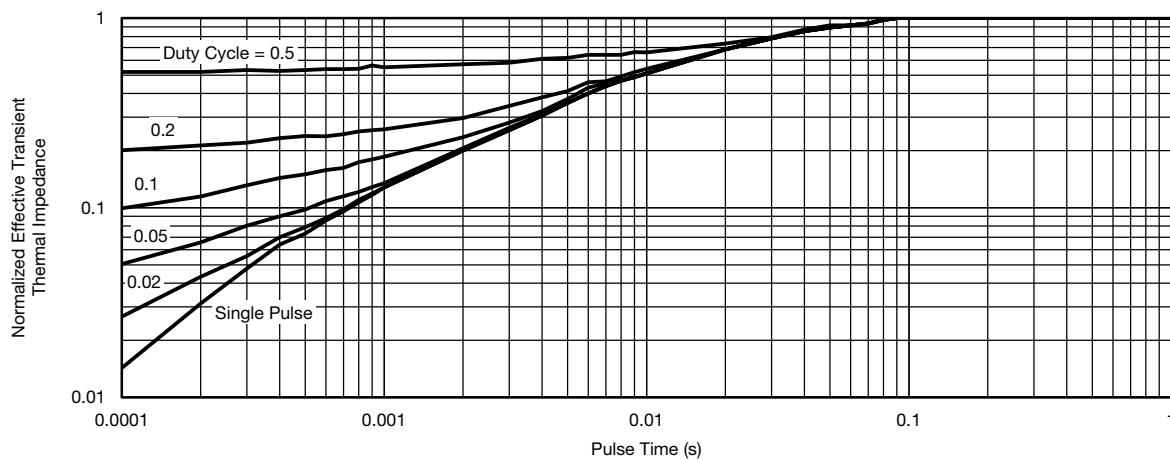
**Fig. 8 - Typical Source-Drain Diode Forward Voltage**



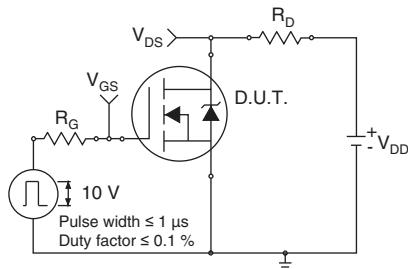
**Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature**



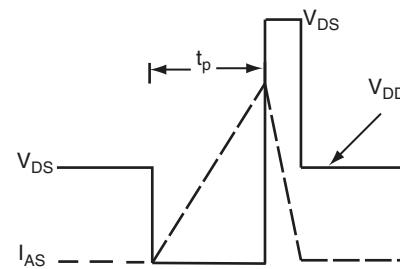
**Fig. 9 - Maximum Safe Operating Area**



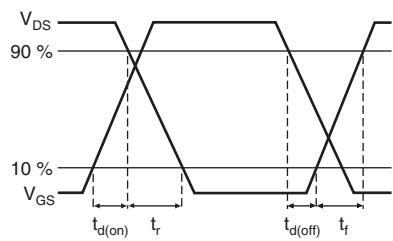
**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**



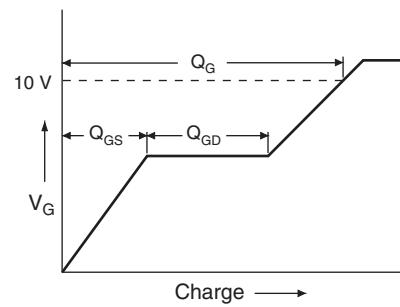
**Fig. 13 - Switching Time Test Circuit**



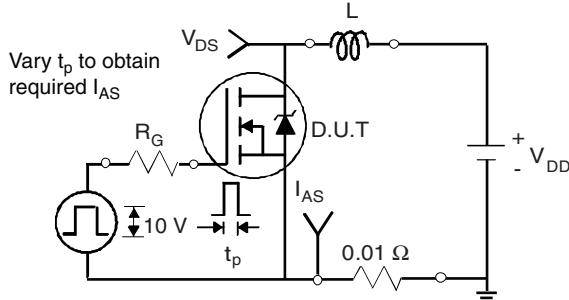
**Fig. 16 - Unclamped Inductive Waveforms**



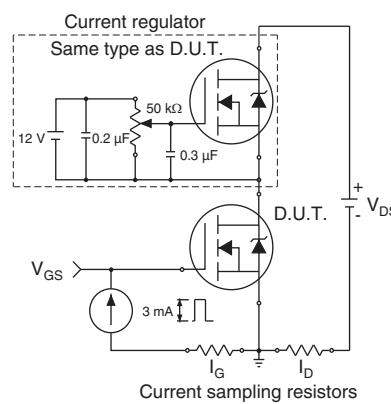
**Fig. 14 - Switching Time Waveforms**



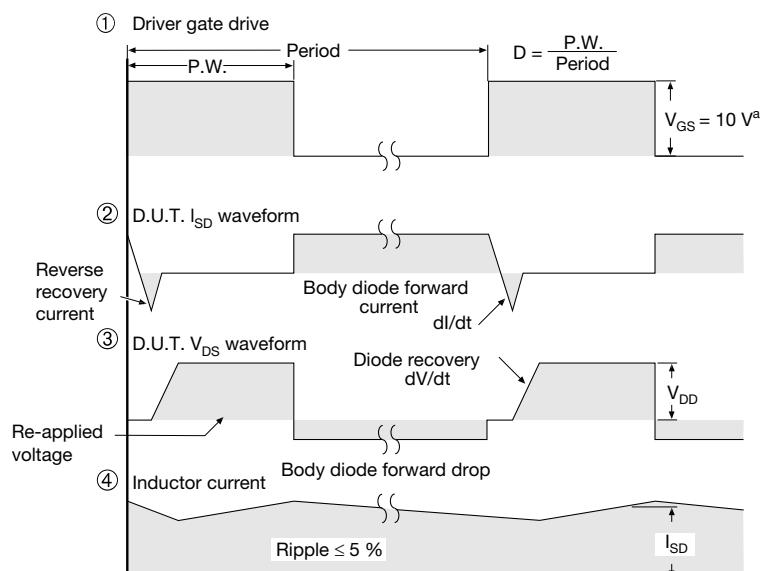
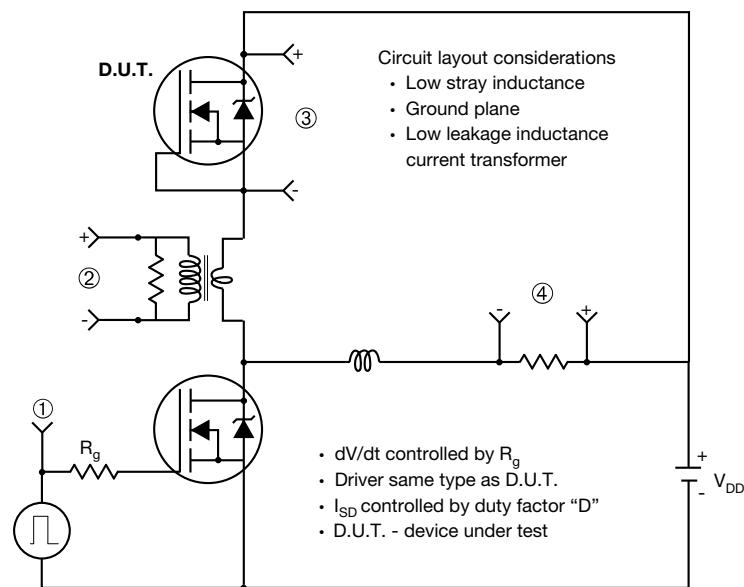
**Fig. 17 - Basic Gate Charge Waveform**



**Fig. 15 - Unclamped Inductive Test Circuit**



**Fig. 18 - Gate Charge Test Circuit**

**Peak Diode Recovery  $dV/dt$  Test Circuit**

**Fig. 19 - For N-Channel**

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