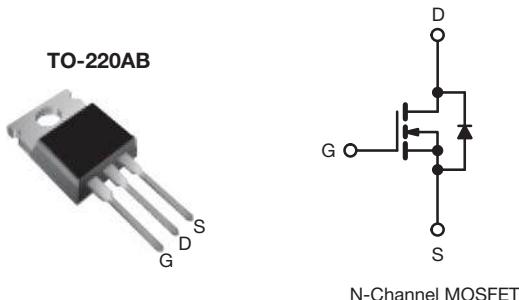


E Series Power MOSFET with Fast Body Diode and Low Gate Charge

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	650
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V 0.127
Q_g (Max.) (nC)	75
Q_{gs} (nC)	17
Q_{gd} (nC)	19
Configuration	Single



FEATURES

- Reduced figure-of-merit (FOM): $R_{on} \times Q_g$
- Fast body diode MOSFET using E series technology
- Reduced t_{rr} , Q_{rr} , and I_{RRM}
- Increased robustness due to low Q_{rr}
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Telecommunications
 - Server and telecom power supplies
- Computing
 - ATX power supplies
- Industrial
 - Welding
 - Induction heating
 - Battery chargers
 - Uninterruptible power supplies (UPS)
- Renewable energy
 - String PV inverters

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free and Halogen-free	SiHP25N60EFL-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	25	A
			16	
Pulsed Drain Current ^a		I_{DM}	61	W/°C
Linear Derating Factor			2	
Single Pulse Avalanche Energy ^b		E_{AS}	353	mJ
Maximum Power Dissipation		P_D	250	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	$V_{DS} = 0$ V to 80 % V_{DS}	dV/dt	70	V/ns
Reverse Diode dV/dt ^d			15	
Soldering Recommendations (Peak temperature) ^c	for 10 s		300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 5$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS

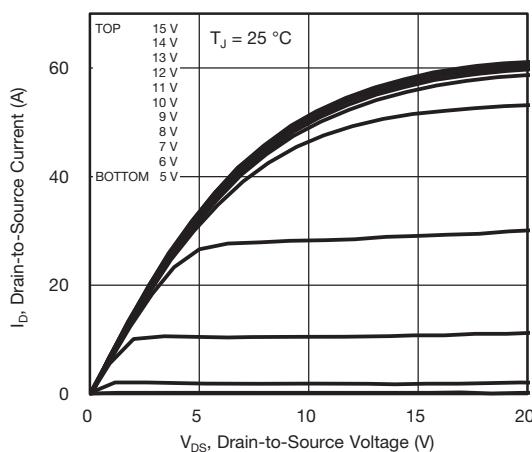
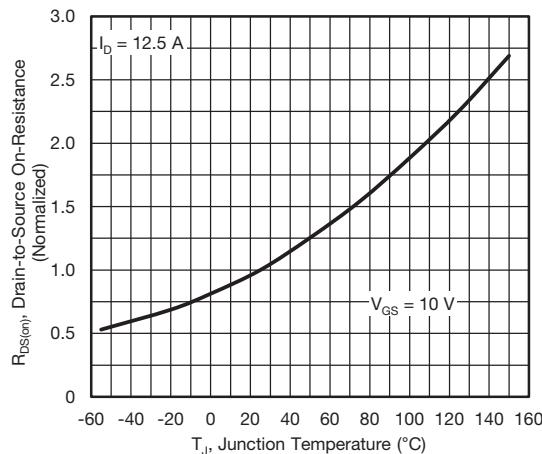
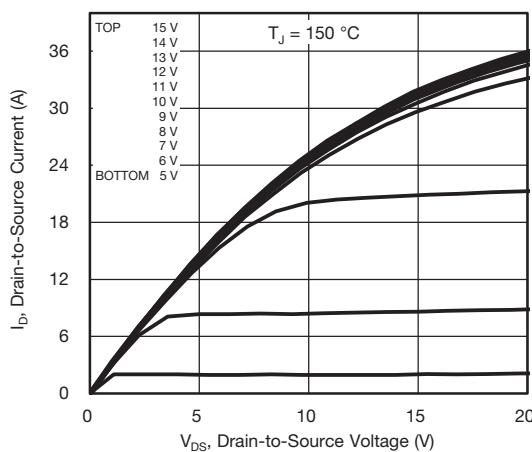
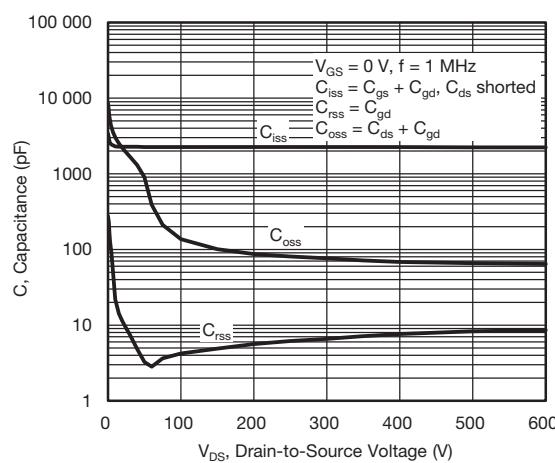
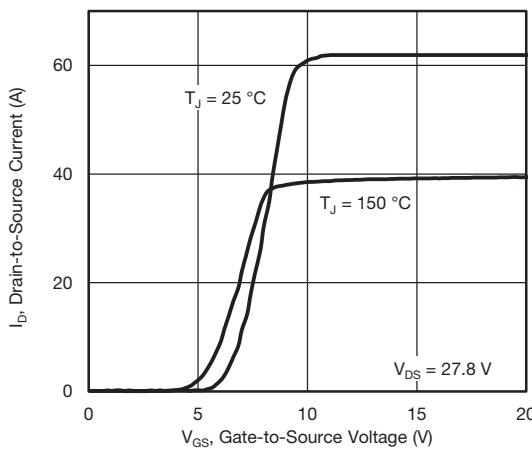
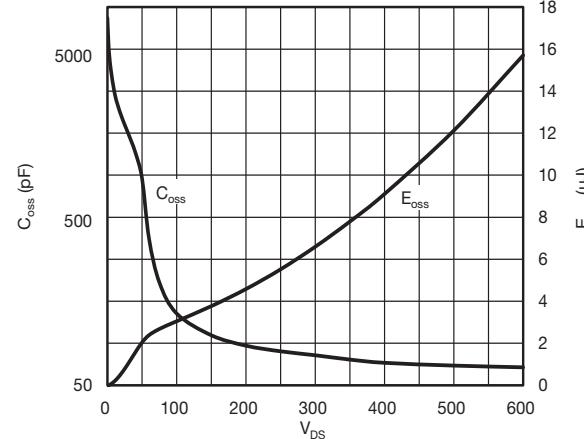
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.5	

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 10\text{ mA}$		-	0.69	-	$\text{V}/^\circ\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 12.5\text{ A}$	-	0.127	0.146	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 12.5\text{ A}$		-	11.3	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$		-	2274	-	pF
Output Capacitance	C_{oss}			-	137	-	
Reverse Transfer Capacitance	C_{rss}			-	4	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V}$ to 480 V , $V_{GS} = 0\text{ V}$		-	79	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	330	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 12.5\text{ A}$, $V_{DS} = 480\text{ V}$	-	50	75	nC
Gate-Source Charge	Q_{gs}			-	17	-	
Gate-Drain Charge	Q_{gd}			-	19	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$, $I_D = 12.5\text{ A}$, $R_g = 9.1\text{ }\Omega$, $V_{GS} = 10\text{ V}$		-	25	50	ns
Rise Time	t_r			-	39	68	
Turn-Off Delay Time	$t_{d(off)}$			-	47	94	
Fall Time	t_f			-	21	42	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain		0.4	0.7	1.4	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	25	A
Pulsed Diode Forward Current	I_{SM}			-	-	61	
Diode Forward Voltage	V_{SD}	$T_J = 25^\circ\text{C}$, $I_S = 12.5\text{ A}$, $V_{GS} = 0\text{ V}$		-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_F = I_S = 12.5\text{ A}$, $dl/dt = 100\text{ A}/\mu\text{s}$, $V_R = 25\text{ V}$		-	138	276	ns
Reverse Recovery Charge	Q_{rr}			-	0.8	1.6	μC
Reverse Recovery Current	I_{RRM}			-	11	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

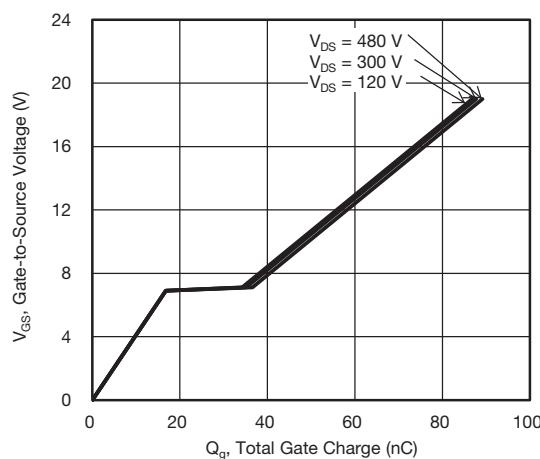


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

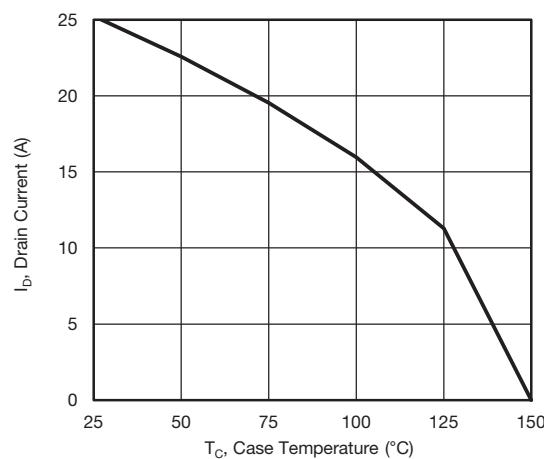


Fig. 10 - Maximum Drain Current vs. Case Temperature

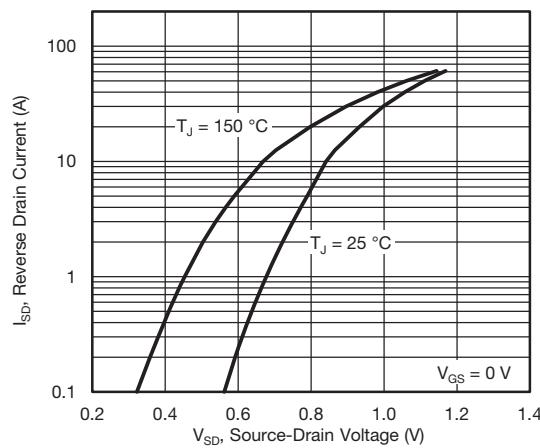


Fig. 8 - Typical Source-Drain Diode Forward Voltage

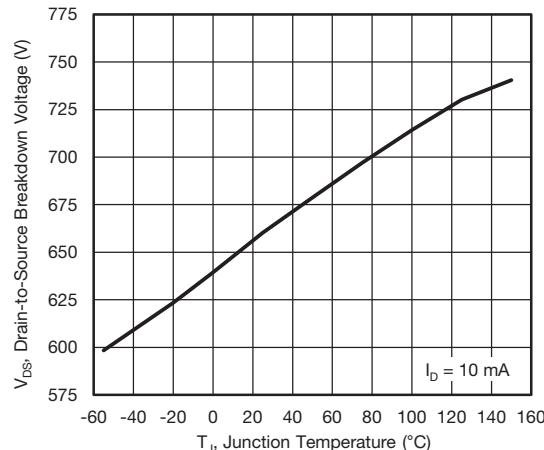


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

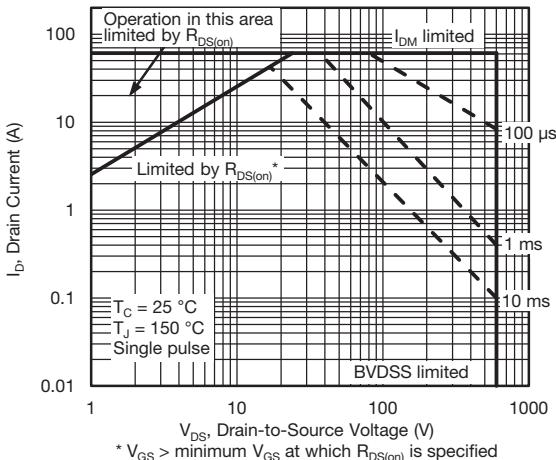


Fig. 9 - Maximum Safe Operating Area

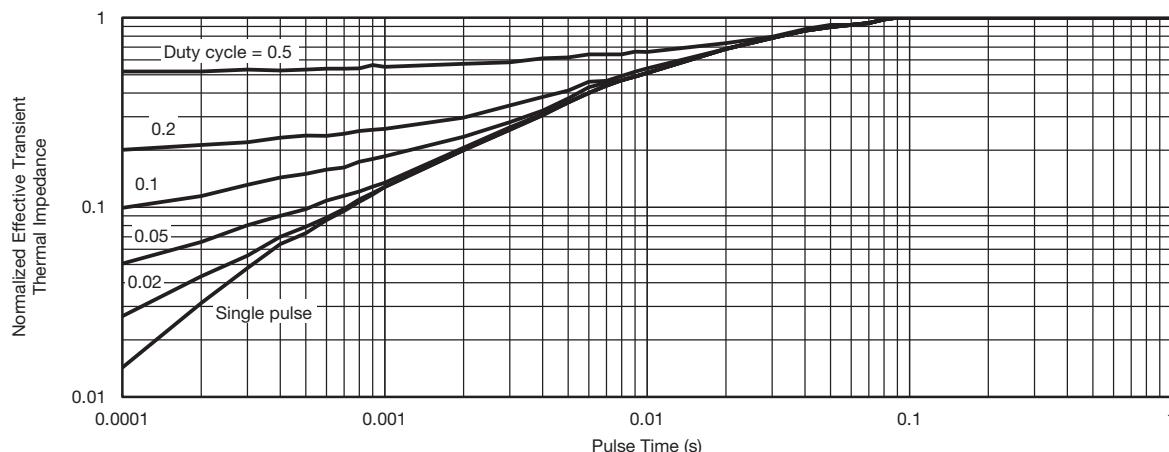


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

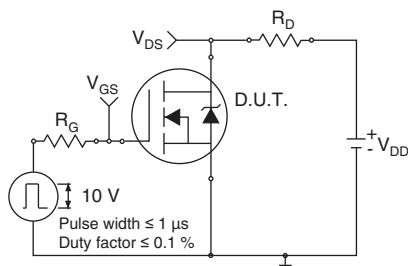


Fig. 13 - Switching Time Test Circuit

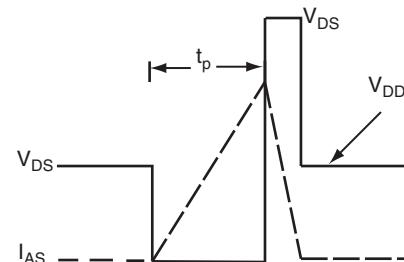


Fig. 16 - Unclamped Inductive Waveforms

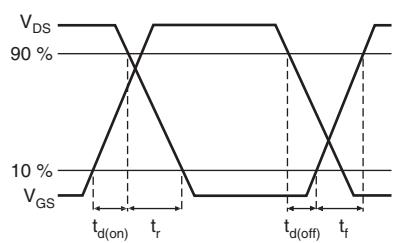


Fig. 14 - Switching Time Waveforms

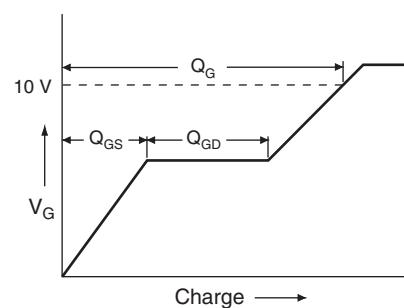


Fig. 17 - Basic Gate Charge Waveform

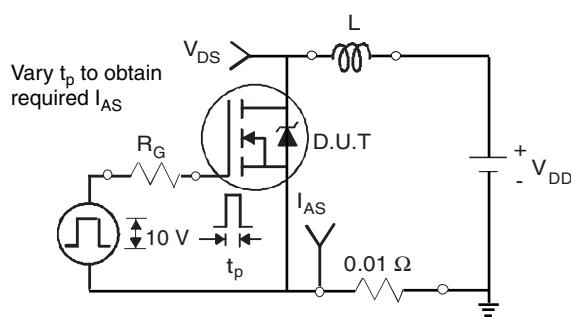


Fig. 15 - Unclamped Inductive Test Circuit

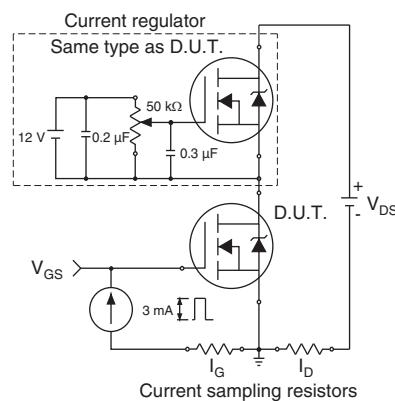
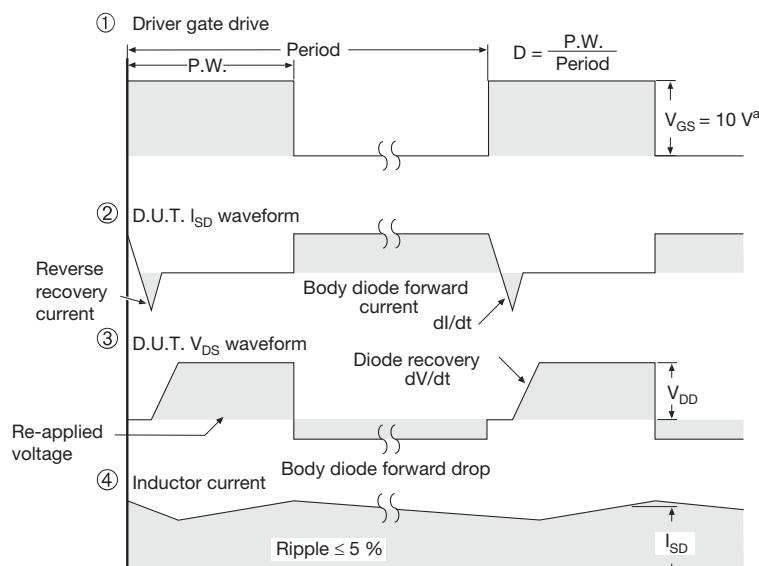
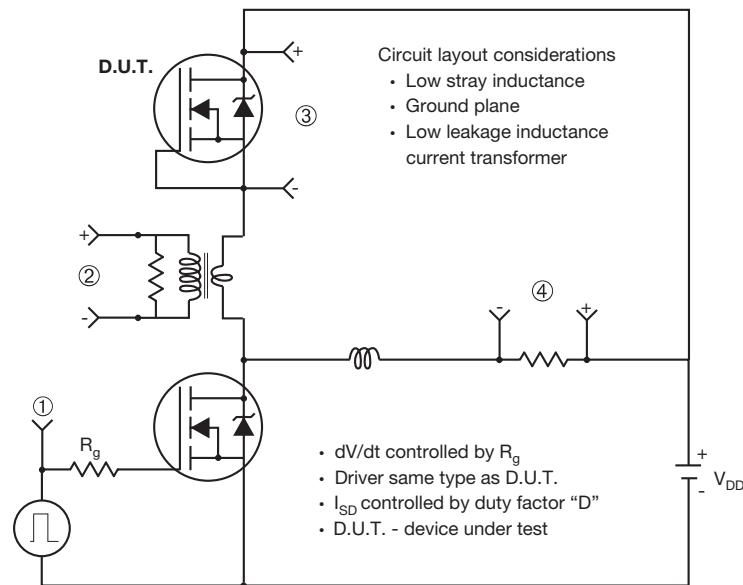


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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