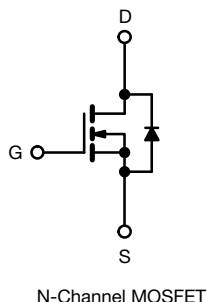
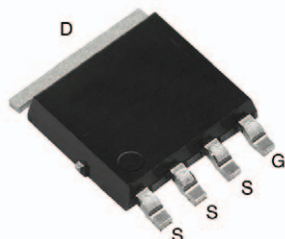


# E Series Power MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	700	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.520
$Q_g$ max. (nC)	44	
$Q_{gs}$ (nC)	6	
$Q_{gd}$ (nC)	9	
Configuration	Single	

PowerPAK® SO-8L Single



## FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## APPLICATIONS

- Switch mode power supplies (SMPS)
- Flyback converter
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Consumer
  - Wall adaptors

## ORDERING INFORMATION

Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SiHJ7N65E-T1-GE3

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	17	
Linear Derating Factor		0.77	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	68	mJ
Maximum Power Dissipation	$P_D$	96	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	°C
Drain-Source Voltage Slope	$dV/dt$	70	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>		14	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 120$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 2.2$  A.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.

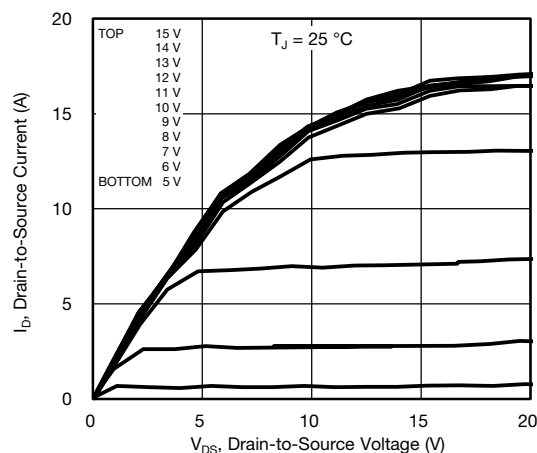
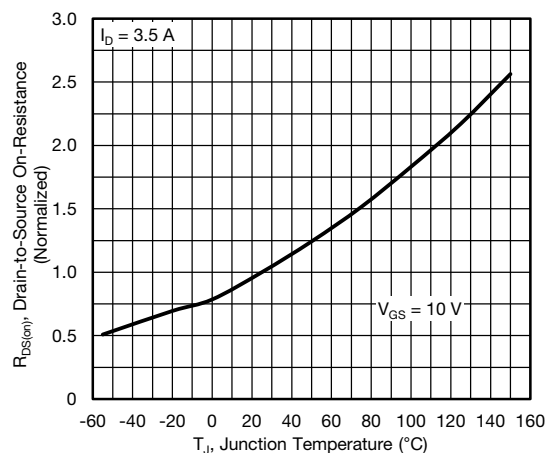
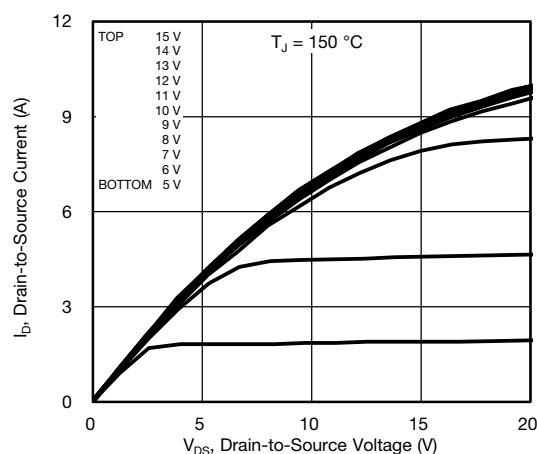
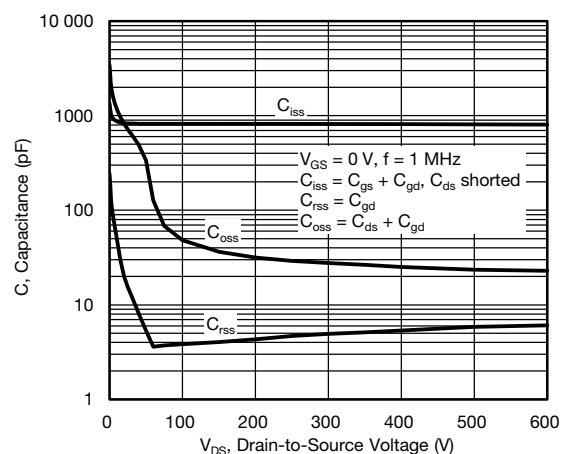
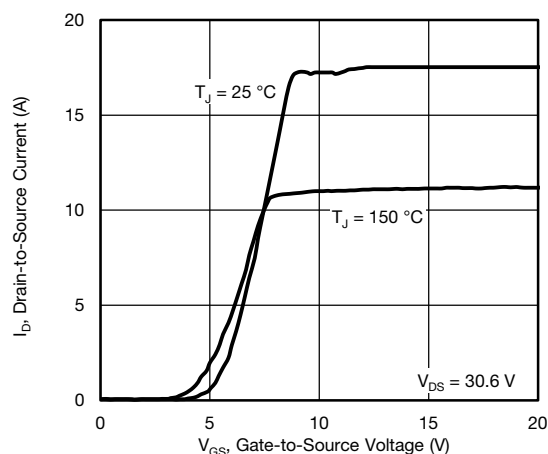
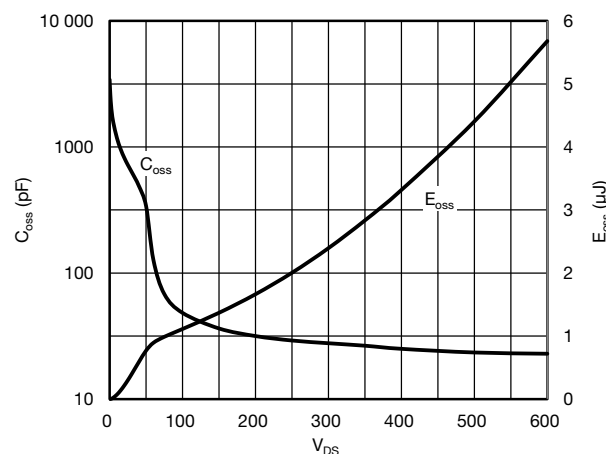
## THERMAL RESISTANCE RATINGS

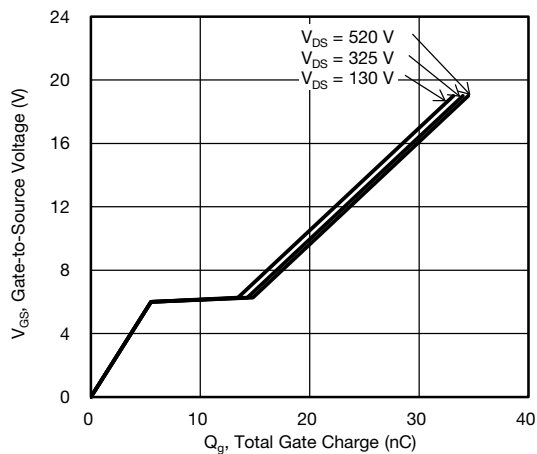
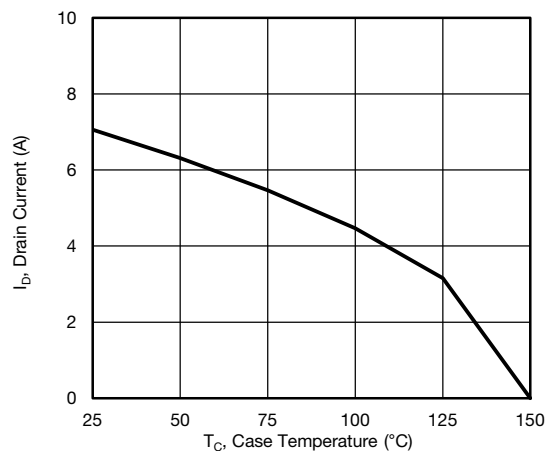
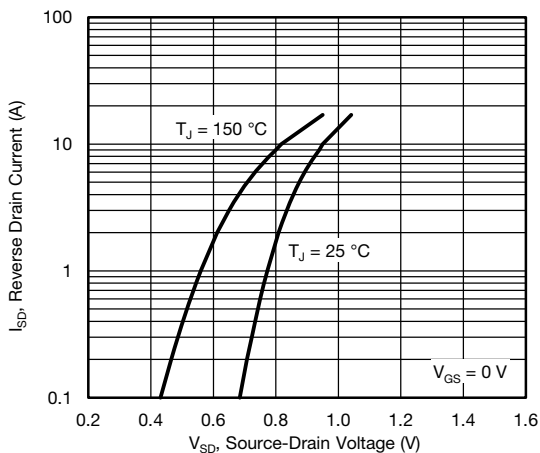
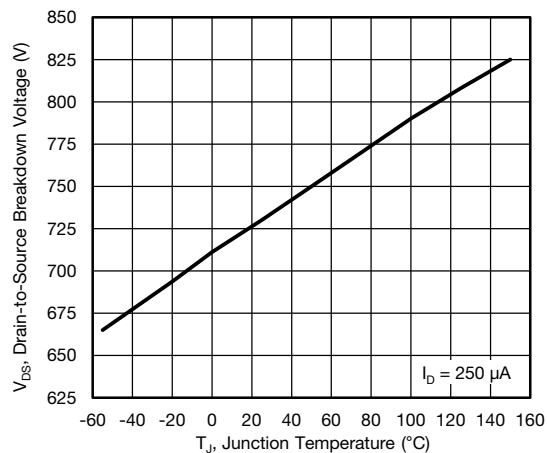
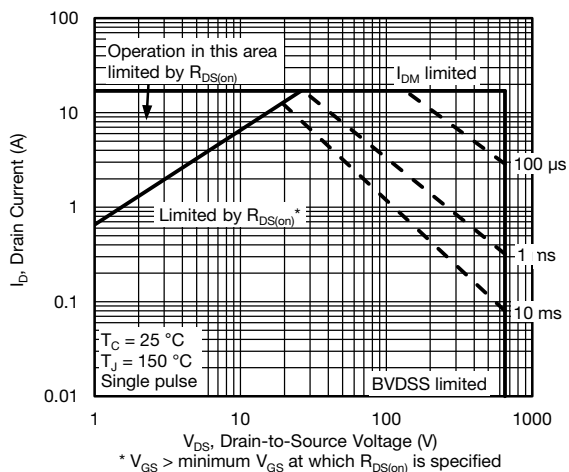
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	52	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	1.0	1.3	

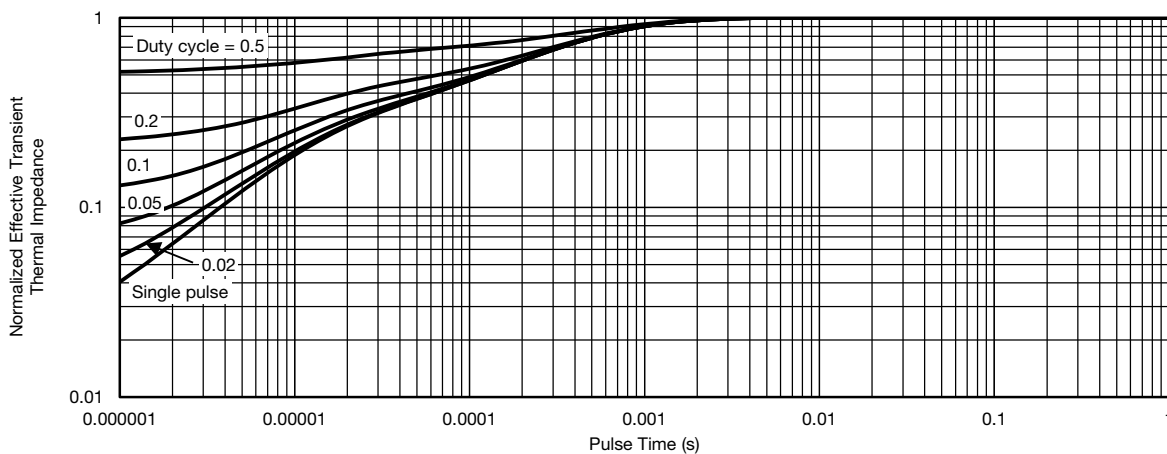
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.8	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	10	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.5 A	-	0.520	0.598	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 3.5 A		-	2.3	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	820	-	pF
Output Capacitance	C <sub>oss</sub>			-	48	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	4	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 520 V, V <sub>GS</sub> = 0 V		-	33	-	
Effective Output Capacitance, Time Related <sup>b</sup>	C <sub>o(tr)</sub>			-	118	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.5 A, V <sub>DS</sub> = 520 V	-	22	44	nC
Gate-Source Charge	Q <sub>gs</sub>			-	6	-	
Gate-Drain Charge	Q <sub>gd</sub>			-	9	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 3.5 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	16	32	ns
Rise Time	t <sub>r</sub>			-	18	36	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	30	60	
Fall Time	t <sub>f</sub>			-	18	36	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz		0.4	0.8	1.6	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	7.9	A
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	17	
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 3.5 A, V <sub>GS</sub> = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 3.5 A, di/dt = 100 A/μs, V <sub>R</sub> = 25 V		-	299	598	ns
Reverse Recovery Charge	Q <sub>rr</sub>			-	2.9	5.8	μC
Reverse Recovery Current	I <sub>RRM</sub>			-	16	-	A

**Notes**

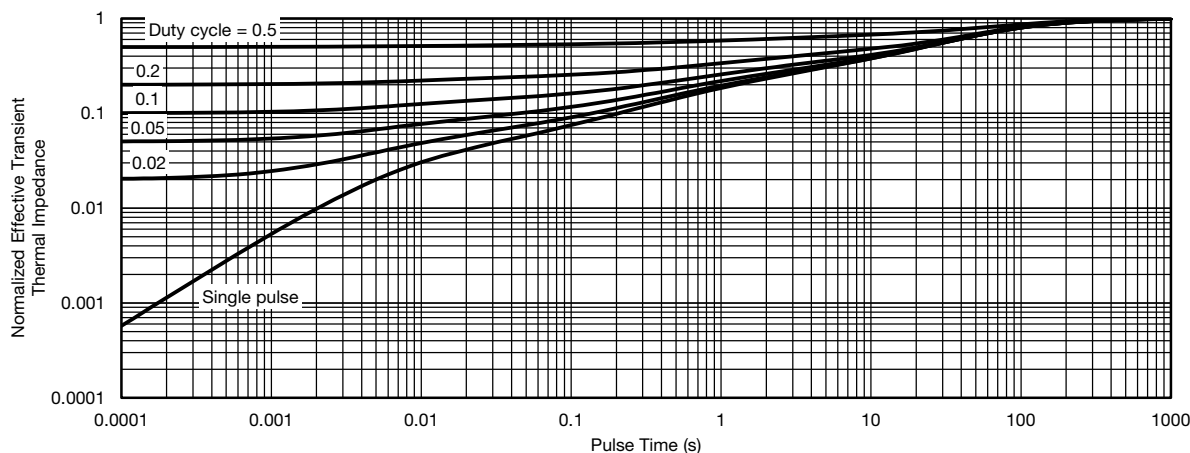
- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .  
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**

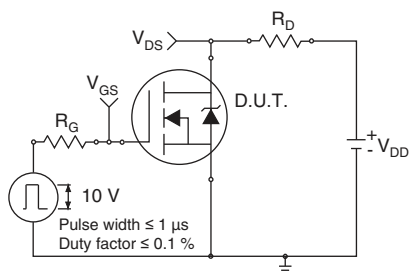

**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 10 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

**Fig. 11 - Temperature vs. Drain-to-Source Voltage**

**Fig. 9 - Maximum Safe Operating Area**



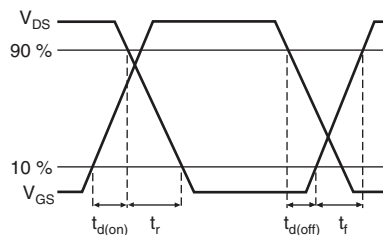
**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**



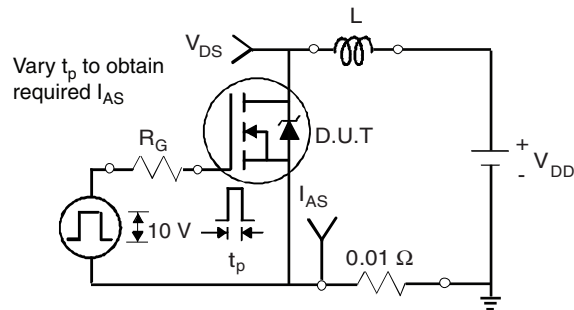
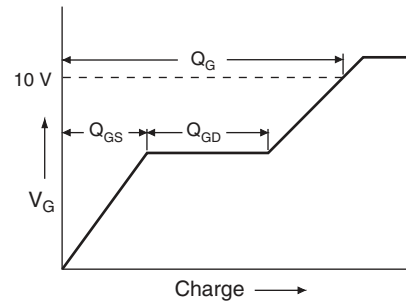
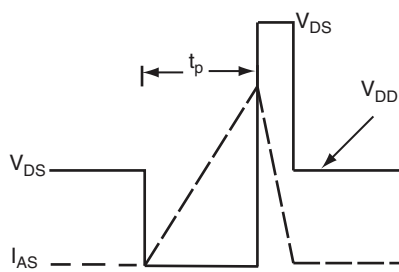
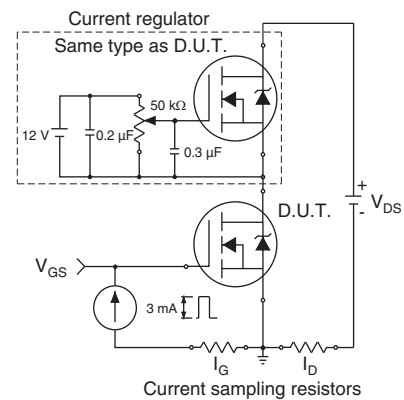
**Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient**

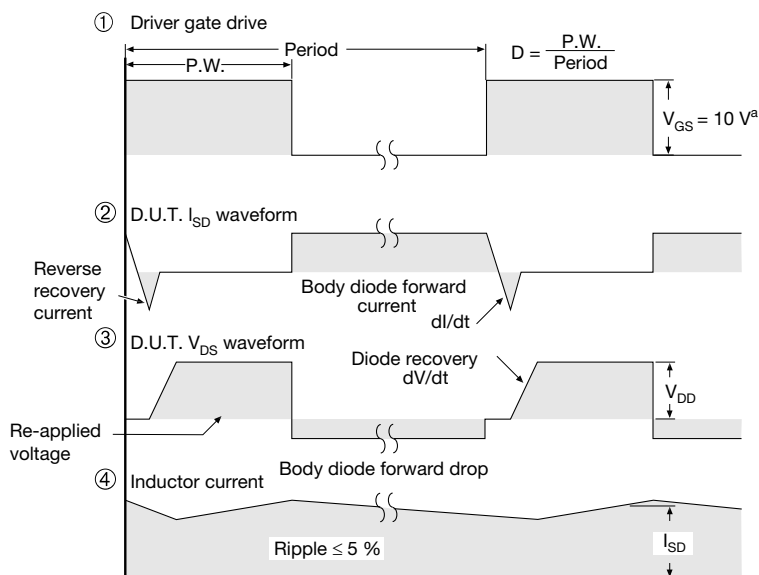
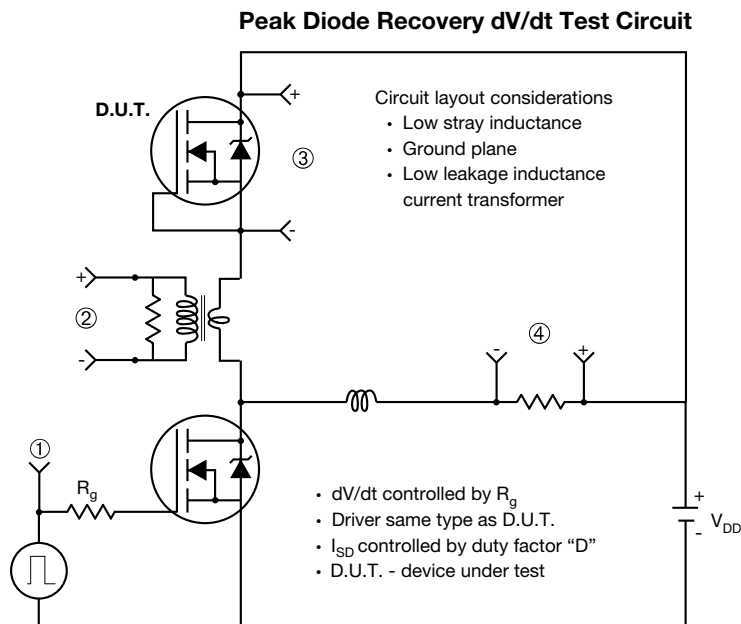


**Fig. 14 - Switching Time Test Circuit**



**Fig. 15 - Switching Time Waveforms**


**Fig. 16 - Unclamped Inductive Test Circuit**

**Fig. 18 - Basic Gate Charge Waveform**

**Fig. 17 - Unclamped Inductive Waveforms**

**Fig. 19 - Gate Charge Test Circuit**



**Note**

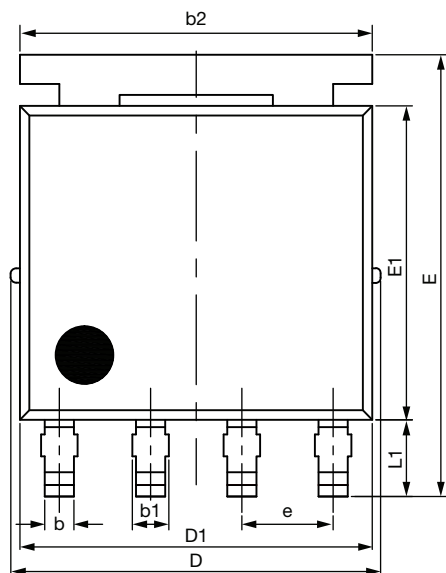
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 20 - For N-Channel**

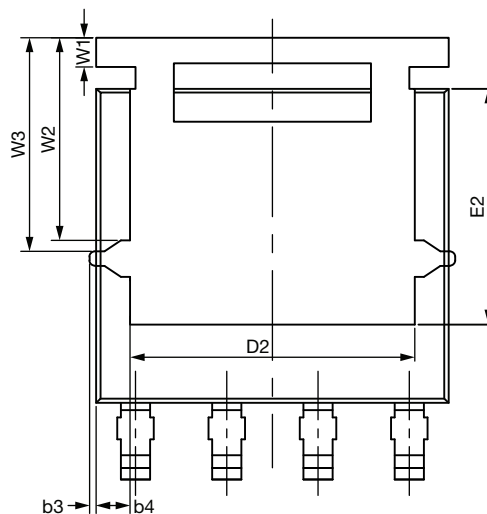
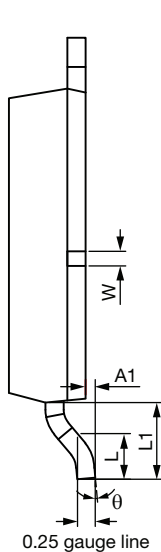
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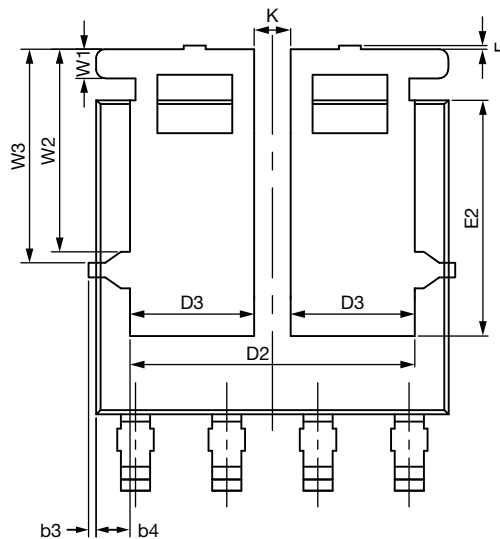
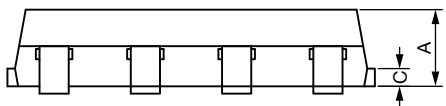
## PowerPAK® SO-8L Case Outline for Non-AI Parts



Topside view



Backside view (single)



Backside view (dual)





DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: T16-0221-Rev. D, 16-May-16 DWG: 5976						

**Note**

- Millimeters will govern



## RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads  
Dimensions in mm (inches)



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