

N-Channel 30-V (D-S) MOSFET

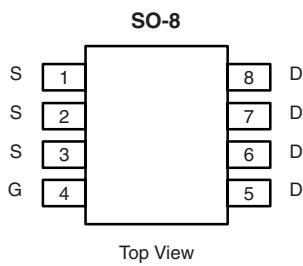
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
30	0.0046 at $V_{GS} = 10$ V	19.8	36 nC
	0.0054 at $V_{GS} = 4.5$ V	18.2	

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- Optimized for "Low Side" Synchronous Rectifier Operation
- 100 % R_g Tested

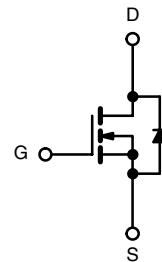


RoHS
COMPLIANT
HALOGEN
FREE
Available



APPLICATIONS

- DC/DC Converters
- Synchronous Rectifiers



N-Channel MOSFET

Ordering Information: Si4362BDY-T1-E3 (Lead-(Pb)-free)
Si4362BDY-T1-GE3 (Lead-(Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150$ °C)	I_D	29	A
		23	
		19.8 ^{b, c}	
		15.8 ^{b, c}	
Pulsed Drain Current	I_{DM}	60	
Continuous Source-Drain Diode Current	I_S	6	
		2.7 ^{b, c}	
Maximum Power Dissipation	P_D	6.6	W
		4.2	
		3.0 ^{b, c}	
		2 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	34	41	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	15	19	

Notes:

- Based on $T_C = 25$ °C.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under Steady State conditions is 80 °C/W.

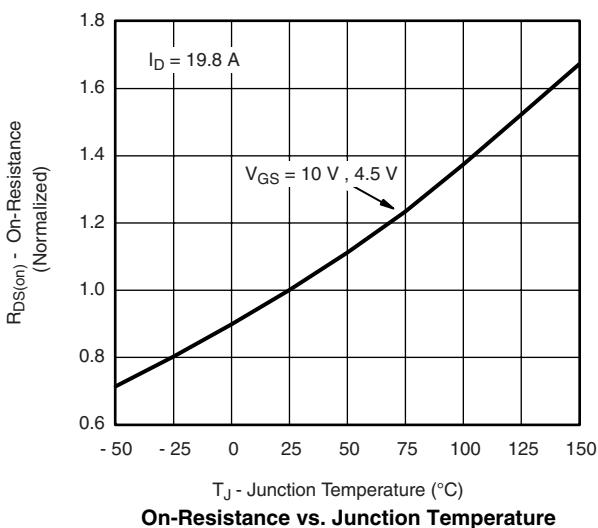
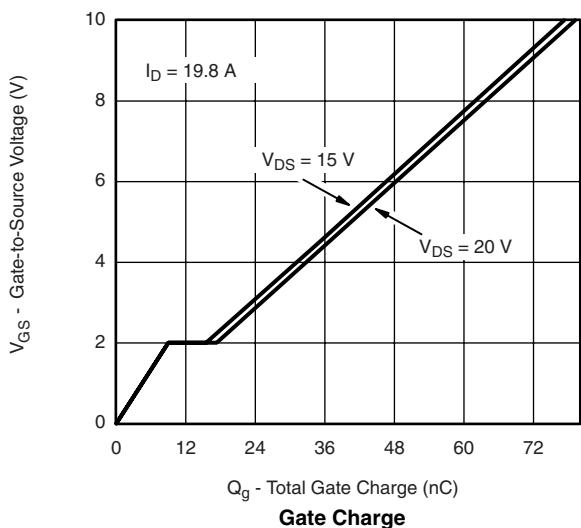
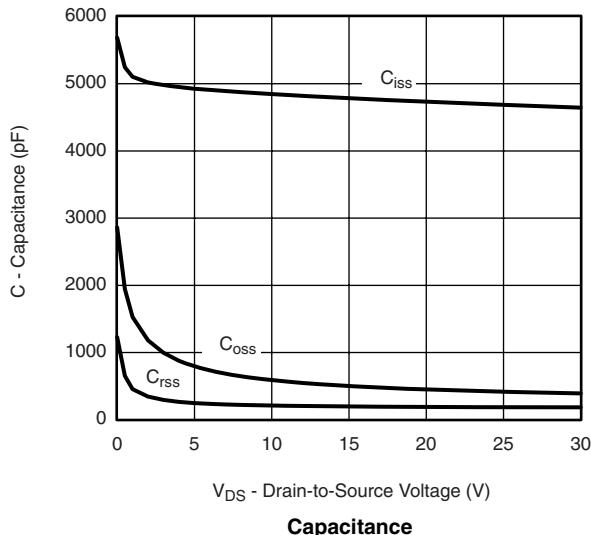
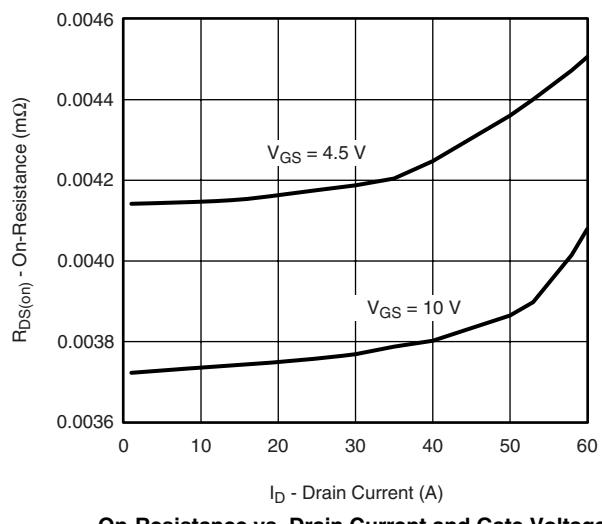
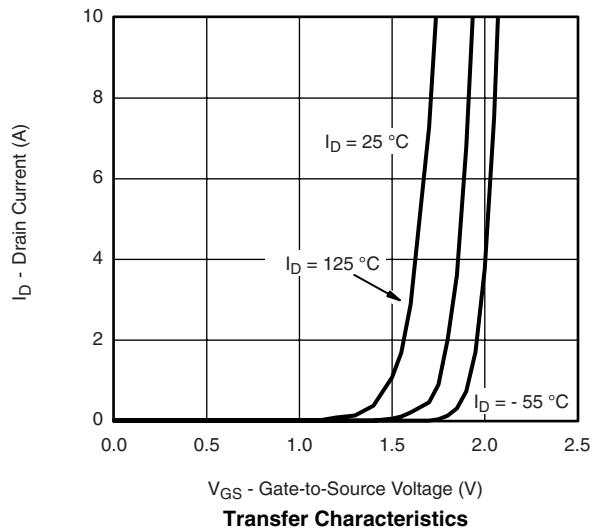
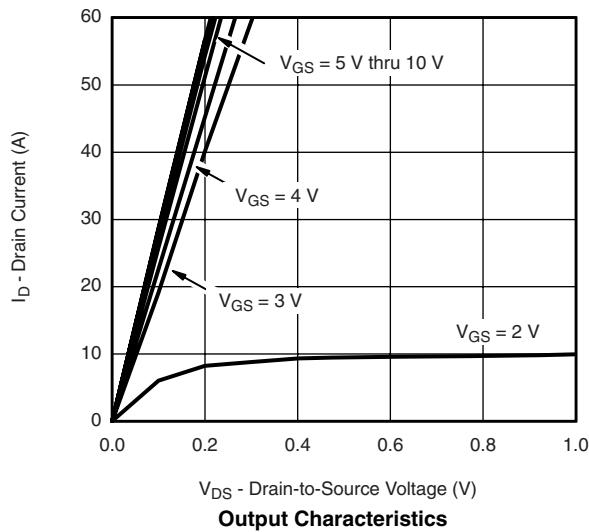
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		31.4		$\text{mV}/^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 4.9		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.6		2.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$		1		μA
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}, I_D = 19.8 \text{ A}$		0.0038	0.0046	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 18.2 \text{ A}$		0.0043	0.0054	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 19.8 \text{ A}$		120		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		4800		pF
Output Capacitance	C_{oss}			500		
Reverse Transfer Capacitance	C_{rss}			200		
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 19.8 \text{ A}$		75	115	nC
				36	54	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 19.8 \text{ A}$		9		
Gate-Drain Charge	Q_{gd}			6.5		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		1.05	1.6	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 15 \text{ V}, R_L = 1.5 \Omega$ $I_D \geq 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		26	40	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(\text{off})}$			41	65	
Fall Time	t_f			7	15	
Turn-On Delay Time	$t_{d(\text{on})}$			12	20	
Rise Time	t_r	$V_{DD} = 15 \text{ V}, R_L = 1.5 \Omega$ $I_D \geq 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		10	15	ns
Turn-Off Delay Time	$t_{d(\text{off})}$			47	70	
Fall Time	t_f			8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			6	A
Pulse Diode Forward Current ^a	I_{SM}				60	
Body Diode Voltage	V_{SD}	$I_S = 5 \text{ A}$		0.7	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		35	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			30	60	nC
Reverse Recovery Fall Time	t_a			18		ns
Reverse Recovery Rise Time	t_b			17		

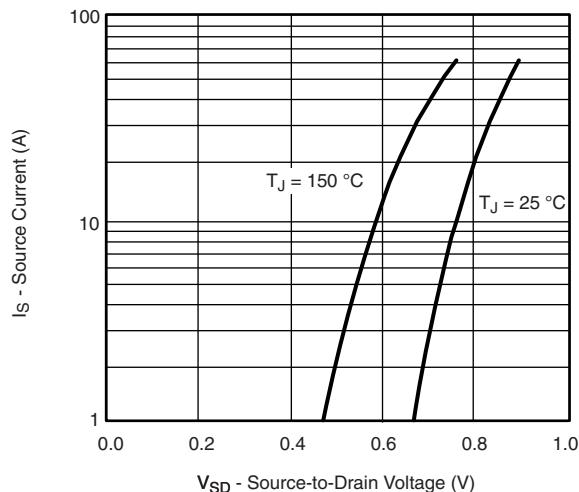
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

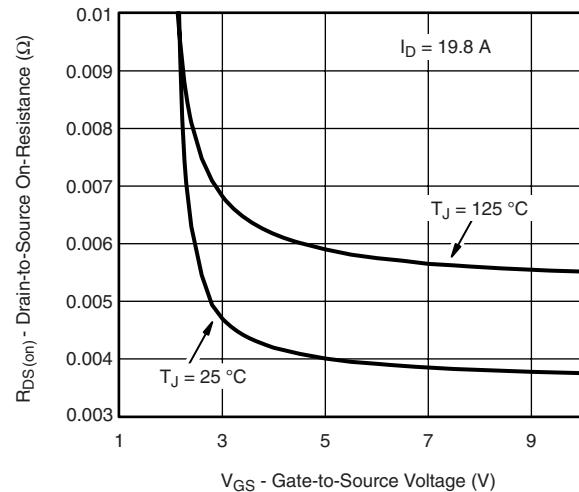
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


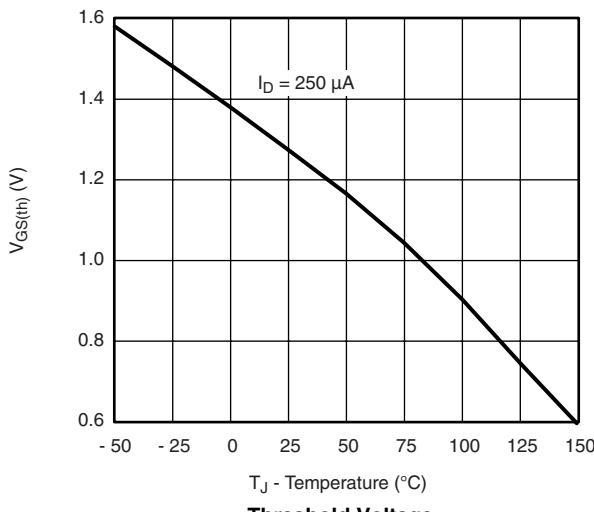
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



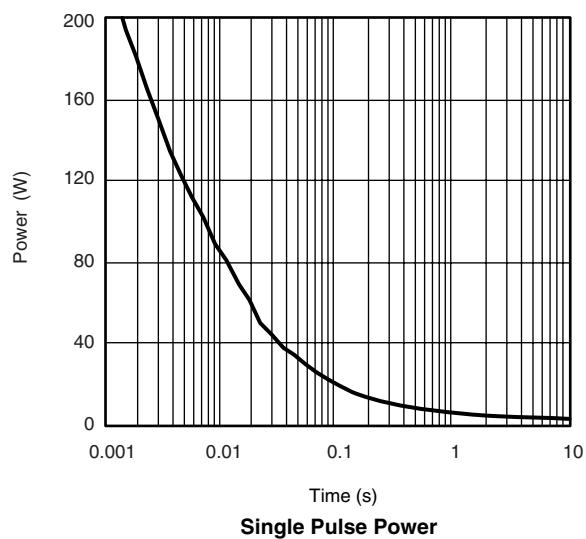
Source-Drain Diode Forward Voltage



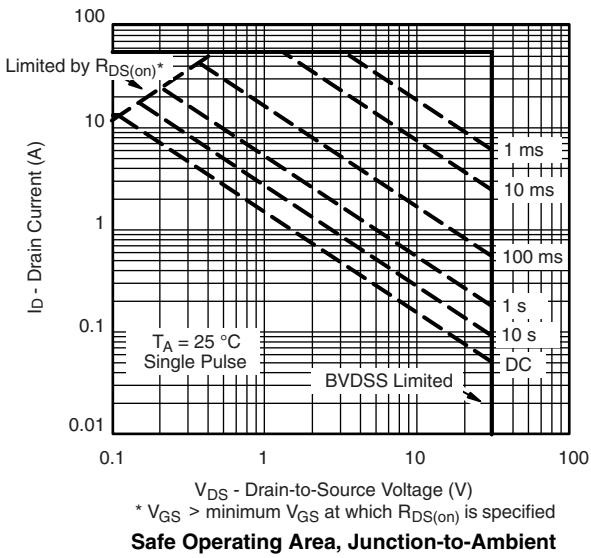
On-Resistance vs. Gate-to-Source Voltage



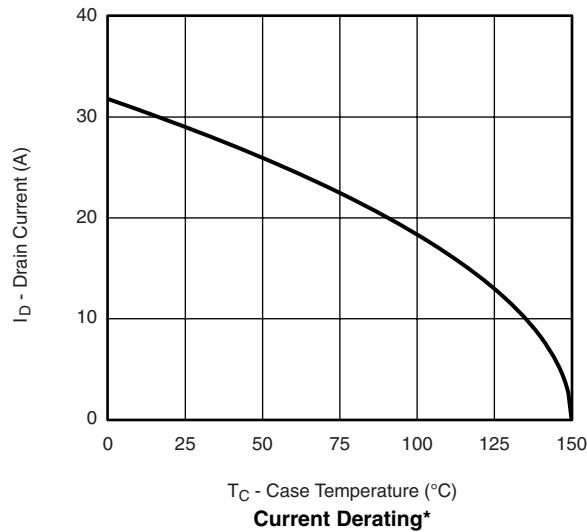
Threshold Voltage



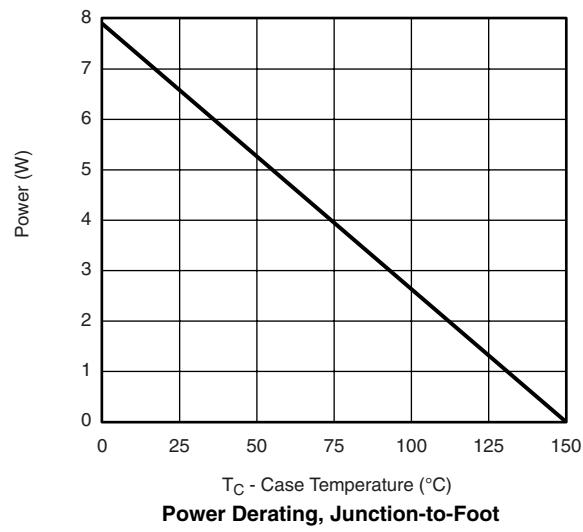
Single Pulse Power



Safe Operating Area, Junction-to-Ambient

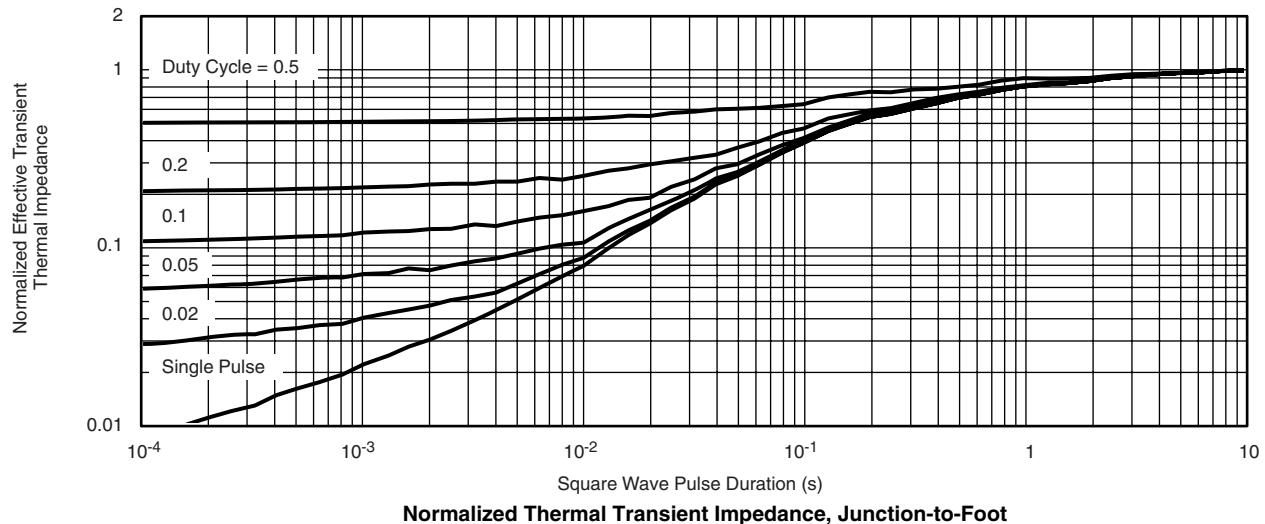
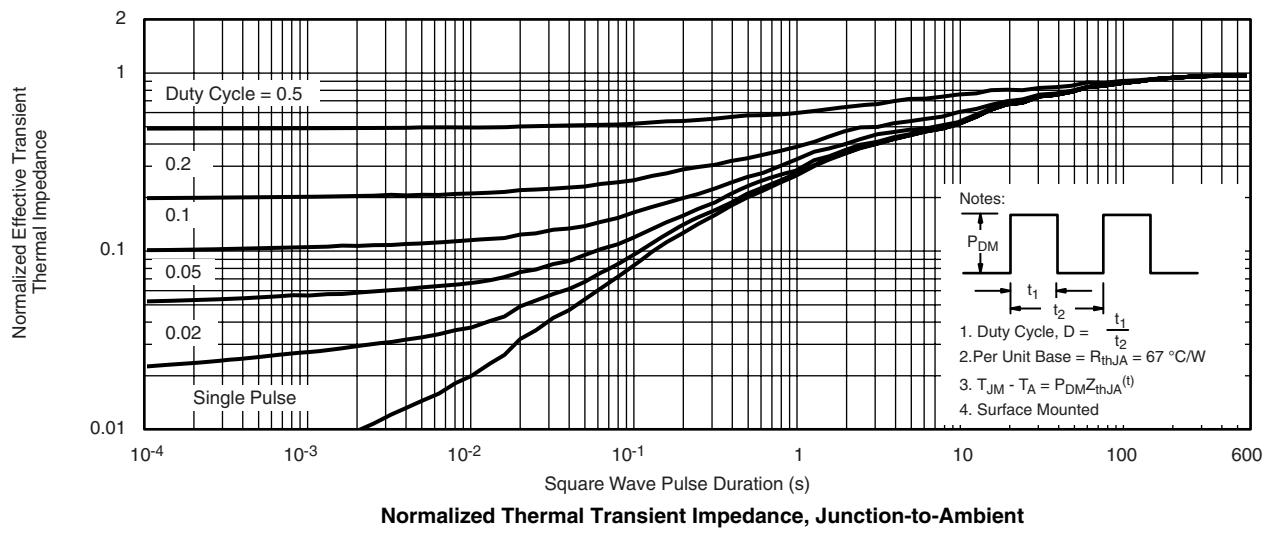
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


T_C - Case Temperature (°C)
Current Derating*



T_C - Case Temperature (°C)
Power Derating, Junction-to-Foot

* The power dissipation P_D is based on $T_{J(\max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


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