



16 Ω , Low Charge Injection and Leakage, +12 V / +5 V / +3 V / ± 5 V Quad SPST Switches

DESCRIPTION

The DG441LE, DG442LE monolithic quad single-pole-single-throw analog switches are designed to provide high speed, low error switching of analog signals. The DG441LE has a normally closed function. The DG442LE has a normally open function.

The DG441LE, DG442LE feature low charge injection of a few picocoulombs over the full analog switch range. Combining low on resistance (16 Ω , typ.), low parasitic capacitance (C_{D(ON)} 15 pF), and fast switching speed (t_{ON}, 18 ns, typ.), the devices are ideal for data acquisition, sample-and-hold, and ADC input circuit designs.

The DG441LE, DG442LE operate on single and dual supplies. Single supply voltage ranges from 3 V to 16 V while dual supply operation is recommended with \pm 3 V to \pm 8 V. Each switch conducts equally well in both direction when on, and blocks input voltages up to the supply levels when off.

The DG441LE, DG442LE are available in 16 lead TSSOP, SOIC, and PDIP packages.

FEATURES

- 3 V to 16 V single supply or \pm 3 V to \pm 8 V dual supply
- On-resistance $R_{DS(on)}$: 16 Ω
- Fast switching t_{ON}: 18 ns,typ.
- Low parasitic capacitance:

C _{D(ON)} :	15	р⊦	•
C _{S(OFF)} :	5	pF	
0(011)		÷ .	

- Less than 8 pC charge injection over the full signal swing range
- Low leakage: < 10 pA, typ.
- TTL, CMOS compatible
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

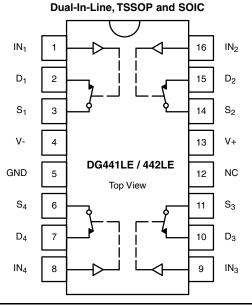
BENEFITS

- Wide operation voltage range
- Low signal errors and distortion
- Fast switching time
- Minimized switching glitch

APPLICATIONS

- · Automatic test equipment
- Process control and automation
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Audio and video signal routing
- Relay replacement
- Battery powered systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE							
LOGIC	DG441LE	DG442LE					
0	On	Off					
1	Off	On					

Logic "0" ≤ 0.8 V Logic "1" ≥ 2.4 V

S16-0392-Rev. A, 07-Mar-16

Document Number: 76754

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1 For technical questions, contact: <u>analogswitchtechsupport@vishay.com</u>

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OODERING INFORMATION								
TEMP. RANGE	CONFIGURATION	PACKAGE	PART NUMBER	MIN. ORDER / PACK. QUANTITY				
		16-pin TSSOP	DG441LEDQ-GE3	Tube 360 units				
		10-piil 1330P	DG441LEDQ-T1-GE3	Tape and reel, 3000 units				
	DG441LE	16-pin SOIC	DG441LEDY-GE3	Tube 500 units				
			DG441LEDY-T1-GE3	Tape and reel, 2500 units				
-40 °C to +85 °C		16-pin PDIP	DG441LEDJ-GE3	Tube 500 units				
Lead (Pb)-free		16-pin TSSOP	DG442LEDQ-GE3	Tube 360 units				
		10-piil 1330F	DG442LEDQ-T1-GE3	Tape and reel, 3000 units				
	DG442LE	16-pin SOIC	DG442LEDY-GE3	Tube 500 units				
		10-pin 3010	DG442LEDY-T1-GE3	Tape and reel, 2500 units				
		16-pin PDIP	DG442LEDJ-GE3	Tube 500 units				

PARAMETER		SYMBOL	LIMIT	UNIT	
V+ to V-			-0.3 to +18		
GND to V-A			18	v	
Digital Inputs ^a V _S , V _D			GND -0.3 to (V +) + 0.3 or 30 mA, whichever occurs first		
Continuous Current (any terminal)			30	m۸	
Current, S or D (pulsed 1 ms, 10 % duty cycle)			100	— mA	
Otowara Tawa anatiwa	(DQ, DY suffix)		-65 to +125		
Storage Temperature	(AK suffix)		-65 to +150	°C	
	16-pin TSSOP °		450		
Power Dissipation (packages) ^b	16-pin narrow body SOIC ^d		650	mW	
	16-pin CerDIP ^e	erDIP ^e 900			
ESD Human Body Model (HBM); per ANSI / ESDA / JEDEC [®] JS-001			2500	V	
Latch Up Current, per JESD78D			400	mA	

Notes

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.

c. Derate 7 mW/°C above 75 °C.

d. Derate 7.6 mW/°C above 75 °C.

e. Derate 12 mW/°C above 75 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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DG441LE, DG442LE

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SPECIFICATIONS ^a (single supply 12 V)									
PARAMETER	TEST CONDITIONS UNLESS OTHERWISE SYMBOL SPECIFIED		TEMP. ^b	TYP.°	A SUFFIX LIMITS -55 °C to +125 °C		LIM	IFFIX IITS o +85 °C	UNIT
		$V_{H} = 12 V, V_{T} = 0 V$ $V_{IN} = 2.4 V, 0.8 V^{f}$			MIN. ^d	MAX. d	MIN. d	MAX. d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full	-	0	12	0	12	V
Drain-Source On-Resistance	R _{DS(on)}	V+ = 10.8 V, V- = 0 V I_S = 10 mA, V _D = 2 V / 9 V	Room Full	16 -	-	26 40	-	26 35	Ω
On-Resistance Match Between Channels ^e	$\Delta R_{DS(on)}$	I _S = 10 mA, V _D = 9 V	Room	0.1	-	0.5	-	0.5	52
			Room	-	-1	1	-1	1	
Switch Off Leakage Current	I _{S(off)}	V _D = 1 V / 11 V,	Full	-	-15	15	-10	10	
Switch Off Leakage Current		V _S = 11 V / 1 V	Room	-	-1	1	-1	1	nA
	I _{D(off)}		Full	-	-15	15	-10	10	ΠA
Channel On Leakage Current		V _S = V _D = 11 V / 1 V	Room	-	-1	1	-1	1	-
Channel On Leakage Current	I _{D(on)}		Full	-	-15	15	-10	10	
Digital Control									
Input Current, V _{IN} Low	۱ _{IL}	V _{IN} under test = 0.8 V	Full	0.01	-1.5	1.5	-1	1	μA
Input Current, V _{IN} High	IIH	V _{IN} under test = 2.4 V	Full	-	-1.5	1.5	-1	1	μΛ
Dynamic Characteristics									
Turn-On Time	t _{ON}		Room	18	-	60	-	60	
	⁴ ON	$R_L = 300 \Omega$, $C_L = 35 pF$	Full	-	-	80	-	70	ns
Turn-Off Time	t _{OFF}	$V_{\rm S}$ = 5 V, see figure 2	Room	18	-	35	-	35	115
	UFF		Full	-	-	50	-	45	
Charge Injection ^e	Q	$V_g = 0 V, R_g = 0 \Omega, C_L = 10 nF$	Room	6.6	-	-	-	-	рС
Off Isolation ^e	OIRR	$R_L = 50 \Omega$, $C_L = 5 pF$,	Room	68.4	-	-	-	-	dB
Channel-to-Channel Crosstalk e	X _{TALK}	f = 1 MHz	Room	114	-	-	-	-	uв
Source Off Capacitance ^e	C _{S(off)}		Room	5	-	-	-	-	
Drain Off Capacitance ^e	C _{D(off)}	f = 1 MHz	Room	6	-	-	-	-	pF
Channel On Capacitance ^e	C _{D(on)}		Room	15	-	-	-	-	
Power Supplies									
Positive Supply Current	l +		Full	0.03	-	1.5	-	1	
Negative Supply Current	1-	V _{IN} = 0 V or 12 V	Room	-	-1	-	-1	-	μA
Regarive Supply Surrent	1-		Full	0.002	-7.5	-	-5	-	μΛ
Ground Current	I _{GND}		Full	0.002	-1.5	-	-1	-	

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SPECIFICATIONS a (SPECIFICATIONS ^a (dual supply ± 5 V)								
PARAMETER	SYMBOL			TYP.°	A SUFFIX LIMITS -55 °C to +125 °C		D SUFFIX LIMITS -40 °C to +85 °C		UNIT
		$V_{+} = 5 V, V_{-} = -5 V$ $V_{IN} = 2.4 V, 0.8 V^{f}$			MIN. ^d	MAX. d	MIN. d	MAX. d	
Analog Switch	_								
Analog Signal Range ^e	V _{ANALOG}		Full	-	-5	5	-5	5	V
Drain-Source On-Resistance	R _{DS(on)}	V+ = 5 V, V- = -5 V I_{S} = 10 mA, V _D = ± 3.5 V	Room Full	18 -	-	30 42	-	30 37	Ω
On-Resistance Match Between Channels ^e	$\Delta R_{DS(on)}$	$I_{\rm S}$ = 10 mA, $V_{\rm D}$ = ± 3.5 V	Room	0.1	-	0.5	-	0.5	52
			Room	-	-1	1	-1	1	
Switch Off	I _{S(off)}	V+ = 5.5, V- = -5.5 V	Full	-	-15	15	-10	10	
Leakage Current ^g		$V_{D} = \pm 4.5 \text{ V}, V_{S} = \pm 4.5 \text{ V}$	Room	-	-1	1	-1	1	- 0
	I _{D(off)}		Full	-	-15	15	-10	10	nA
Channel On		V+ = 5.5 V, V- = -5.5 V	Room	-	-1	1	-1	1	
Leakage Current ^g	I _{D(on)}	$V_{\rm S} = V_{\rm D} = \pm 4.5 \rm V$	Full	-	-15	15	-10	10	
Digital Control									
Input Current, V _{IN} Low ^e	١ _{١L}	V_{IN} under test = 0.8 V	Full	0.05	-1.5	1.5	-1	1	μA
Input Current, V _{IN} High ^e	I _{IH}	V_{IN} under test = 2.4 V	Full	0.05	-1.5	1.5	-1	1	μΑ
Dynamic Characteristics	_								
Turn-On Time	t _{ON}		Room	42	-	65	-	65	
	UN	$R_L = 300 \Omega$, $C_L = 35 pF$	Full	-	-	90	-	75	ns
Turn-Off Time	t _{OFF}	$V_{\rm S}$ = ± 3.5 V, see figure 2	Room	34	-	45	-	45	113
	•OFF		Full	-	-	65	-	55	
Charge Injection ^e	Q	$V_{g} = 0 V, R_{g} = 0 \Omega, C_{L} = 10 nF$	Room	5.8	-	-	-	-	рС
Off Isolation ^e	OIRR		Room	68.4	-	-	-	-	
Channel-to-Channel Crosstalk ^e	X _{TALK}	$R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$	Room	113	-	-	-	-	dB
Source Off Capacitance ^e	C _{S(off)}		Room	5	-	-	-	-	
Drain Off Capacitance ^e	C _{D(off)}	f = 1 MHz	Room	6	-	-	-	-	pF
Channel On Capacitance ^e	C _{D(on)}		Room	14	-	-	-	-	
Power Supplies									
Positive Supply Current ^e	l +		Full	0.002	-	1.5	-	1	
Negative Supply Current ^e	1-	$V_{IN} = 0 V \text{ or } 5 V$	Room	-0.002	-1	-	-1	-	μA
			Full	-	-7.5	-	-5	-	μ
Ground Current ^e	I _{GND}		Full	-0.002	-1.5	-	-1	-	



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DG441LE, DG442LE

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SPECIFICATIONS ^a (single supply ± 5 V)									
PARAMETER	SYMBOL			TYP.°	LIN	IFFIX IITS 9 +125 °C	LIN	JFFIX 1ITS o +85 °C	UNIT
		V+ = 5 V, V- = 0 V $V_{IN} = 2.4 V, 0.8 V f$			MIN. ^d	MAX. d	MIN. ^d	MAX. d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full	-	-	5	-	5	V
Drain-Source	Base	V + = 4.5 V	Room	36	-	50	-	50	
On-Resistance ^e	R _{DS(on)}	$I_{S} = 5 \text{ mA}, V_{D} = 1 \text{ V}, 3.5 \text{ V}$	Full	-	-	88	-	75	Ω
On-Resistance Match Between Channels ^e	$\Delta R_{DS(on)}$	$I_{\rm S}$ = 10 mA, $V_{\rm D}$ = 3.5 V	Room	0.5	-	1	-	1	
Dynamic Characteristics									
Turn-On Time ^e	+	R _L = 300 Ω, C _L = 35 pF	Room	53	-	70	-	70	
	t _{ON}		Hot	-	-	90	-	80	ns
Turn-Off Time ^e	0	$V_{\rm S}$ = 3.5 V, see figure 2	Room	34	-	50	-	50	115
	t _{OFF}		Hot	-	-	70	-	60	
Charge Injection ^e	Q	$V_g = 0 \text{ V}, \text{R}_g = 0 \Omega, \text{C}_\text{L} = 10 \text{nF}$	Room	3.3	-	-	-	-	рС
Power Supplies									
Positive Supply Current ^e	l +		Full	10	-	200	-	100	
Negative Supply Current ^e	1-	V _{IN} = 0 V or 5 V	Room	-0.002	-1	-	-1	-	
Negative Supply Current	1-	$v_{\rm IN} = 0$ v or 5 v	Full	-	-7.5	-	-5	-	μA
Ground Current ^e	I _{GND}		Full	-10	-200	-	-100	-	



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SPECIFICATIONS ^a (single supply 3 V)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED	TEMP. ^b	TEMP. ^b TYP. ^c	A SUFFIX LIMITS -55 °C to +125 °C		D SUFFIX LIMITS -40 °C to +85 °C		UNIT
		V + = 3 V, V - = 0 V $V_{IN} = 0.4 V^{f}$			MIN. ^d	MAX. d	MIN. d	MAX. d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full	-	0	3	0	3	V
Drain-Source On-Resistance	R _{DS(on)}	V+ = 2.7 V, V- = 0 V I _S = 5 mA, V _D = 0.5 V, 2.2 V	Room Full	106 -	-	130 150	-	130 140	0
On-Resistance Match Between Channels ^e	$\Delta R_{DS(on)}$	$I_{\rm S}$ = 5 mA, $V_{\rm D}$ = 2.2 V	Room	1	-	3	-	3	Ω
			Room	-	-1	1	-1	1	
Switch Off	I _{S(off)}	V+ = 3.3, V- = 0 V	Full	-	-15	15	-10	10	
Leakage Current ^g		$V_{D} = 1 V, 2 V, V_{S} = 2 V, 1 V$	Room	-	-1	1	-1	1	nA
	I _{D(off)}		Full	-	-15	15	-10	10	
Channel On	1	V+ = 3.3 V, V- = 0 V	Room	-	-1	1	-1	1	
Leakage Current ^g	I _{D(on)}	$V_{S} = V_{D} = 1 V, 2 V$	Full	-	-15	15	-10	10	
Digital Control									
Input Current, V _{IN} Low ^e	۱ _{IL}	V_{IN} under test = 0.4 V	Full	0.005	-1.5	1.5	-1	1	μA
Input Current, V _{IN} High ^e	I _{IH}	V_{IN} under test = 2.4 V	Full	0.005	-1.5	1.5	-1	1	μΛ
Dynamic Characteristics			-				-	-	
Turn-On Time	t _{ON}		Room	141	-	200	-	200	
	UN	$R_L = 300 \Omega$, $C_L = 35 pF$	Full	-	-	220	-	210	ns
Turn-Off Time	t _{OFF}	$V_{\rm S}$ = 1.5 V, see figure 2	Room	84	-	120	-	120	115
	*OFF		Full	-	-	140	-	130	
Charge Injection ^e	Q	$V_{g} = 0 V, R_{g} = 0 \Omega, C_{L} = 10 nF$	Room	2	-	-	-	-	рС
Off Isolation ^e	OIRR		Room	68	-	-	-	-	
Channel-to-Channel Crosstalk ^e	X _{TALK}	$R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$	Room	107	-	-	-	-	dB
Source Off Capacitance ^e	C _{S(off)}		Room	6	-	-	-	-	
Drain Off Capacitance ^e	C _{D(off)}	f = 1 MHz	Room	7	-	-	-	-	pF
Channel On Capacitance ^e	C _{D(on)}		Room	15	-	-	-	-	

Notes

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.

e. Guaranteed by design, not subject to production test.

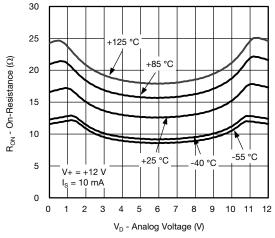
f. V_{IN} = input voltage to perform proper function.

g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.

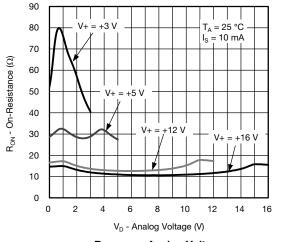


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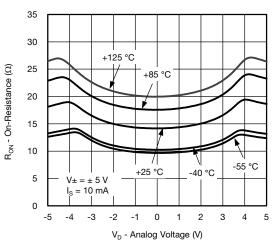
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



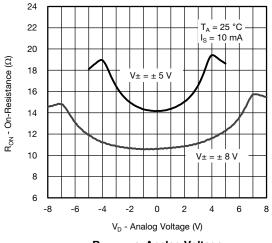
R_{DS(on)} vs. Analog Voltage and Temperature



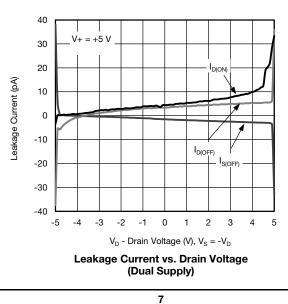
R_{DS(on)} vs. Analog Voltage



R_{DS(on)} vs. Drain Voltage and Temperature



R_{DS(on)} vs. Analog Voltage



S16-0392-Rev. A, 07-Mar-16

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Document Number: 76754

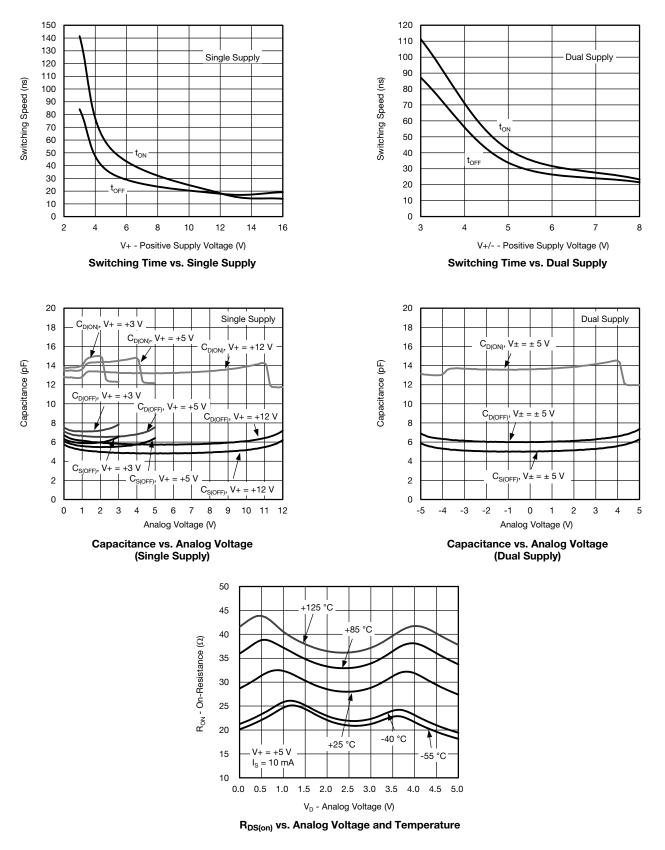
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



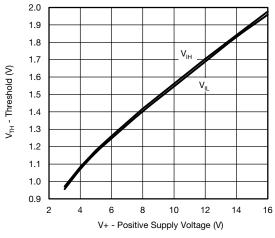
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Document Number: 76754

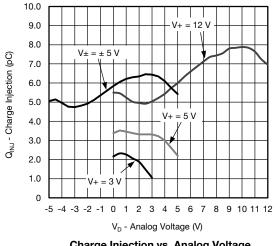


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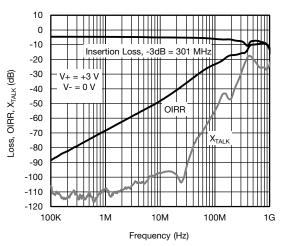
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



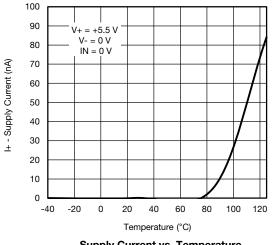
Input Threshold vs. Single Supply Voltage



Charge Injection vs. Analog Voltage



Insertion Loss, Off Isolation and Crosstalk vs. Frequency (Single Supply)



Supply Current vs. Temperature



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SCHEMATIC DIAGRAM (typical channel)

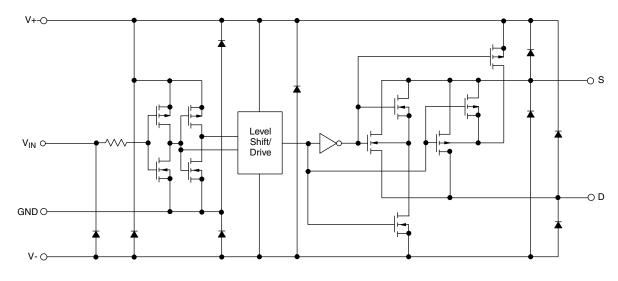
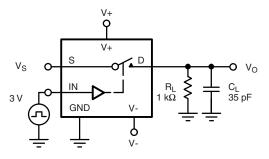


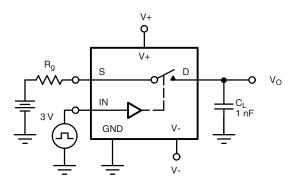
Fig. 1

TEST CIRCUITS

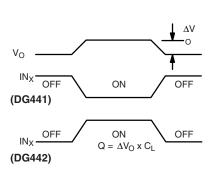


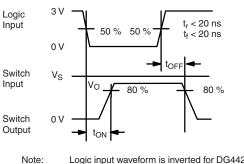
C_L (includes fixture and stray capacitance)











Logic input waveform is inverted for DG442.



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TEST CIRCUITS

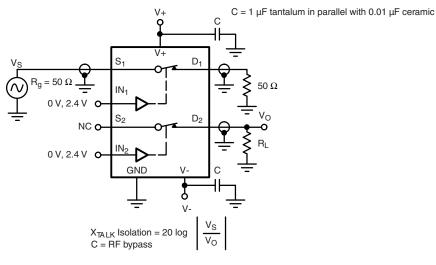
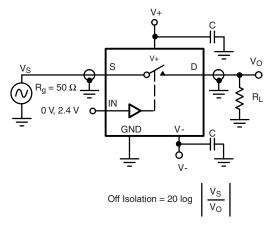


Fig. 4 - Crosstalk





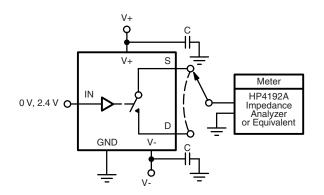


Fig. 6 - Source / Drain Capacitances

-0 + 12 V GND V IN O 0 = Load Off 1 = Load On

1+ 12 V

DG441L or DG442L

V δ V GND

V+

150 Ω

 $10 \ k\Omega$

+ 24 V C

I = 3A

VN0300L, M

ξ R_L

Fig. 7 - Power MOSFET Driver

VIN O

0

0

0

C

GAIN₁

 $A_V = 1$

 $\begin{array}{l} \mathsf{GAIN}_2\\ \mathsf{A}_V=10 \end{array}$

 $GAIN_3$ $A_V = 20$

 $GAIN_4$ A_V = 100



Ş R₁ 90 kΩ

Ş

Ş R₃ 4 kΩ

 R_2

5 kΩ

R₄ 1 kΩ Ş

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APPLICATIONS

+ 12 V O

IN C

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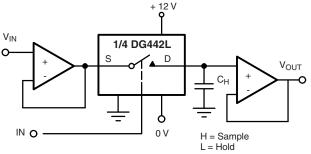
+ 12 V 0

V+

DG442L

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V_{OUT} o

Gain error is determined only by the resistor tolerance. Op amp offset and CMRR will limit accuracy of circuit.

With SW₄ Closed

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

S16-0392-Rev. A, 07-Mar-16

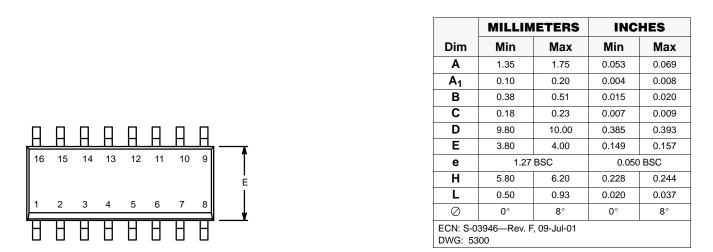
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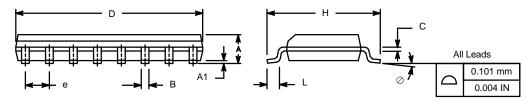
Document Number: 76754



SOIC (NARROW): 16-LEAD

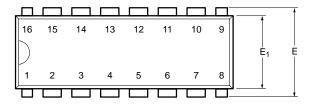
JEDEC Part Number: MS-012

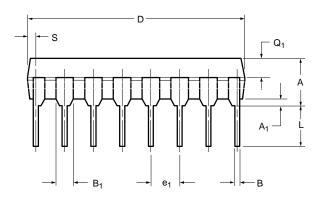


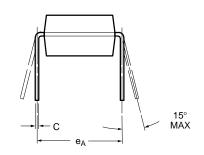




PDIP: 16-LEAD







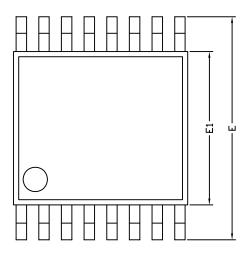
	MILLIN	IETERS	INC	HES		
Dim	Min	Max	Min	Max		
Α	3.81	5.08	0.150	0.200		
A ₁	0.38	1.27	0.015	0.050		
В	0.38	0.51	0.015	0.020		
B ₁	0.89	1.65	0.035	0.065		
С	0.20	0.30	0.008	0.012		
D	18.93	21.33	0.745	0.840		
E	7.62	8.26	0.300	0.325		
E ₁	5.59	7.11	0.220	0.280		
e ₁	2.29	2.79	0.090	0.110		
e _A	7.37	7.87	0.290	0.310		
L	2.79	3.81	0.110	0.150		
Q ₁	1.27	2.03	0.050	0.080		
S	0.38	1.52	.015	0.060		
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482						

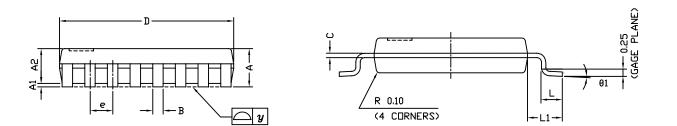


Package Information

Vishay Siliconix

TSSOP: 16-LEAD





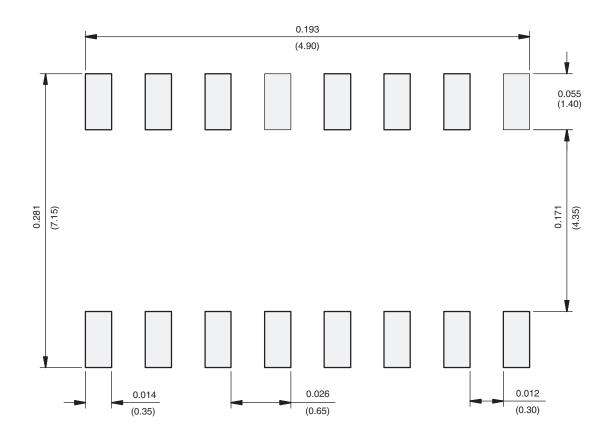
	DIMENSIONS IN MILLIMETERS						
Symbols	Min	Nom	Мах				
A	-	1.10	1.20				
A1	0.05	0.10	0.15				
A2	-	1.00	1.05				
В	0.22	0.28	0.38				
С	-	0.127	-				
D	4.90	5.00	5.10				
E	6.10	6.40	6.70				
E1	4.30	4.40	4.50				
е	-	0.65	-				
L	0.50	0.60	0.70				
L1	0.90	1.00	1.10				
у	-	-	0.10				
θ1	0°	3°	6°				
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624							



PAD Pattern

Vishay Siliconix

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads Dimensions in inches (mm)

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



Vishay

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