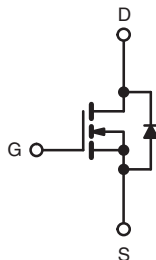
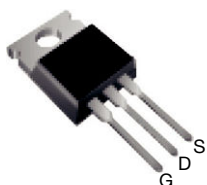


D Series Power MOSFET

PRODUCT SUMMARY

V _{DS} (V) at T _J max.	450	
R _{DS(on)} max. at 25 °C (Ω)	V _{GS} = 10 V	1.0
Q _g max. (nC)	18	
Q _{gs} (nC)	3	
Q _{gd} (nC)	4	
Configuration	Single	

TO-220AB


N-Channel MOSFET

FEATURES

- Optimal Design
 - Low Area Specific On-Resistance
 - Low Input Capacitance (C_{iss})
 - Reduced Capacitive Switching Losses
 - High Body Diode Ruggedness
 - Avalanche Energy Rated (UIS)
- Optimal Efficiency and Operation
 - Low Cost
 - Simple Gate Drive Circuitry
 - Low Figure-of-Merit (FOM): R_{on} x Q_g
 - Fast Switching
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Note

* Lead (Pb)-containing terminations are not RoHS-compliant. Exemptions may apply.

APPLICATIONS

- Consumer Electronics
 - Displays (LCD or Plasma TV)
- Server and Telecom Power Supplies
 - SMPS
- Industrial
 - Welding
 - Induction Heating
 - Motor Drives
- Battery Chargers



RoHS*
COMPLIANT
HALOGEN
FREE
Available

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	SiHP6N40D-E3
Lead (Pb)-free and Halogen-free	SiHP6N40D-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	400	V
Gate-Source Voltage	V _{GS}	± 30	
Gate-Source Voltage AC (f > 1 Hz)		30	
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed Drain Current ^a	I _{DM}	13	A
Linear Derating Factor		0.8	
Single Pulse Avalanche Energy ^b	E _{AS}	104	mJ
Maximum Power Dissipation	P _D	104	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Drain-Source Voltage Slope	dV/dt	24	V/ns
Reverse Diode dV/dt ^d		0.48	
Soldering Recommendations (Peak Temperature)	for 10 s	300°	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- V_{DD} = 50 V, starting T_J = 25 °C, L = 2.3 mH, R_g = 25 Ω, I_{AS} = 9.5 A.
- 1.6 mm from case.
- I_{SD} ≤ I_D, starting T_J = 25 °C.

**THERMAL RESISTANCE RATINGS**

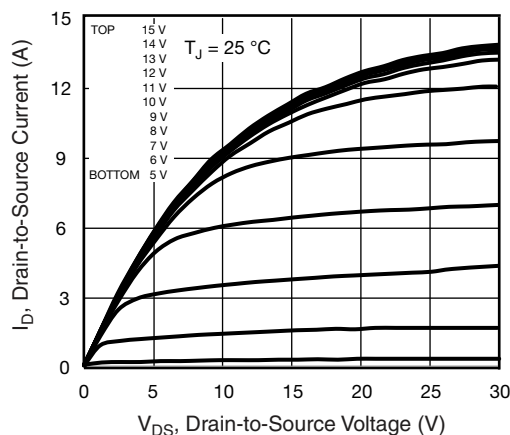
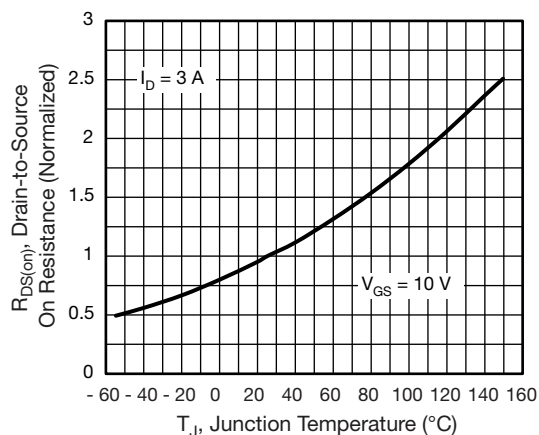
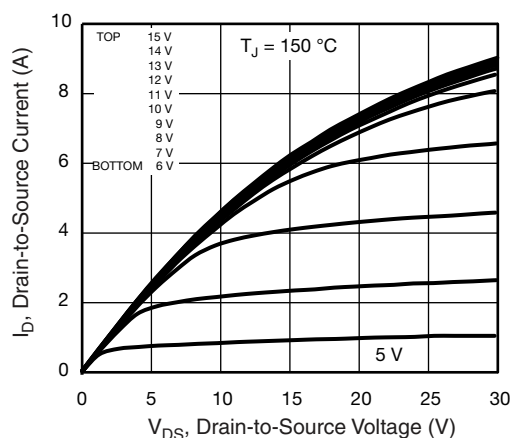
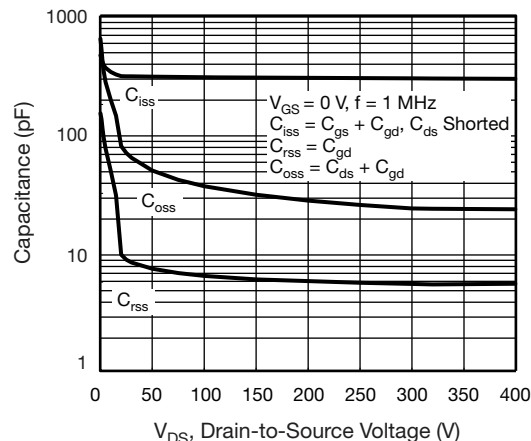
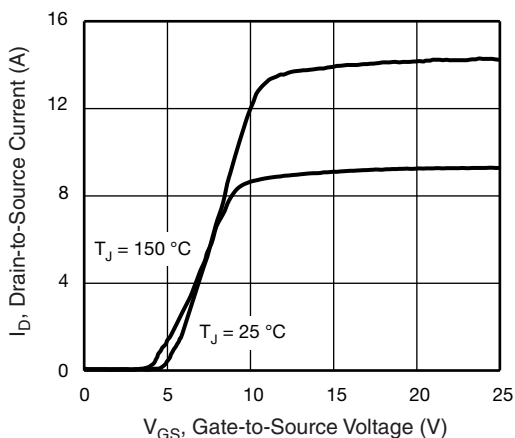
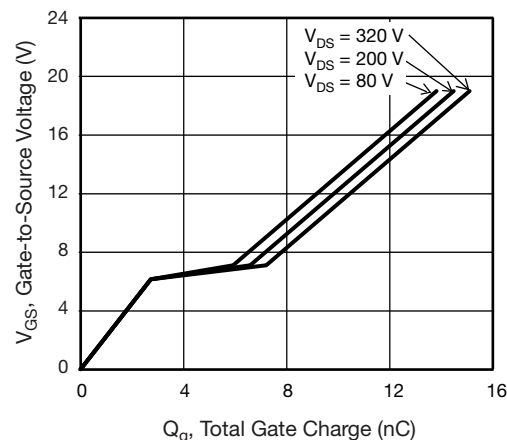
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.2	

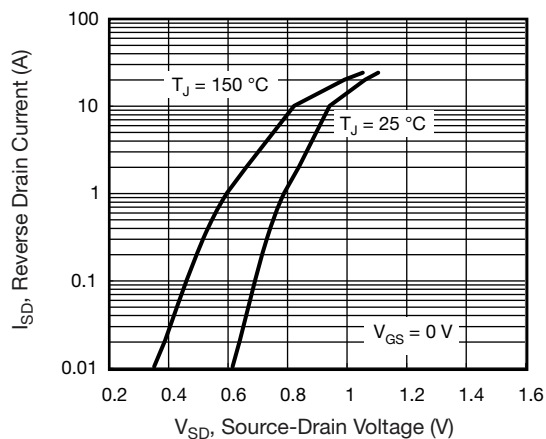
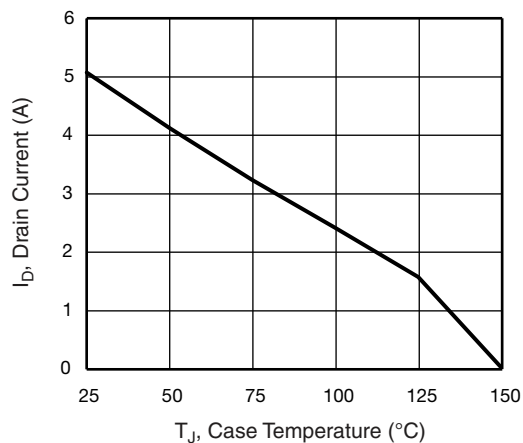
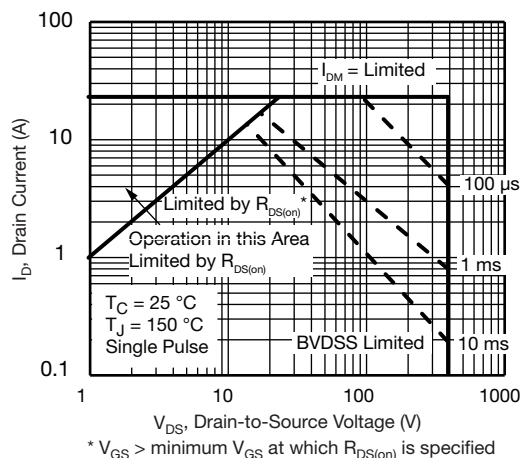
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		400	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 250\text{ }\mu\text{A}$		-	0.53	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		3	-	5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 320\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$	-	0.85	1.0	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 3\text{ A}$		-	1.7	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$		-	311	-	pF
Output Capacitance	C_{oss}			-	38	-	
Reverse Transfer Capacitance	C_{rss}			-	7	-	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V to } 320\text{ V}$		-	44	-	pF
Effective output capacitance, time related ^b	$C_{o(tr)}$			-	54	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$, $V_{DS} = 320\text{ V}$	-	9	18	nC
Gate-Source Charge	Q_{gs}			-	3	-	
Gate-Drain Charge	Q_{gd}			-	4	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}$, $I_D = 3\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$		-	12	24	ns
Rise Time	t_r			-	11	22	
Turn-Off Delay Time	$t_{d(off)}$			-	14	28	
Fall Time	t_f			-	8	16	
Gate Input Resistance	R_g	f = 1 MHz, open drain		-	1.9	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	6	A
Pulsed Diode Forward Current	I_{SM}			-	-	24	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 3\text{ A}$, $V_{GS} = 0\text{ V}$		-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = I_S = 3\text{ A}$, dI/dt = 100 A/ μs , $V_R = 20\text{ V}$		-	236	-	ns
Reverse Recovery Charge	Q_{rr}			-	1.1	-	μC
Reverse Recovery Current	I_{RRM}			-	9	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

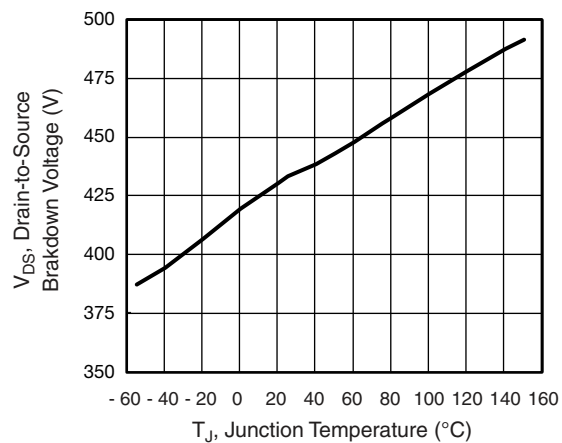
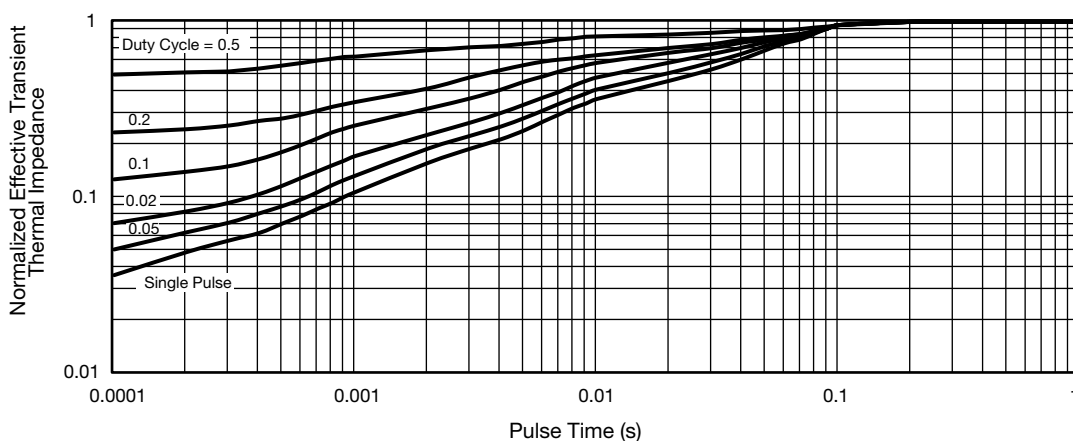
Fig. 8 - Maximum Safe Operating Area

Fig. 10 - Temperature vs. Drain-to-Source Voltage

Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case


Fig. 12 - Switching Time Test Circuit

Fig. 16 - Basic Gate Charge Waveform

Fig. 13 - Switching Time Waveforms

Fig. 17 - Gate Charge Test Circuit

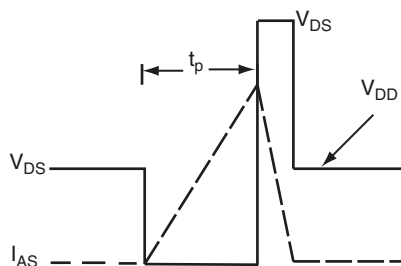
Fig. 14 - Unclamped Inductive Test Circuit

Fig. 15 - Unclamped Inductive Waveforms



Fig. 18 - For N-Channel

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