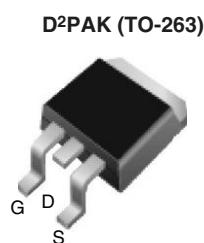


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	- 100	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = - 10$ V	0.20
$Q_g$ (Max.) (nC)	61	
$Q_{gs}$ (nC)	14	
$Q_{gd}$ (nC)	29	
Configuration	Single	



### FEATURES

- Halogen-free According to IEC 61249-2-21
- **Definition**
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- P-Channel
- 175 °C Operating Temperature
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK (TO-263) is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF9540S-GE3	SiHF9540STRL-GE3 <sup>a</sup>
Lead (Pb)-free	IRF9540SPbF	IRF9540STRLPbFa
	SiHF9540S-E3	SiHF9540STL-E3 <sup>a</sup>

#### Note

a. See device orientation.

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	- 100	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	- 19	A
		- 13	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	- 72	
Linear Derating Factor		1.0	
Linear Derating Factor (PCB Mount) <sup>e</sup>		0.025	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	640	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	- 19	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	15	mJ
Maximum Power Dissipation	$P_D$	150	W
		3.7	
Peak Diode Recovery dV/dt <sup>c</sup>	$dV/dt$	- 5.5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	°C

#### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b.  $V_{DD} = - 25$  V, starting  $T_J = 25$  °C,  $L = 2.7$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = - 19$  A (see fig. 12).

c.  $I_{SD} \leq - 19$  A,  $dI/dt \leq 200$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175$  °C.

d. 1.6 mm from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material)

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	1.0	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

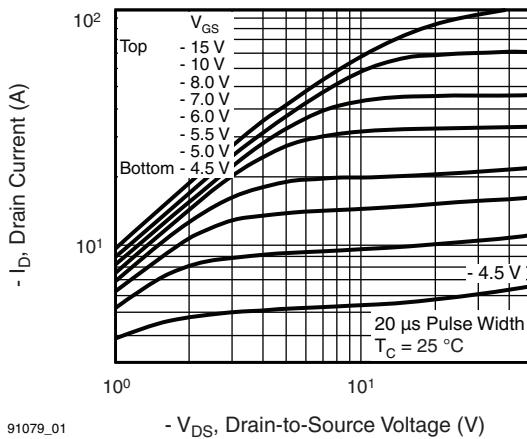
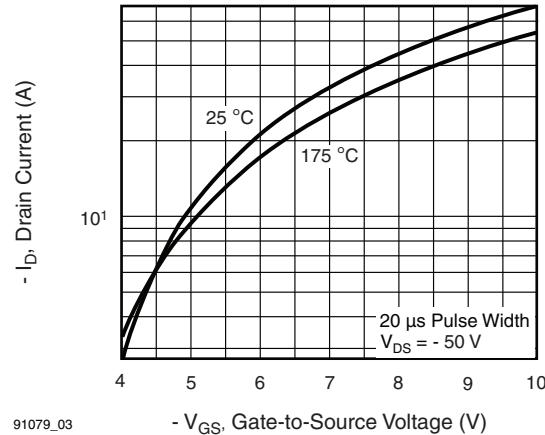
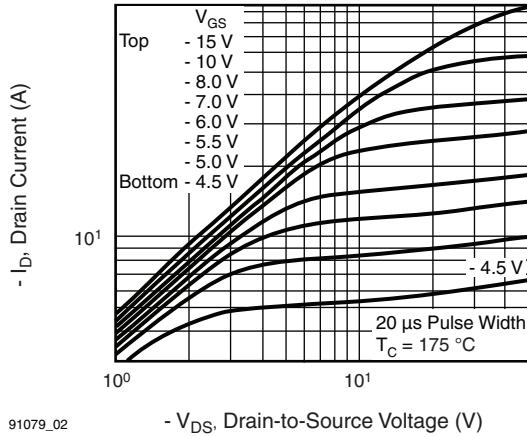
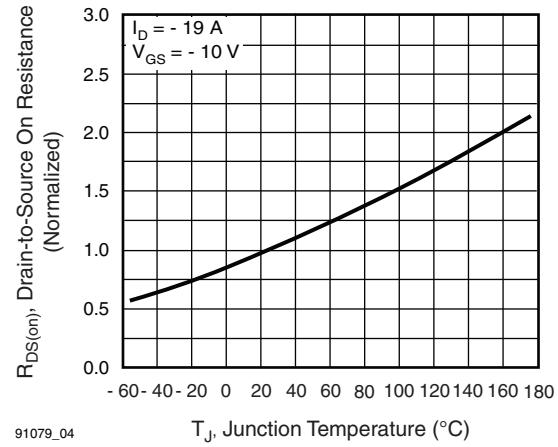
**SPECIFICATIONS** ( $T_J = 25$  °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ , $I_D = -250$ µA		- 100	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = -1$ mA		-	- 0.087	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250$ µA		- 2.0	-	- 4.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20$ V		-	-	± 100	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -100$ V, $V_{GS} = 0$ V		-	-	- 100	µA	
		$V_{DS} = -80$ V, $V_{GS} = 0$ V, $T_J = 150$ °C		-	-	- 500		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10$ V	$I_D = -11$ A <sup>b</sup>	-	-	0.20	Ω	
Forward Transconductance	$g_{fs}$	$V_{DS} = -50$ V, $I_D = -11$ A		6.2	-	-	S	
<b>Dynamic</b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0$ V, $V_{DS} = -25$ V, $f = 1.0$ MHz, see fig. 5		-	1400	-	pF	
Output Capacitance	$C_{oss}$			-	590	-		
Reverse Transfer Capacitance	$C_{rss}$			-	140	-		
Total Gate Charge	$Q_g$	$V_{GS} = -10$ V	$I_D = -19$ A, $V_{DS} = -80$ V, see fig. 6 and 13 <sup>b</sup>	-	-	61	nC	
Gate-Source Charge	$Q_{gs}$			-	-	14		
Gate-Drain Charge	$Q_{gd}$			-	-	29		
Turn-On Delay Time	$t_{d(on)}$			-	16	-		
Rise Time	$t_r$	$V_{DD} = -50$ V, $I_D = -19$ A, $R_G = 9.1$ Ω, $R_D = 2.4$ Ω, see fig. 10 <sup>b</sup>		-	73	-	ns	
Turn-Off Delay Time	$t_{d(off)}$			-	34	-		
Fall Time	$t_f$			-	57	-		
Internal Drain Inductance	$L_D$			-	4.5	-	nH	
Internal Source Inductance	$L_S$	Between lead, 6 mm (0.25") from package and center of die contact		-	7.5	-		
<b>Drain-Source Body Diode Characteristics</b>								
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	- 19	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	- 72		
Body Diode Voltage	$V_{SD}$	$T_J = 25$ °C, $I_S = -19$ A, $V_{GS} = 0$ V <sup>b</sup>		-	-	- 5.0	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25$ °C, $I_F = -19$ A, $dI/dt = 100$ A/µs <sup>b</sup>		-	130	260	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.35	0.70	nC	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )						

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_C = 25 \text{ }^{\circ}\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_C = 175 \text{ }^{\circ}\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

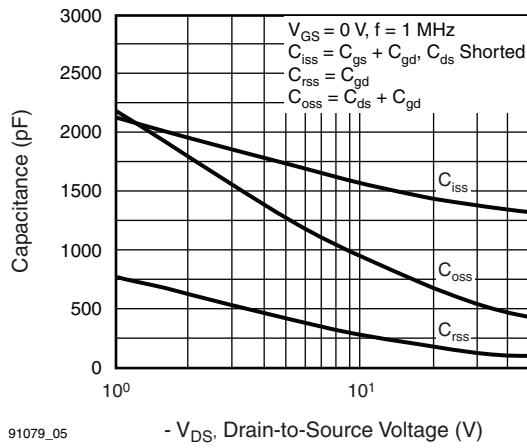


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

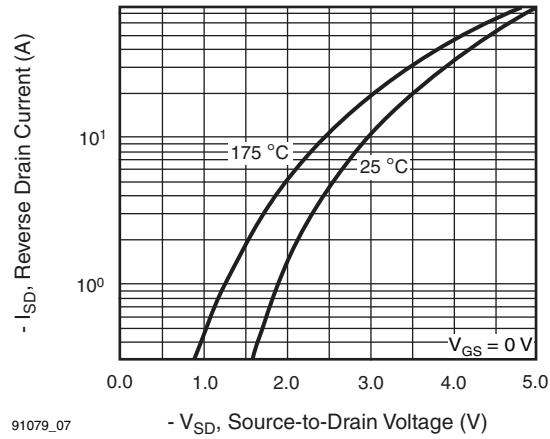


Fig. 7 - Typical Source-Drain Diode Forward Voltage

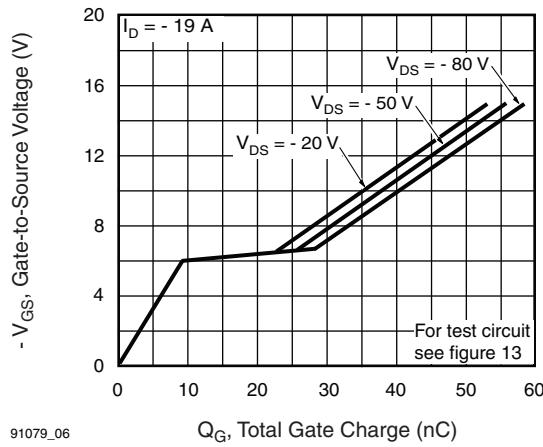


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

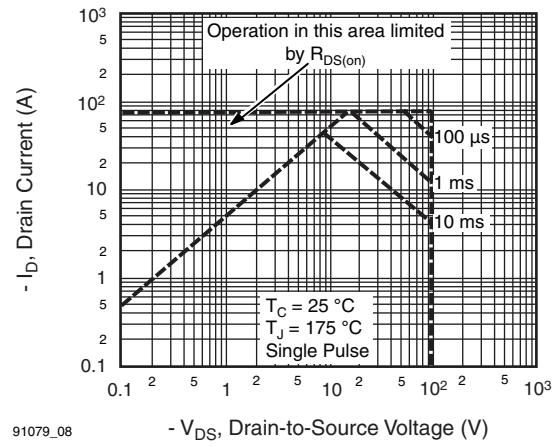
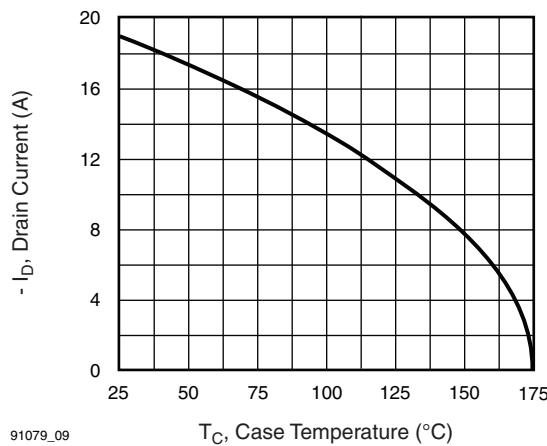
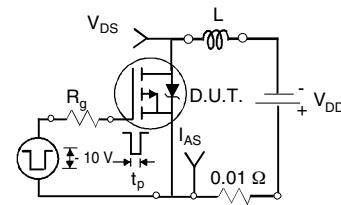
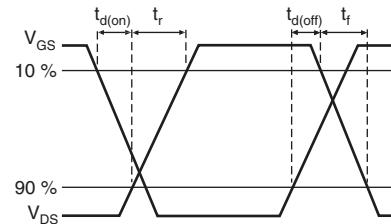
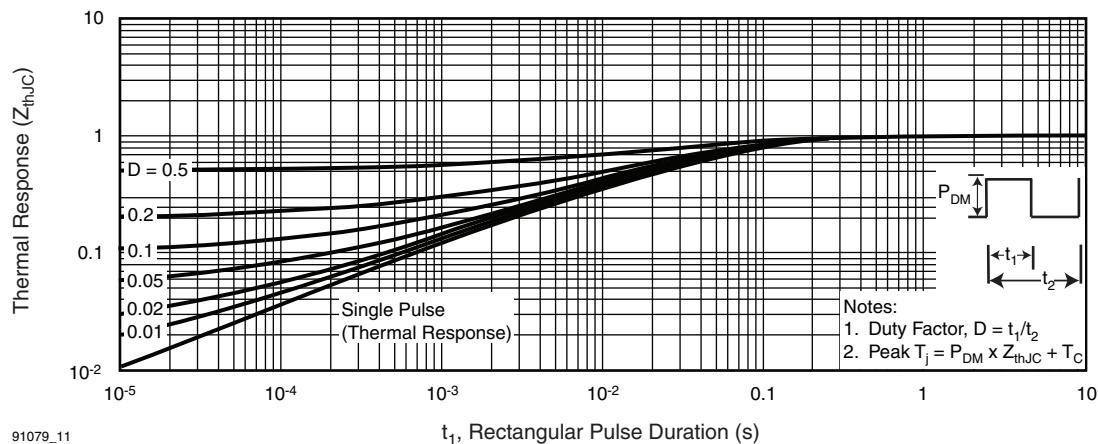


Fig. 8 - Maximum Safe Operating Area


**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

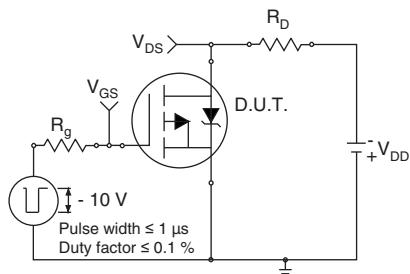


Fig. 12a - Unclamped Inductive Test Circuit

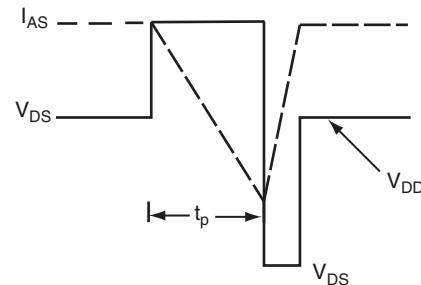


Fig. 12b - Unclamped Inductive Waveforms

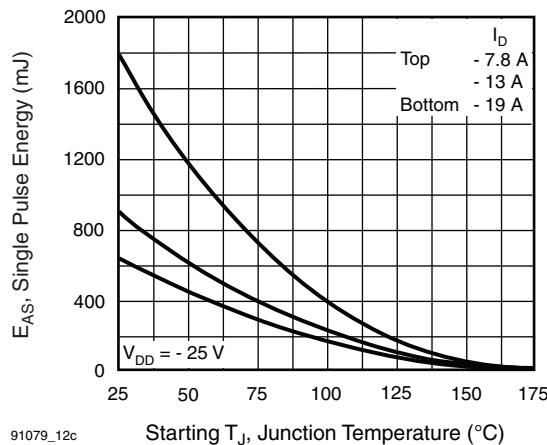


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

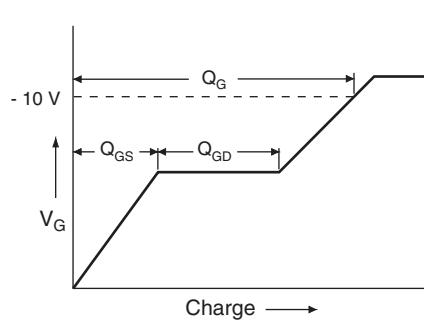


Fig. 13a - Basic Gate Charge Waveform

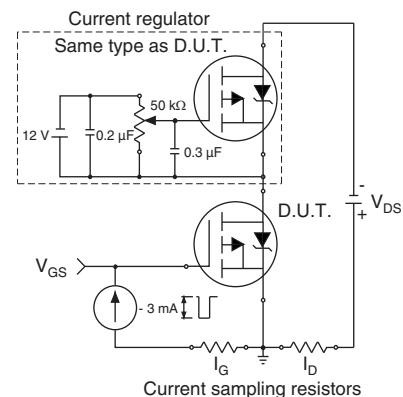
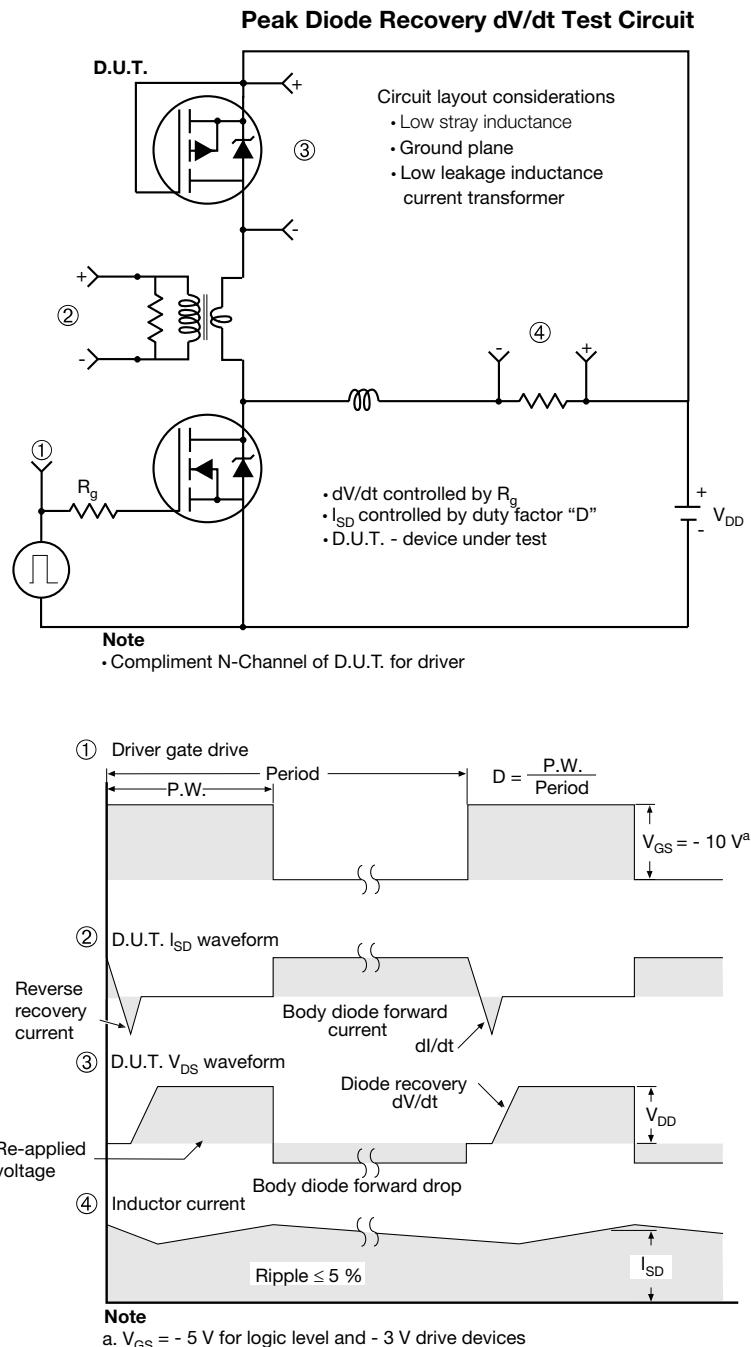
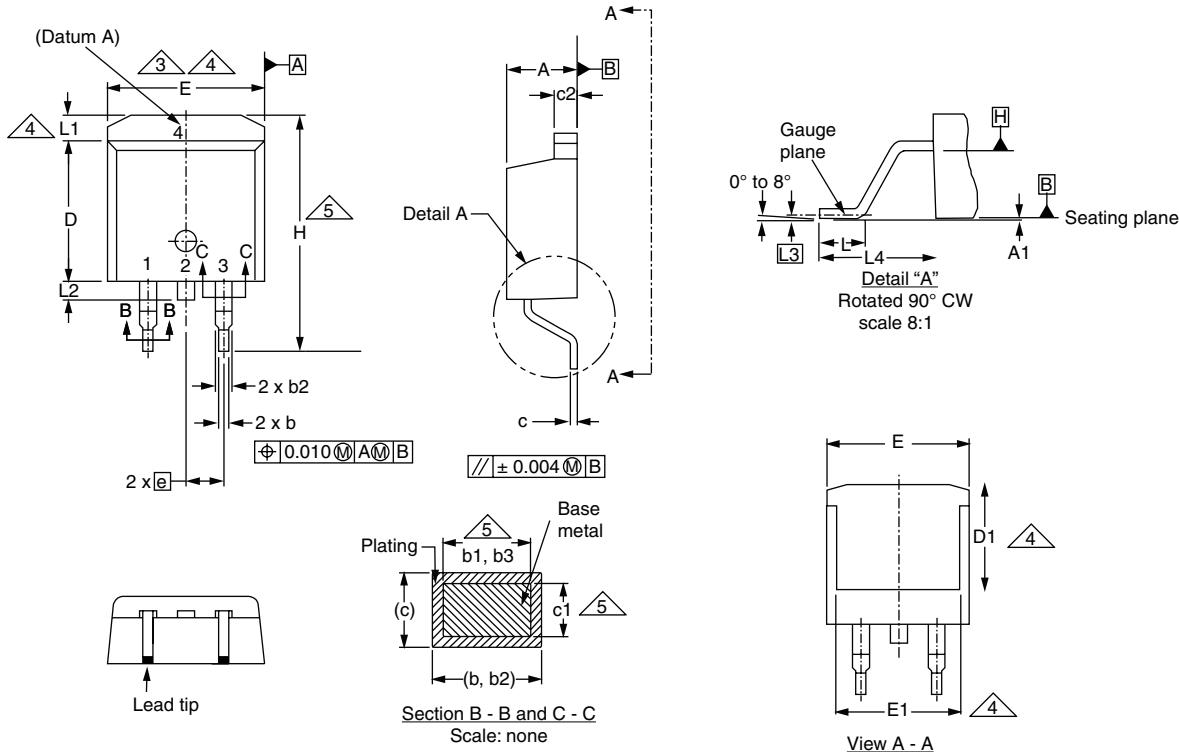


Fig. 13b - Gate Charge Test Circuit


**Fig. 14 - For P-Channel**

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## **TO-263AB (HIGH VOLTAGE)**



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

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## Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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