

## EL Series Power MOSFET

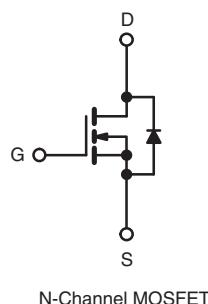
PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	650
$R_{DS(on)}$ typ. at 25 °C (Ω)	$V_{GS} = 10$ V 0.171
$Q_g$ max. (nC)	74
$Q_{gs}$ (nC)	15
$Q_{gd}$ (nC)	15
Configuration	Single

### FEATURES

- Reduced figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS  
COMPLIANT  
HALOGEN  
FREE



### APPLICATIONS

- Server and telecom power supplies
  - Switch mode power supplies (SMPS)
  - Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHB22N60EL-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	21	A
		13	
	$I_{DM}$	45	
Linear Derating Factor		1.8	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	286	mJ
Maximum Power Dissipation	$P_D$	227	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	°C
Drain-Source Voltage Slope	$dV/dt$	62	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>		22	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s	300	°C

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$  Ω,  $I_{AS} = 4.5$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/μs, starting  $T_J = 25$  °C.

**THERMAL RESISTANCE RATINGS**

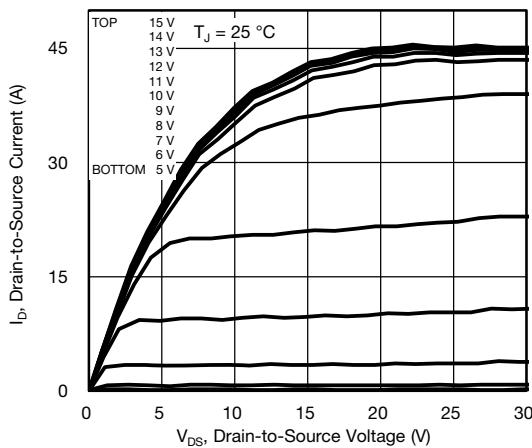
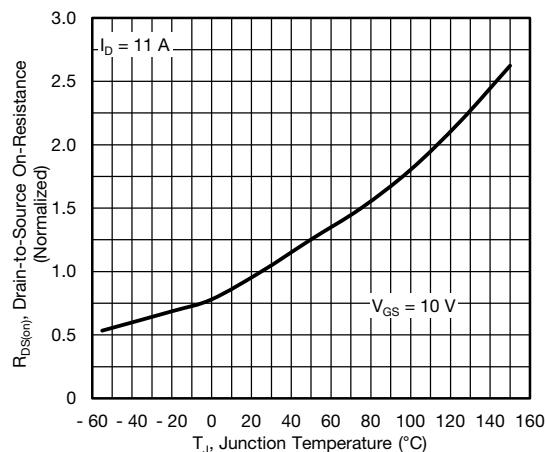
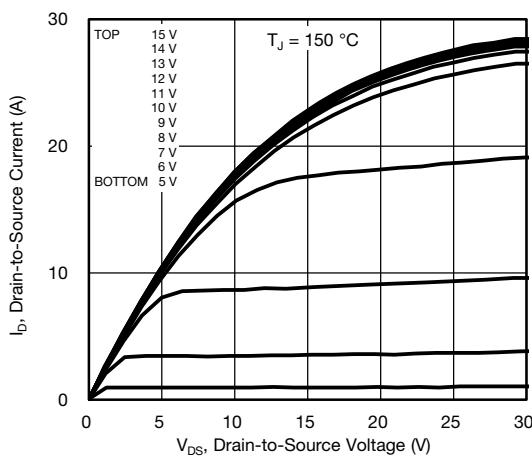
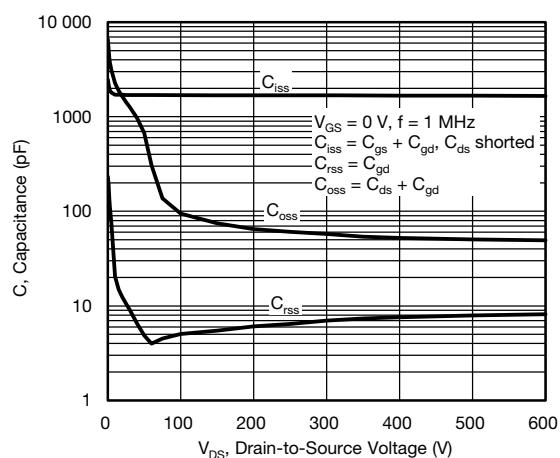
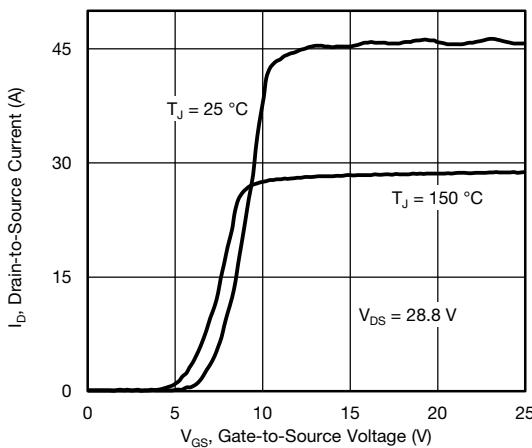
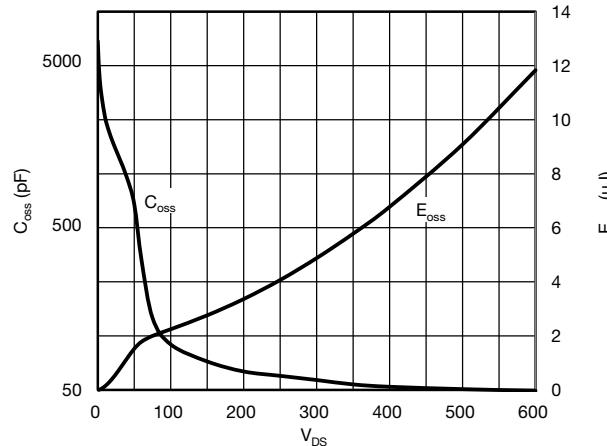
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.55	

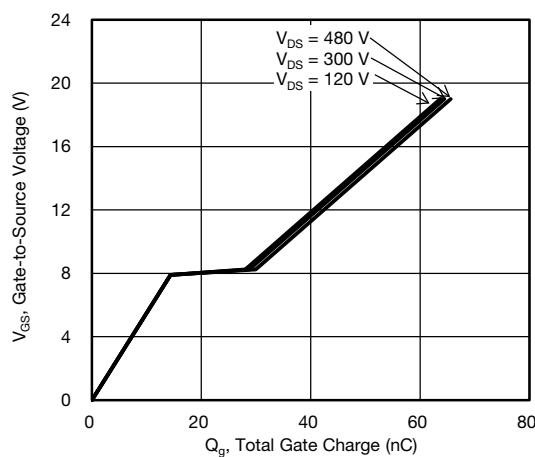
**SPECIFICATIONS** ( $T_J = 25^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25^{\circ}\text{C}$ , $I_D = 1 \text{ mA}$		-	0.71	-	$\text{V}/^{\circ}\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		3	-	5	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$		-	-	$\pm 100$	nA
		$V_{GS} = \pm 30 \text{ V}$		-	-	$\pm 1$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 480 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125^{\circ}\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 11 \text{ A}$	-	0.171	0.197	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 20 \text{ V}$ , $I_D = 11 \text{ A}$		-	6.5	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 100 \text{ V}$ , $f = 1 \text{ MHz}$		-	1690	-	pF
Output Capacitance	$C_{oss}$			-	95	-	
Reverse Transfer Capacitance	$C_{rss}$			-	5	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0 \text{ V}$ to $400 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	85	-	
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$			-	296	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10 \text{ V}$	$I_D = 11 \text{ A}$ , $V_{DS} = 480 \text{ V}$	-	37	74	nC
Gate-Source Charge	$Q_{gs}$			-	15	-	
Gate-Drain Charge	$Q_{gd}$			-	15	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480 \text{ V}$ , $I_D = 11 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_g = 9.1 \Omega$		-	22	44	ns
Rise Time	$t_r$			-	46	92	
Turn-Off Delay Time	$t_{d(off)}$			-	27	54	
Fall Time	$t_f$			-	24	48	
Gate Input Resistance	$R_g$	$f = 1 \text{ MHz}$ , open drain		-	0.65	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	21	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	45	
Diode Forward Voltage	$V_{SD}$	$T_J = 25^{\circ}\text{C}$ , $I_S = 11 \text{ A}$ , $V_{GS} = 0 \text{ V}$		-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}$ , $I_F = I_S = 11 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_R = 25 \text{ V}$		-	365	-	ns
Reverse Recovery Charge	$Q_{rr}$			-	5.8	-	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$			-	29	-	A

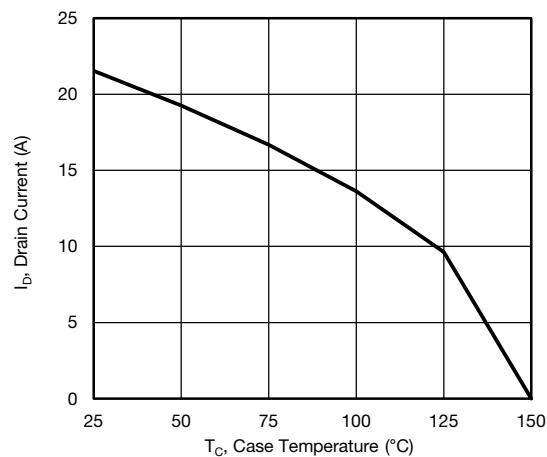
**Notes**

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .  
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

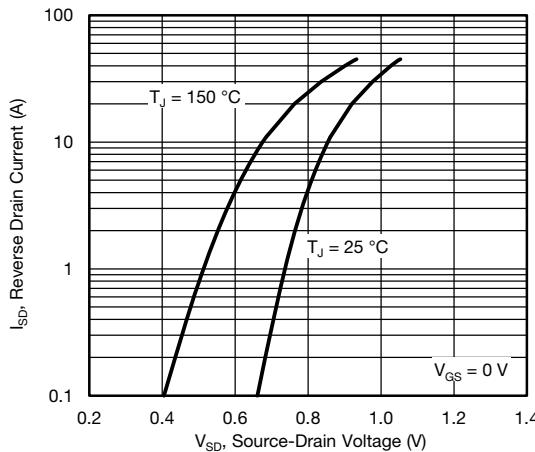
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**



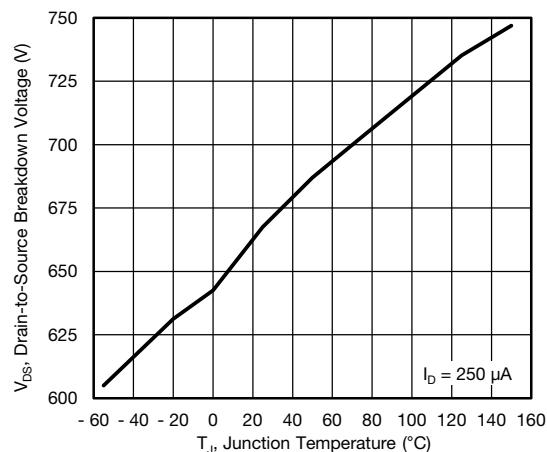
**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**



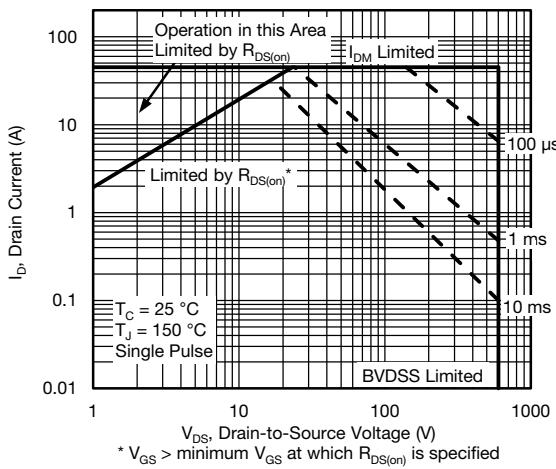
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



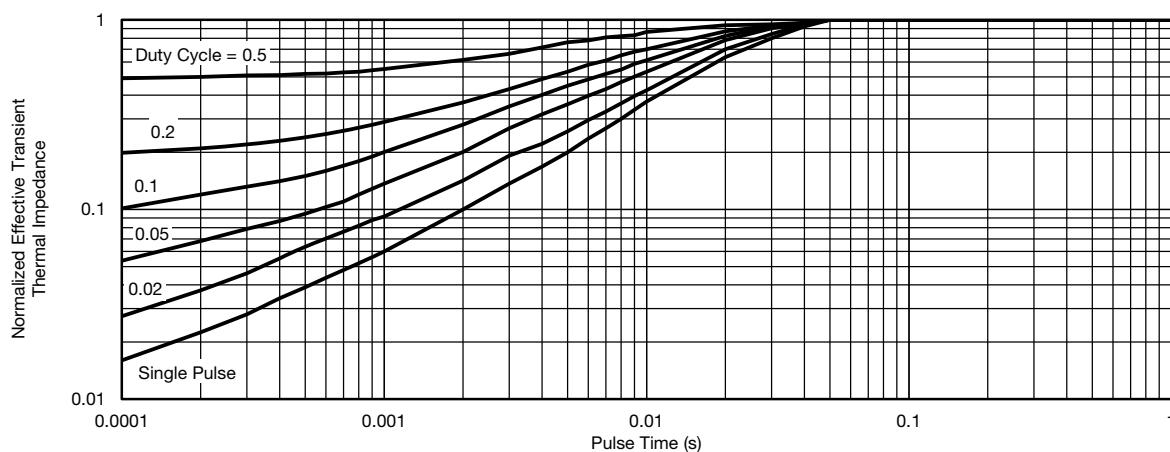
**Fig. 8 - Typical Source-Drain Diode Forward Voltage**



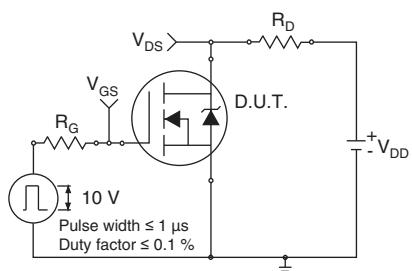
**Fig. 11 - Temperature vs. Drain-to-Source Voltage**



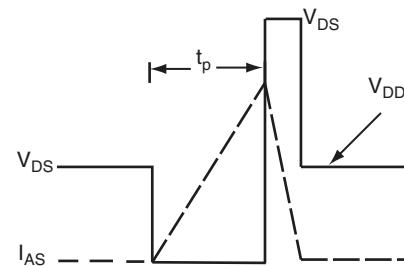
**Fig. 9 - Maximum Safe Operating Area**



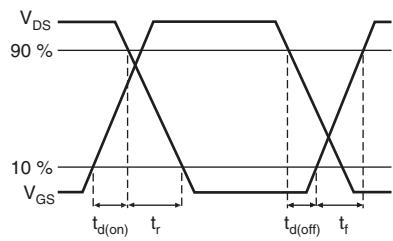
**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**



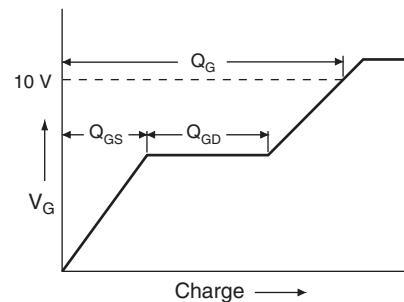
**Fig. 13 - Switching Time Test Circuit**



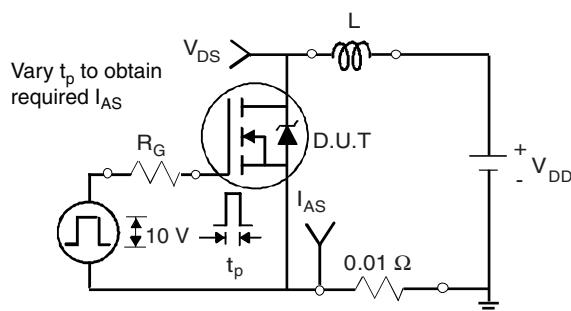
**Fig. 16 - Unclamped Inductive Waveforms**



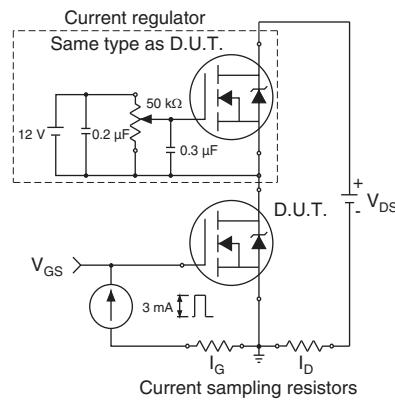
**Fig. 14 - Switching Time Waveforms**



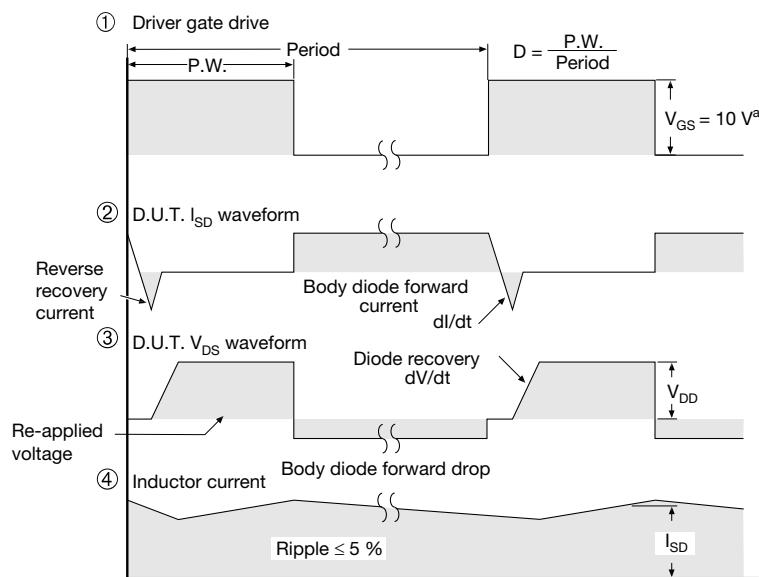
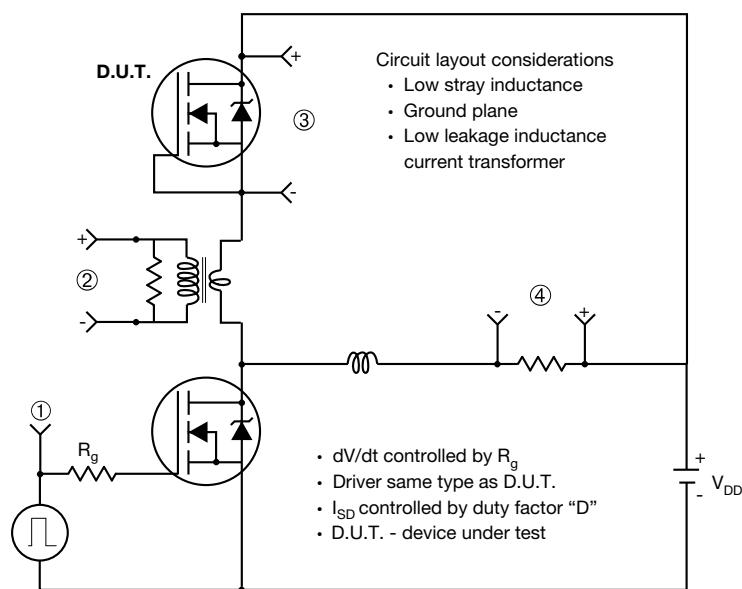
**Fig. 17 - Basic Gate Charge Waveform**



**Fig. 15 - Unclamped Inductive Test Circuit**



**Fig. 18 - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**

**Note**

a.  $V_{GS} = 5 \text{ V}$  for logic level devices

**Fig. 19 - For N-Channel**

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