D Series Power MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.85
Q_g (max.) (nC)	30	
Q_{gs} (nC)	4	
Q_{gd} (nC)	7	
Configuration	Single	

D²PAK (TO-263)
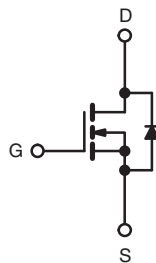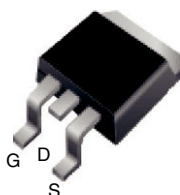
N-Channel MOSFET

FEATURES

- Optimal Design
  - Low Area Specific On-Resistance
  - Low Input Capacitance (C_{iss})
  - Reduced Capacitive Switching Losses
  - High Body Diode Ruggedness
  - Avalanche Energy Rated (UIS)
- Optimal Efficiency and Operation
  - Low Cost
  - Simple Gate Drive Circuitry
  - Low Figure-of-Merit (FOM): $R_{on} \times Q_g$
  - Fast Switching
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Consumer Electronics
  - Displays (LCD or Plasma TV)
- Server and Telecom Power Supplies
  - SMPS
- Industrial
  - Welding
  - Induction Heating
  - Motor Drives
- Battery Chargers

RoHS COMPLIANT

HALOGEN FREE

ORDERING INFORMATION

Package	D²PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHB8N50D-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

| PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	
Gate-Source Voltage			V_{GS}	± 30	V
Gate-Source Voltage AC (f > 1 Hz)				30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	I_D	8.7	A
		$T_C = 100$ °C		5.5	
Pulsed Drain Current[a]			I_{DM}	18	
Linear Derating Factor				1.25	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	29	mJ
Maximum Power Dissipation			P_D	156	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Drain-Source Voltage Slope	$T_J = 125$ °C		dV/dt	24	V/ns
Reverse Diode dV/dt[d]				0.37	
Soldering Recommendations (Peak Temperature)[c]	for 10 s			300	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, L = 2.3 mH, $R_g = 25$ Ω, $I_{AS} = 5$ A.
c. 1.6 mm from case.
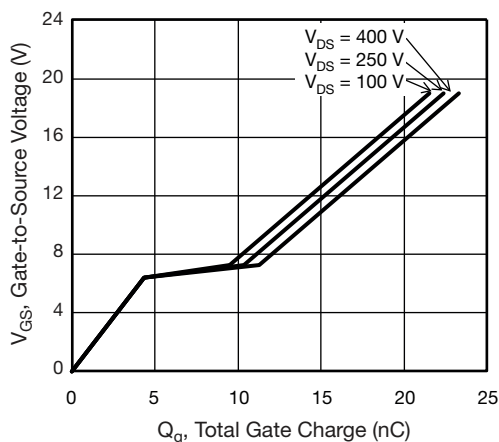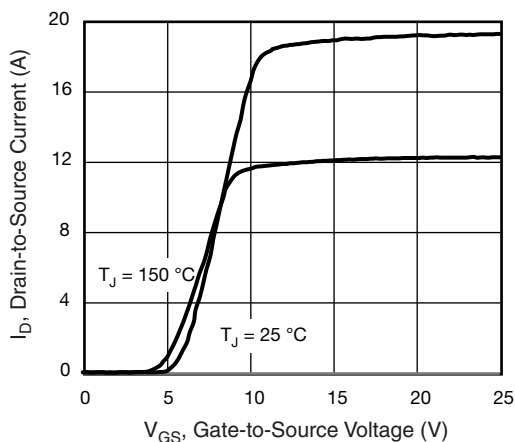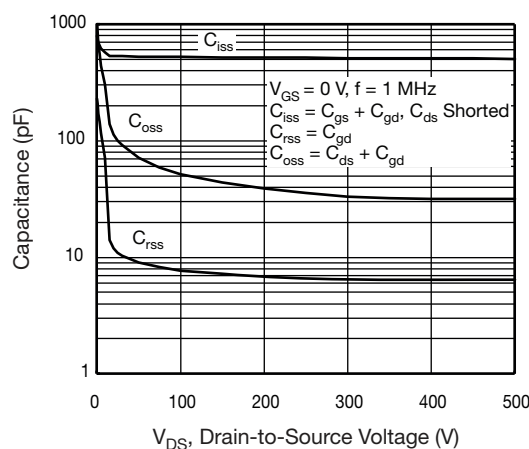d. $I_{SD} \le I_D$, starting $T_J = 25$ °C.
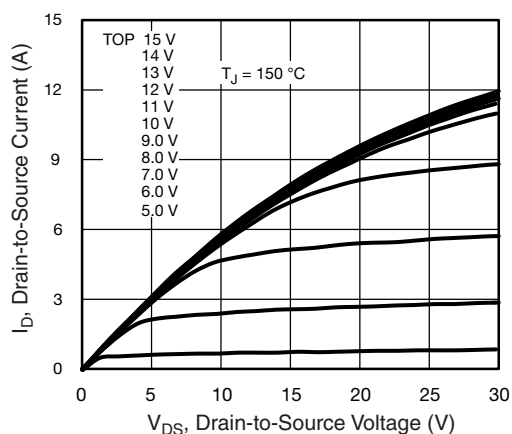
THERMAL RESISTANCE RATINGS

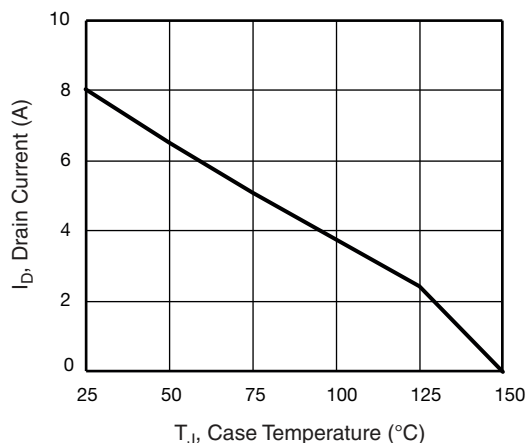| PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.8	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 250 µA		-	0.58	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		3	-	5	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V		-	-	1	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 4 A	-	0.70	0.85	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = 20 V, I_D = 4 A		-	3	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz		-	527	-	pF
Output Capacitance	C_{oss}			-	52	-	
Reverse Transfer Capacitance	C_{rss}			-	8	-	
Effective Output Capacitance, Energy Related[b]	$C_{o(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		-	46	-	
Effective Output Capacitance, Time Related[c]	$C_{o(tr)}$			-	64	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 4 A, V_{DS} = 400 V	-	15	30	nC
Gate-Source Charge	Q_{gs}			-	4	-	
Gate-Drain Charge	Q_{gd}			-	7	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 4 A, R_g = 9.1 Ω, V_{GS} = 10 V		-	13	26	ns
Rise Time	t_r			-	16	32	
Turn-Off Delay Time	$t_{d(off)}$			-	17	34	
Fall Time	t_f			-	11	22	
Gate Input Resistance	R_g	f = 1 MHz, open drain		-	1.8	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	8	A
Pulsed Diode Forward Current	I_{SM}			-	-	32	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 4 A, V_{GS} = 0 V		-	-	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 4 A, dI/dt = 100 A/µs, V_R = 20 V		-	308	-	ns
Reverse Recovery Charge	Q_{rr}			-	1.8	-	µC
Reverse Recovery Current	I_{RRM}			-	11	-	A

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.

b. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

c. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - **Typical Output Characteristics**

Fig. 4 - **Normalized On-Resistance vs. Temperature**

Fig. 2 - **Typical Output Characteristics**

Fig. 5 - **Typical Capacitance vs. Drain-to-Source Voltage**

Fig. 3 - **Typical Transfer Characteristics**

Fig. 6 - **Typical Gate Charge vs. Gate-to-Source Voltage**
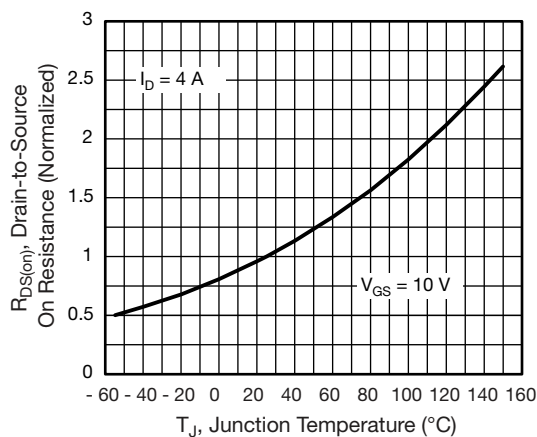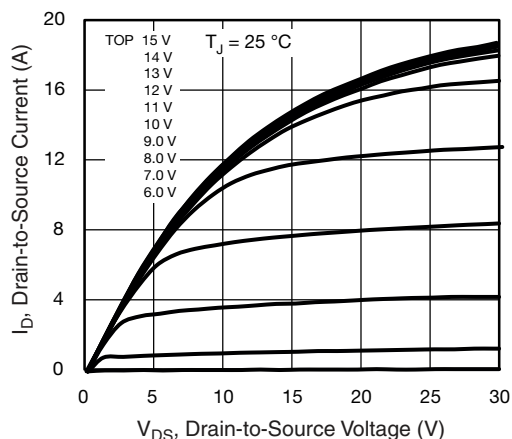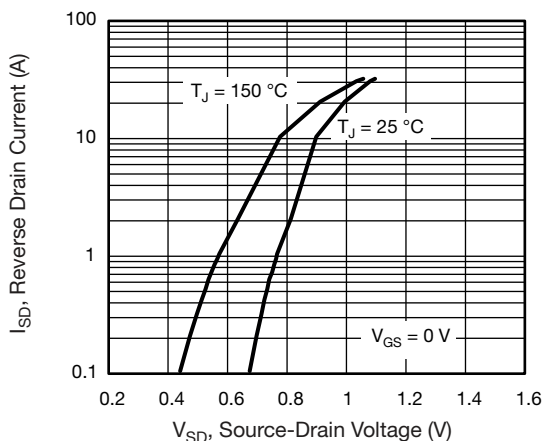
Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified
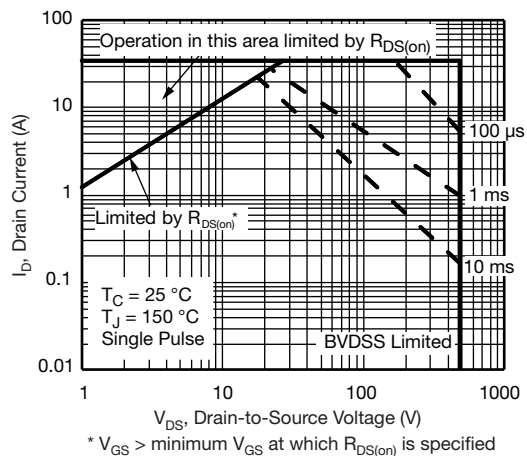
Fig. 8 - Maximum Safe Operating Area
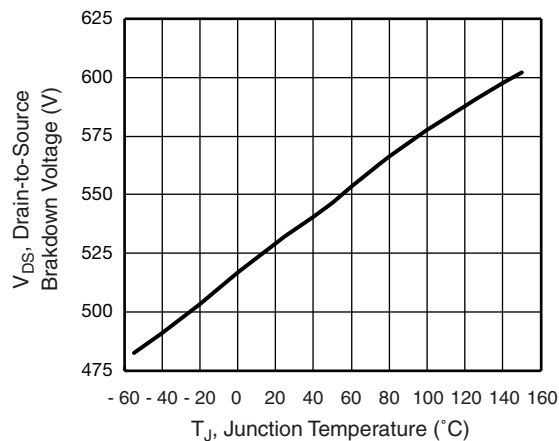
Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature
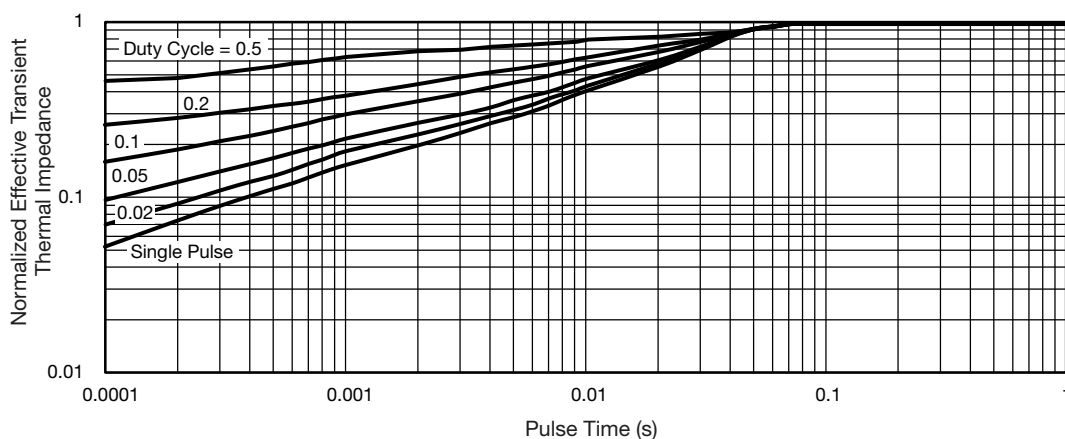
Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case
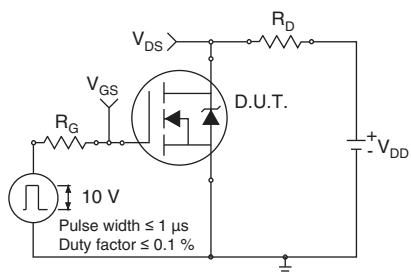
Fig. 12 - Switching Time Test Circuit

Fig. 13 - Switching Time Waveforms
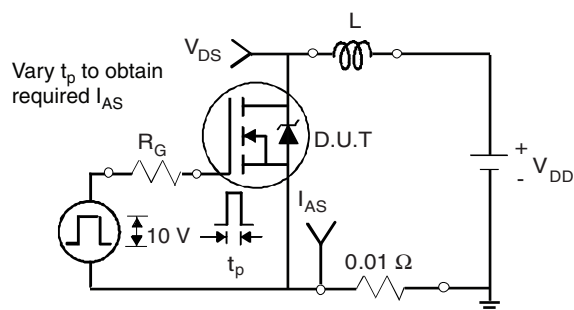
Fig. 14 - Unclamped Inductive Test Circuit
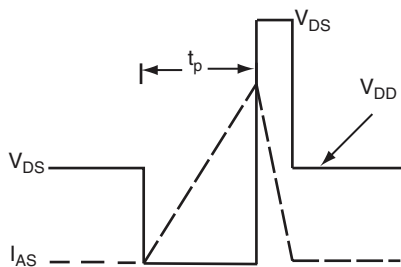
Fig. 15 - Unclamped Inductive Waveforms

Fig. 16 - Basic Gate Charge Waveform
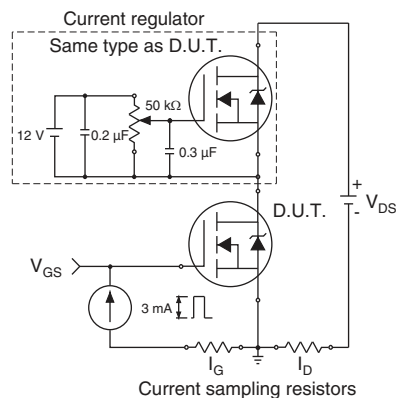
Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

D.U.T.

③

Circuit layout considerations
- Low stray inductance
- Ground plane
- Low leakage inductance current transformer

②

④

- dV/dt controlled by R_g
- Driver same type as D.U.T.
- I_{SD} controlled by duty factor "D"
- D.U.T. - device under test

R_g

V_{DD}

①

① Driver gate drive

P.W.

Period

$D = \dfrac{P.W.}{Period}$

$V_{GS} = 10\ V^a$

② D.U.T. I_{SD} waveform

Reverse recovery current

Body diode forward current

dI/dt

③ D.U.T. V_{DS} waveform

Diode recovery dV/dt

V_{DD}

Re-applied voltage

Body diode forward drop

④ Inductor current

Ripple ≤ 5 %

I_{SD}

Note

a. $V_{GS} = 5\ V$ for logic level devices

Fig. 18 - For N-Channel

For technical questions, contact: hvm@vishay.com

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