

# N-Channel 40-V (D-S) Fast Switching MOSFET

## PRODUCT SUMMARY

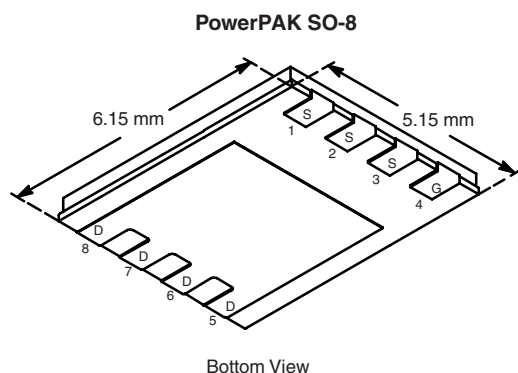
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
40	0.0061 at $V_{GS} = 10$ V	23.6	105

## FEATURES

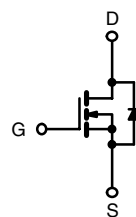
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 %  $R_g$  Tested
- High Threshold Voltage at High Temperature



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



**Ordering Information:** Si7444DP-T1-E3 (Lead (Pb)-free)  
Si7444DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

## ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ , unless otherwise noted

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	40		V
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	I <sub>D</sub>	23.6	14	A
	T <sub>A</sub> = 70 °C		18.9	11.2	
Pulsed Drain Current		I <sub>DM</sub>	60		
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	4.5	1.6	
Avalanche Current		I <sub>AS</sub>	45		
Avalanche Energy		E <sub>AS</sub>	100		
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5.4	1.9	W
	T <sub>A</sub> = 70 °C		3.4	1.2	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b,c</sup>			260		

## THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ s	$R_{thJA}$	18	23	$^\circ\text{C/W}$
	Steady State		52	65	
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	1.0	1.3	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile ([www.vishay.com/bpg?73257](http://www.vishay.com/bpg?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

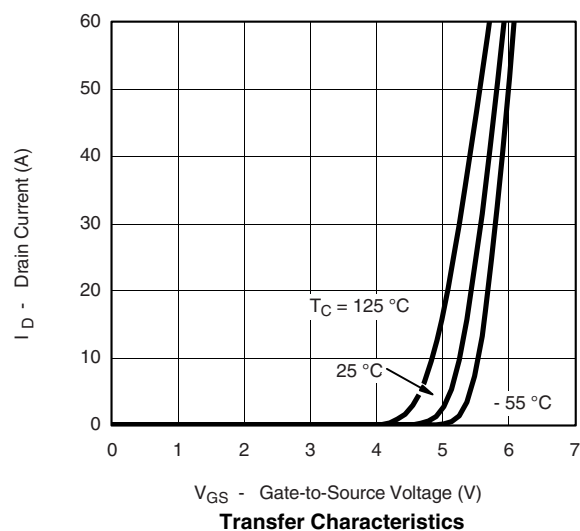
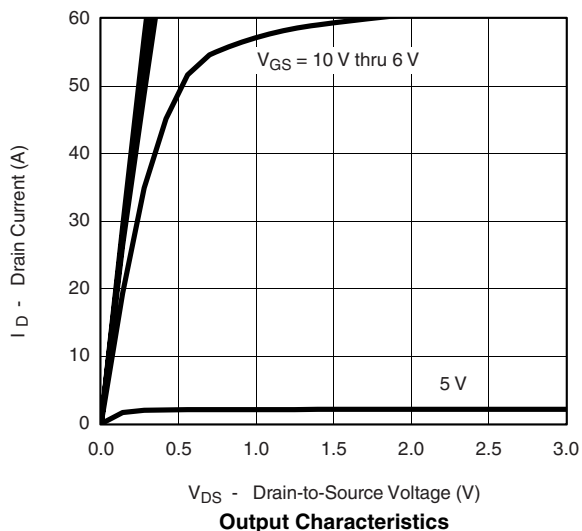
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.4		4.5	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 55\text{ }^{\circ}\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$ , $V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 23.6\text{ A}$		0.005	0.0061	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 23.6\text{ A}$		56		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 4.5\text{ A}$ , $V_{GS} = 0\text{ V}$		0.76	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 23.6\text{ A}$		105	160	nC
Gate-Source Charge	$Q_{gs}$			39.4		
Gate-Drain Charge	$Q_{gd}$			21.7		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.5	1.0	1.5	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}$ , $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 6\text{ }\Omega$		45	70	ns
Rise Time	$t_r$			30	45	
Turn-Off Delay Time	$t_{d(off)}$			90	135	
Fall Time	$t_f$			45	70	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 4.5\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$		45	70	

Notes:

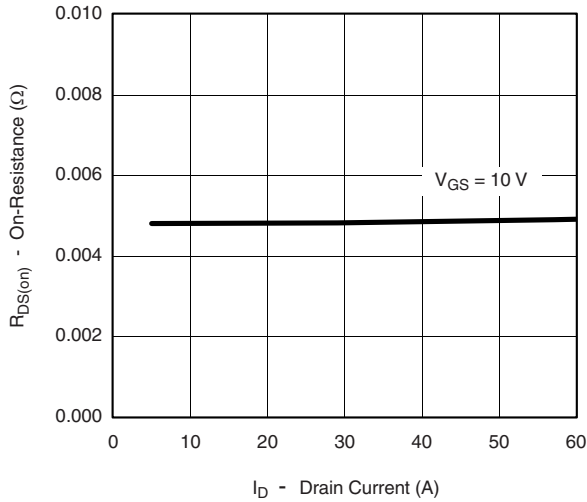
a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

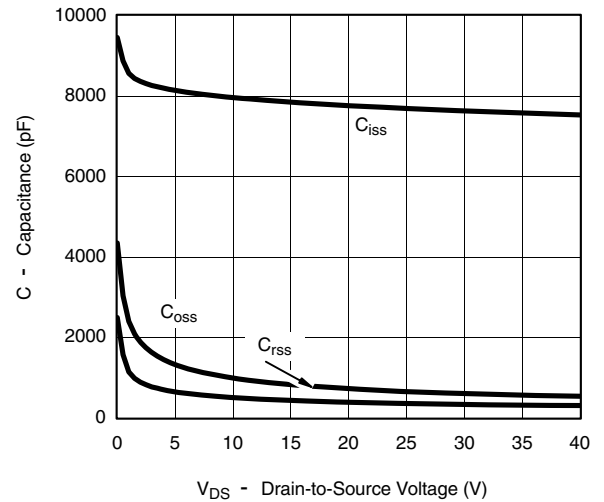
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS**  $25\text{ }^{\circ}\text{C}$ , unless otherwise noted

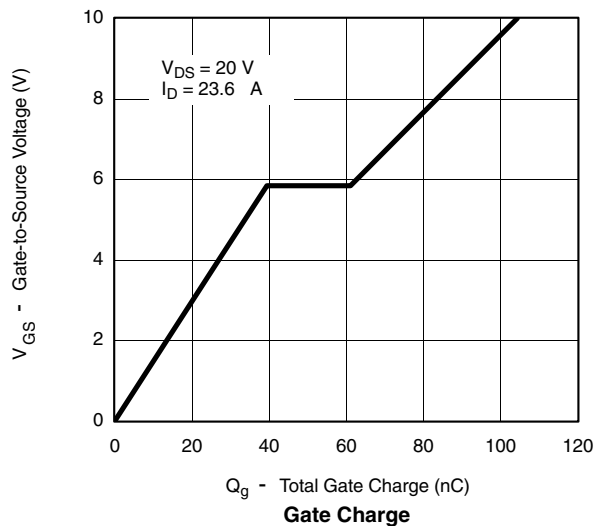
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



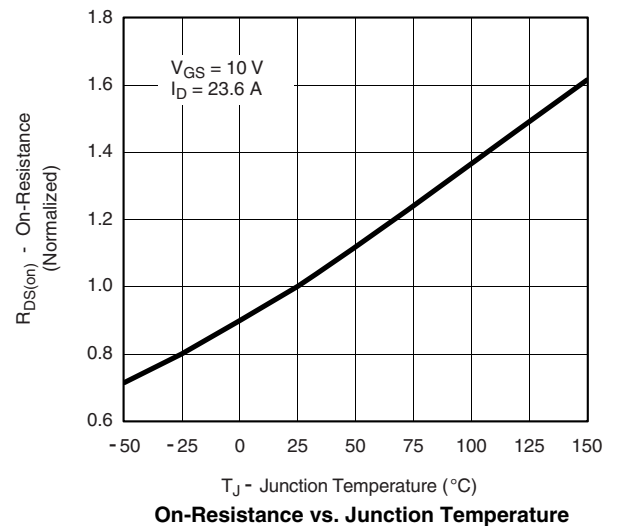
On-Resistance vs. Drain Current



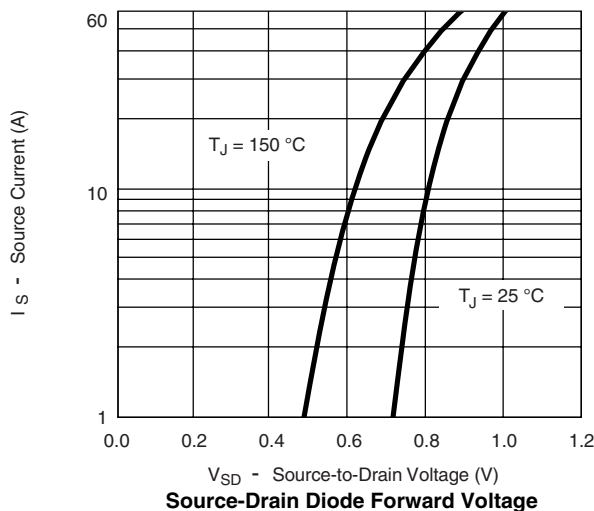
Capacitance



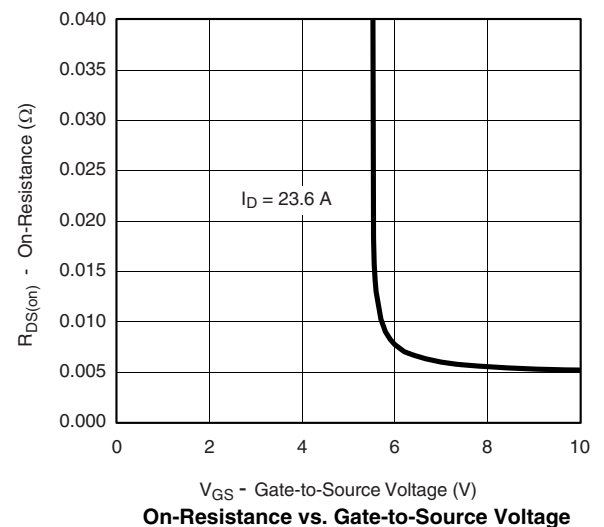
Gate Charge



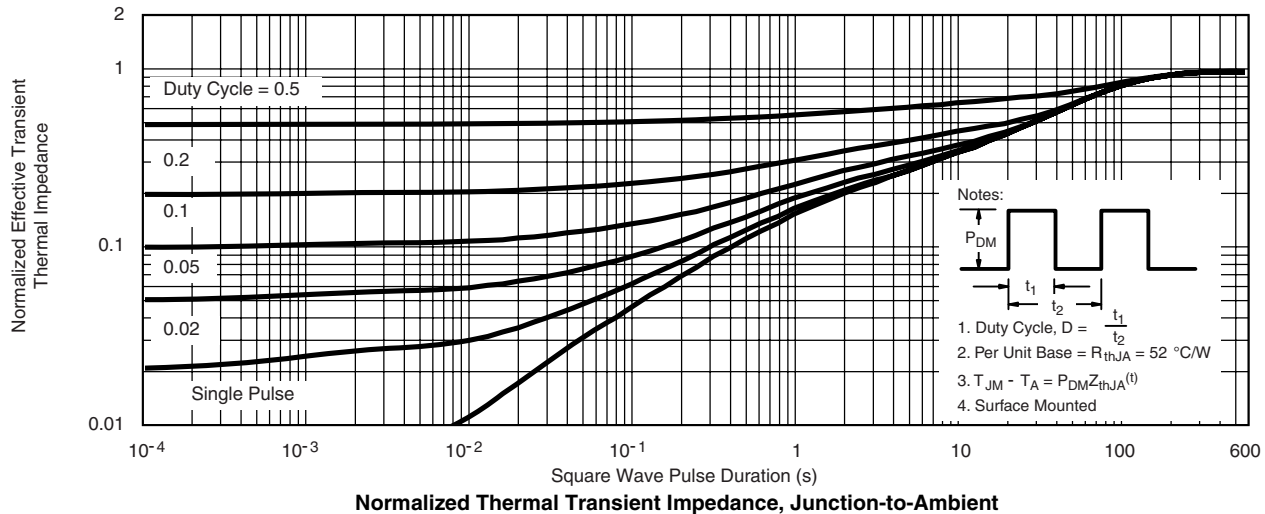
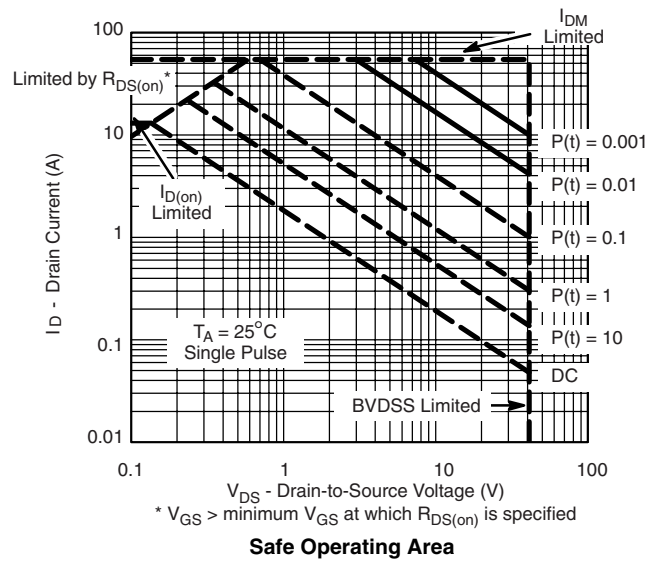
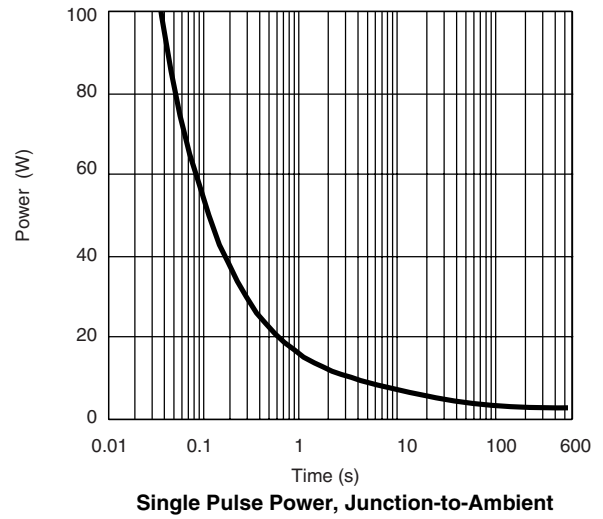
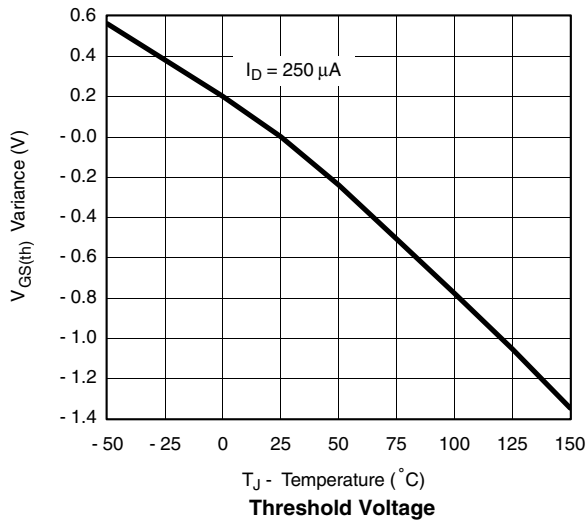
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

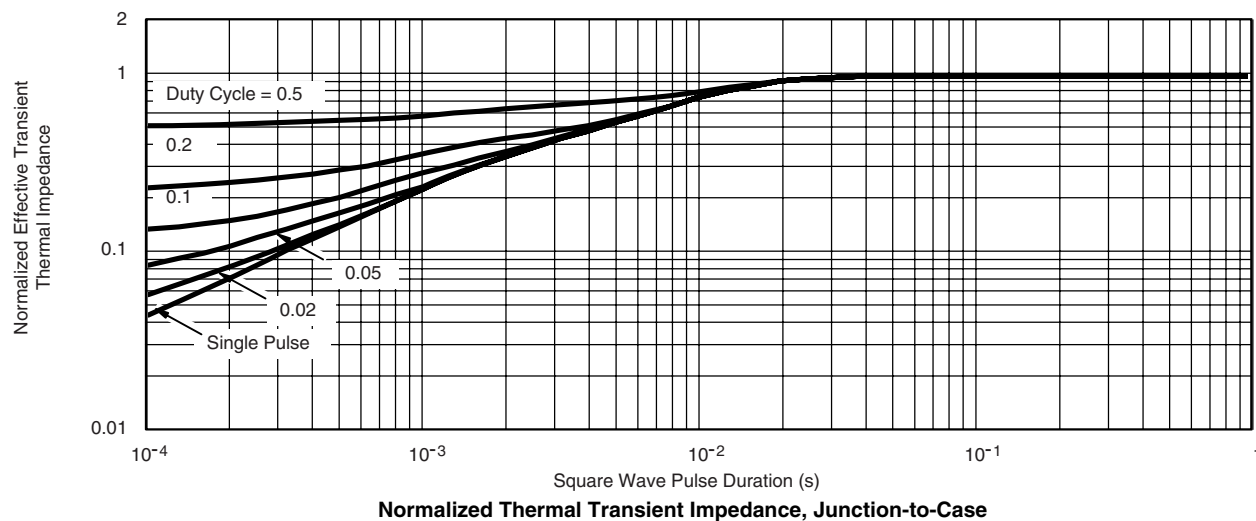


On-Resistance vs. Gate-to-Source Voltage

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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