

RoHS

COMPLIANT

HALOGEN

FREE

Single 8-Ch/Differential 4-Ch Latchable Analog Multiplexers

DESCRIPTION

The DG428, DG429 analog multiplexers have on-chip address and control latches to simplify design in microprocessor based applications. Break-before-make switching action protects against momentary crosstalk of adjacent input signals.

The DG428 selects one of eight single-ended inputs to a common output, while the DG429 selects one of four differential inputs to a common differential output.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

The silicon-gate CMOS process enables operation over a wide range of supply voltages. The absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed and an epitaxial layer prevents latchup.

On-board TTL-compatible address latches simplify the digital interface design and reduce board space in bus-controlled systems such as data acquisition systems, process controls, avionics, and ATE.

FEATURES

- Halogen-free according to IEC 61249-2-21 Definition
- Low R_{DS(on)}: 55 Ω
- Low Charge Injection: 1 pC
- **On-Board TTL Compatible Address Latches**
- High Speed t_{TBANS}: 160 ns
- Break-Before-Make
- Low Power Consumption: 0.3 mW
- Compliant to RoHS Directive 2002/95/EC

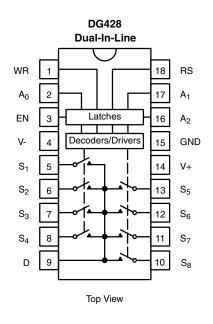
BENEFITS

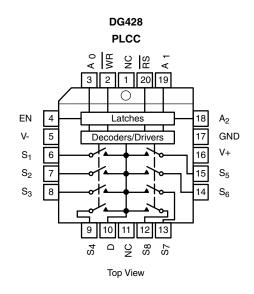
- Improved System Accuracy
- Microprocessor Bus Compatible
- Easily Interfaced
- Reduced Crosstalk
- High Throughput
- Improved Reliability

APPLICATIONS

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- **Communication Systems**
- Microprocessor-Controlled Analog Systems
- Medical Instrumentation

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

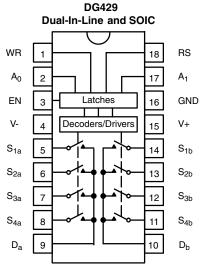




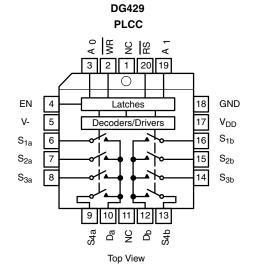
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FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View



TRUTH TABLE - DG429

TRU	TRUTH TABLE - DG428										
	8	-Chanr	el Sing	le-End	ed Mult	iplexer					
A ₂	A ₁	A ₀	EN	WR	RS	On Switch					
Latching											
х	х	х	х	F	1	Maintains previous switch condition					
Reset											
х	х	х	х	х	0	None (latches cleared)					
Trans	parent	Operati	on								
Х	Х	Х	0	0	1	None					
0	0	0	1	0	1	1					
0	0	1	1	0	1	2					
0	1	0	1	0	1	3					
0	1	1	1	0	1	4					
1	0	0	1	0	1	5					
1	0	1	1	0	1	6					
1	1	0	1	0	1	7					
1	1	1	1	0	1	8					

Differential 4-Channel Multiplexer													
A ₁	A ₀	EN	WR	RS	On Switch								
Latchir	Latching												
Х	х	х	Ţ	1	Maintains previous switch condition								
Reset													
х	х	х	х	0	None (latches cleared)								
Transp	arent Op	peration											
Х	Х	0	0	1	None								
0	0	1	0	1	1								
0	1	1	0	1	2								
1	0	1	0	1	3								
1	1	1	0	1	4								
	' = V _{AL} ≤ ' = V _{AH} ≥												

X = Don't Care

ORDERING INFORMATION - DG428							
Temp Range	Package	Part Number					
	19 pin Plastia DIP	DG428DJ					
- 40 °C to 85 °C	18-pin Plastic DIP	DG428DJ-E3					
- 40 0 10 85 0	20-pin PLCC	DG428DN					
	20-pin PLOC	DG428DN-E3					

ORDERING INFORMATION - DG429									
Temp Range	Package	Part Number							
	18-pin Plastic DIP	DG429DJ							
	To-pin Flastic DiF	DG429DJ-E3							
- 40 °C to 85 °C	20-pin PLCC	DG429DN							
- 40 0 10 65 0	20-pi11 PLOC	DG429DN-E3							
	18-pin Widebody SOIC	DG429DW							
	To-pill widebody SOIC	DG429DW-E3							

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ABSOLUTE MAXIMUM RATINGS ($T_A = 25 ^{\circ}C$, unless otherwise noted)

F	Parameter	Symbol	Limit	Unit	
Voltagos Referenced to V	V+		44		
Voltages Referenced to V-	GND		25	v	
Digital Inputs ^a , V _S , V _D			(V-) - 2 V to (V+) + 2 V or 30 mA, whichever occurs first	, v	
Current (Any Terminal)			30	mA	
Peak Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle Max)			100	IIIA	
Storage Temperature	(AK Suffix)		- 65 to 150	°C	
Slorage remperature	(DJ, DN Suffix)		- 65 to 125		
	18-pin Plastic DIP ^c		470		
Power Dissipation (Package) ^b	18-pin CerDIP ^d		900	mW	
	20-pin PLCC ^f		800	11100	
	28-Pin Widebody SOIC ^f		450		

Notes:

a. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads soldered or welded to PC board.

c. Derate 6.3 mW/°C above 75 °C.

d. Derate 12 mW/°C above 75 °C.

e. Derate 10 mW/°C above 75 °C.

f. Derate 6 mW/°C above 75 °C.

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SPECIFICATIONS ^a										
		Test Conditior Unless Otherwise S					uffix to 125 °C		uffix to 85 °C	
		V+ = 15 V, V- = - 15 V,	$\overline{WR} = 0,$							
Parameter	Symbol	$\overline{\text{RS}}$ = 2.4 V, V _{IN} = 2.4	V, 0.8 V ^f	Temp. ^b	Typ. ^c	Min. ^d	Max. ^d	Min. ^d	Max. ^d	Unit
Analog Switch	-									
Analog Signal Range ^e	V _{ANALOG}			Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	R _{DS(on)}	V _D = ± 10 V, V _{AL} = I _S = - 1 mA, V _{AH} =	2.4 V	Room Full	55		100 125		100 125	Ω
Greatest Change in R _{DS(on)} Between Channels ^g	$\Delta R_{DS(on)}$	- 10 V < V _S < 10 I _S = - 1 mA) V	Room	5					%
Source Off Leakage Current	I _{S(off)}	$V_{S} = \pm 10 \text{ V},$ $V_{EN} = 0 \text{ V}, \text{ V}_{D} = \pm$	10 V	Room Full	± 0.03	- 0.5 - 50	0.5 50	- 0.5 - 50	0.5 50	
		V _{EN} = 0 V	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100	
Drain Off Leakage Current	I _{D(off)}	$V_D = \pm 10 V$ $V_S = \pm 10 V$	DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	nA
Drain On Lookage Current	I	$V_{S} = V_{D} = \pm 10 V$ $V_{EN} = 2.4 V$	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100	
Drain On Leakage Current	I _{D(on)}	V _{AL} = 0.8 V V _{AH} = 2.4 V	DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	
Digital Control								•		
Logic Input Current	I _{AH}	V _A = 2.4 V		Full	0.01		1		1	
Input Voltage High	'AH	V _A = 15 V		Full	0.01		1		1	μA
Logic Input Current Input Voltage Low	I _{AL}	V _{EN} = 0 V, 2.4 V, V _A RS = 0 V, WR =		Full	- 0.01	- 1		- 1		po t
Logic Input Capacitance	C _{in}	f = 1 MHz		Room	8					pF
Dynamic Characteristics	-								-	
Transition Time	t _{TRANS}	See Figure 5		Room Full	150		250 300		250 300	
Break-Before-Make Interval	t _{OPEN}	See Figure 4		Full	30	10		10		
Enable and Write Turn-On Time	t _{ON(EN,WR)}	See Figure 6 an	d 7	Room Full	90		150 225		150 225	ns
Enable and Reset Turn-Off Time	t _{OFF(EN,RS)}	See Figure 6 an		Room Full	55		150 300		150 300	
Charge Injection	Q	V _{GEN} = 0 V, R _{GEN} C _L = 1 nF, See Fig	ure 9	Room	1					рС
Off Isolation	OIRR	$V_{EN} = 0 V, R_L = 30$ $C_L = 15 pF, V_S = 7$ f = 100 kHz	V _{RMS}	Room	- 75					dB
Source Off Capacitance	C _{S(off)}	$V_{S} = 0 V, V_{EN} = 0 V, f$	= 1 MHz	Room	11					
Drain Off Capacitance	C _{D(off)}	$V_{D} = 0 V$	DG428 DG429	Room Room	40 20					pF
Drain On Capacitance	Cara	V _{EN} = 0 V f = 1 MHz	DG429 DG428	Room	54					pr
Drain On Capacitance	C _{D(on)}		DG429	Room	34					
Minimum Input Timing Requirer	nents								-	
Write Pulse Width	t _W			Full		100		100		
A _X , EN Data Set Up time	t _S	See Figure 2		Full		100		100		ns
A _X , EN Data Hold Time	t _H			Full Full		10		10		
Reset Pulse Width	t _{RS}	V _S = 5 V, See Figu	V _S = 5 V, See Figure 3			100		100		
Power Supplies										
Positive Supply Current	l+	$V_{EN} = V_A = 0, \overline{RS}$	= 5 V	Room	20		100		100	μA
Negative Supply Current	I-			Room	- 0.001	- 5		- 5		



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		Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V, WR = 0,				A Suffix - 55°C to 125 °C		D Suffix - 40 °C to 85 °C			
Parameter	Symbol	$\overline{RS} = 2.4 \text{ V}, \text{ V}_{IN} = 2.4 \text{ V}$		Temp. ^b	Typ. ^c	Min. ^d	Max. ^d	Min. ^d	Max. ^d	Unit	
Analog Switch	 ,						<u> </u>	I			
Analog Signal Range ^e	V _{ANALOG}			Full		0	12	0	12	V	
Drain-Source On-Resistance	R _{DS(on)}	V _D = ± 10 V, V _{AL} = I _S = - 500 μA, V _{AH} =	0.8 V = 2.4 V	Room	80		150		150	Ω	
R _{DS(on)} Match ^g	$\Delta R_{DS(on)}$	0 V < V _S < 10 I _S = - 1 mA	V	Room	5					%	
Source Off Leakage Current	I _{S(off)}	V _S = 0 V, 10 V V _{EN} = 0 V, V _D = 10		Room Full	± 0.03	- 0.5 - 50	0.5 50	- 0.5 - 50	0.5 50		
Drain Off Leakage Current	I _{D(off)}	$V_{\rm D} = 0 \text{ V}, 10 \text{ V}$ $V_{\rm S} = 10 \text{ V}, 0 \text{ V}$	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100		
Brain en Leakage earrent	·D(01)	$V_{EN} = 0 V$	DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	nA	
Durin On Lookana Quimant		$V_{\rm S} = V_{\rm D} = 0 \text{ V}, 10 \text{ V}$ $V_{\rm EN} = 2.4 \text{ V}$	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100		
Drain On Leakage Current	I _{D(on)}	$V_{AL} = 0.8 V$ $V_{AH} = 2.4 V$	DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50		
Digital Control			•								
Logic Input Current Input Voltage High	I _{AH}	V _A = 2.4 V V _A = 12 V		Full Full			1		1		
Logic Input Current Input Voltage Low	I _{AL}	V _{EN} = 0 V, 2.4 V, V _A RS = 0 V, WR =	_= 0 V	Full		- 1		- 1		μA	
Dynamic Characteristics				1							
Transition Time	t _{TRANS}	S ₁ = 10 V/ 2 V, S ₈ = 2 See Figure 5	V/ 10 V	Room Full	160		280 350		280 350		
Break-Before-Make Interval	t _{OPEN}	See Figure 4		Room Full	40	25 10		25 10			
Enable and WriteTurn-On Time	t _{ON(EN,WR)}	S ₁ = 5 V See Figure 6 an	d 7	Room Full	110		300 400		300 400	ns	
Enable and Reset Turn-Off Time	t _{OFF(EN,RS)}	S ₁ = 5 V See Figure 6 an	d 8	Room Full	70		300 400		300 400		
Charge Injection	Q	V _{GEN} = 6 V, R _{GEN} C _L = 1 nF, See Fig		Room	4					pC	
Off Isolation	OIRR	$V_{EN} = 0 V, R_L = 30$ $C_L = 15 pF, V_S = 7$ f = 100 kHz	00 Ω V _{RMS}	Room	- 75					dB	
Minimum Input Timing Requirem	nents										
Write Pulse Width	t _W			Full		100		100			
A _X , EN Data Set Up time	t _S	See Figure 2		Full		100		100		ns	
A _X , EN Data Hold Time	t _H			Full		10		10		113	
Reset Pulse Width	t _{RS}	V _S = 5 V, See Fig	ure 3	Full		100		100			
Power Supplies	_										
Positive Supply Current	I+	$V_{EN} = 0 V, V_A = 0, \overline{R}$	S = 5 V	Room	20		100		100	μA	

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 $^{\circ}$ C, full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

e. Guaranteed by design, not subject to production test.

f. V_{IN} = input voltage to perform proper function.

g.
$$\Delta R_{DS(on)} = \left(\frac{R_{DS(on)} MAX - R_{DS(on)} MIN}{R_{DS(on)} AVE}\right) \times 100 \%$$

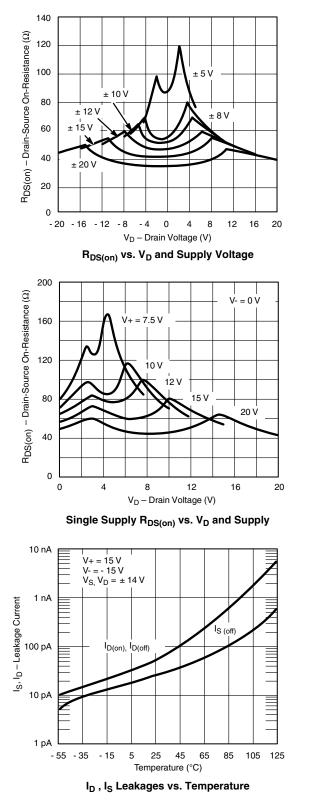
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

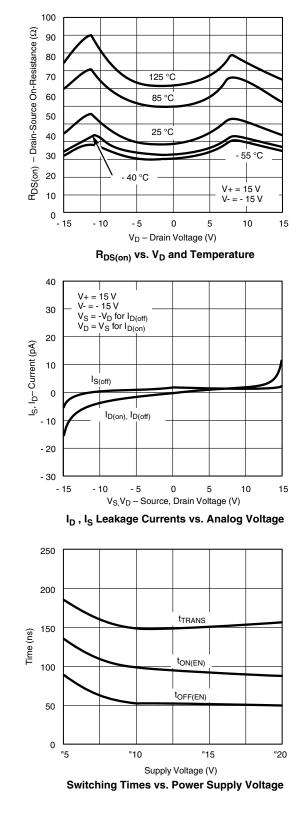
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TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



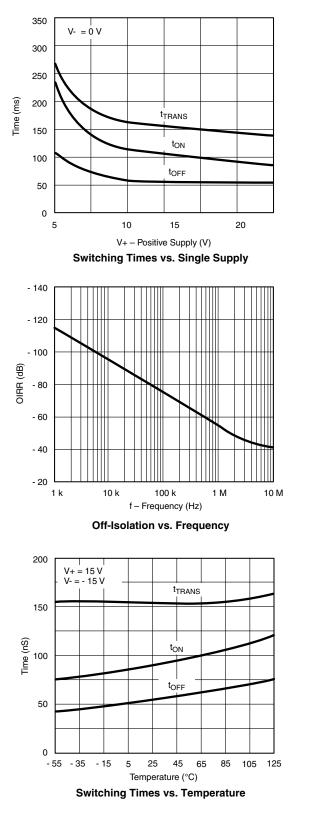


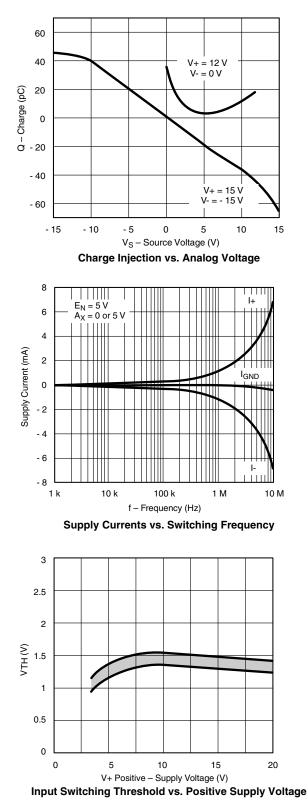
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DG428, DG429 Vishay Siliconix

TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

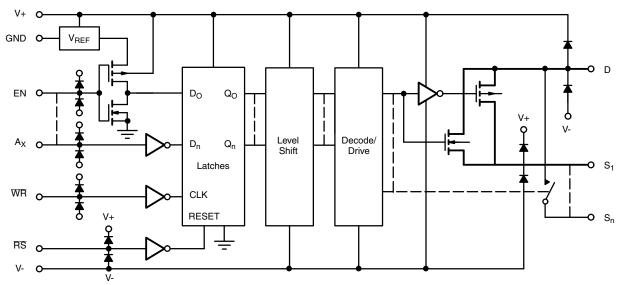




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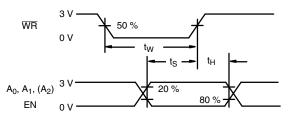
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SCHEMATIC DIAGRAM (Typical Channel)

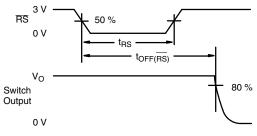




TIMING DIAGRAMS









TEST CIRCUITS

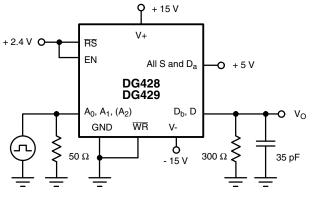


Figure 4. Break-Before-Make

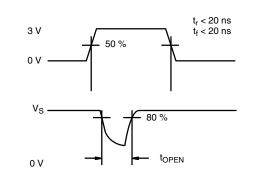
Logic

Input

Switch

Output

 V_{O}

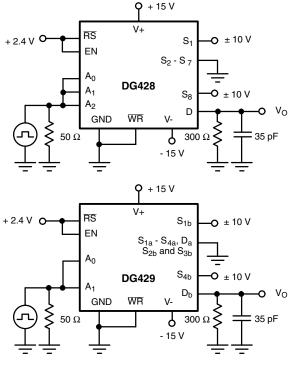


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TEST CIRCUITS



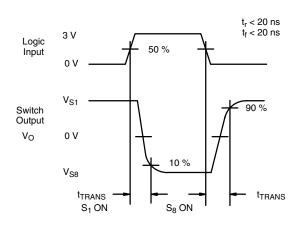
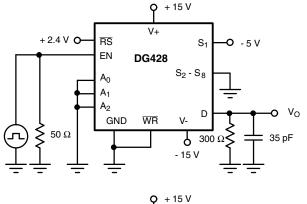
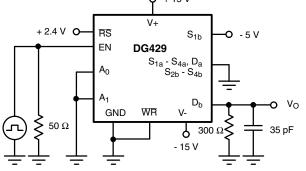


Figure 5. Transition Time





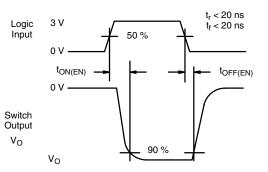
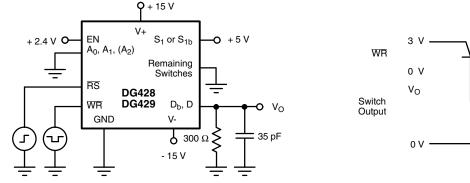


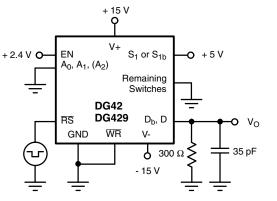
Figure 6. Enable t_{ON}/t_{OFF} Time

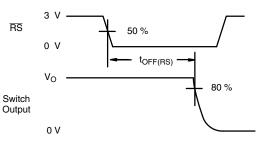
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TEST CIRCUITS





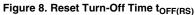




50 %

t_{ON(WR)}

20 %



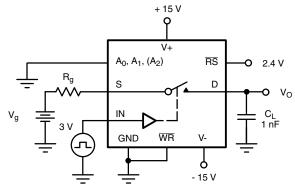
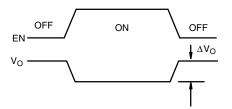


Figure 9. Charge Injection



 ΔV_O is the measured voltage error due to charge injection. The charge in coulombs is Q = $C_L \; x \; \Delta V_O$

Document Number: 70063 S11-1350–Rev. K, 04-Jul-11





DETAILED DESCRIPTION

The internal structure of the DG428, DG429 includes a 5 V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel n- and p-channel MOSFETs (see Figure 1).

The input protection on the logic lines A_0 , A_1 , A_2 , EN and control lines \overline{WR} , \overline{RS} shown in Figure 1 minimizes susceptibility to ESD that may be encountered during handling and operational transients.

The logic interface is a CMOS logic input with its supply voltage from an internal + 5 V reference voltage. The output of the input inverter feeds the data input of a D type latch. The level sensitive D latch continuously places the D_X input signal on the Q_X output when the \overline{WR} input is low, resulting in transparent latch operation. As soon as \overline{WR} returns high the latch holds the data last present on the D_n input, subject to the "Minimum Input Timing Requirements" table.

Following the latches the Q_n signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting ensures full on/off switch operation for any analog signal level between the V+ and V- supply rails.

The EN pin is used to enable the address latches during the $\overline{\text{WR}}$ pulse. It can be hard wired to the logic supply or to V+ if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{\text{RS}}$ pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The $\overline{\text{WR}}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

APPLICATIONS HINTS

Bus Interfacing

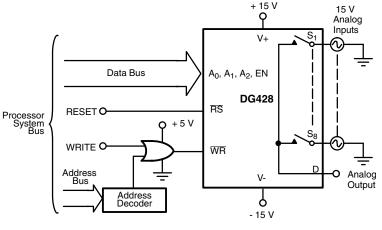
The DG428, DG429 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 on) until the microprocessor determines it is necessary to turn different switches on or turn all switches off (see Figure 10).

The input latches become transparent when \overline{WR} is held low; therefore, these multiplexers operate by direct command of the coded switch state on A₂, A₁, A₀. In this mode the DG428 is identical to the popular DG408. The same is true of the DG429 versus the popular DG409.

During system power-up, $\overline{\text{RS}}$ would be low, maintaining all eight switches in the off state. After $\overline{\text{RS}}$ returned high the DG428 maintains all switches in the off state.

When the system program performs a write operation to the address assigned to the DG428, the address decoder provides a \overline{CS} active low signal which is gated with the WRITE (\overline{WR}) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the \overline{WR} signal returns to the high state, (positive edge) the input latches of the DG428 save the data from the DATA BUS. The coded information in the A₀, A₁, A₂ and EN latches is decoded and the appropriate switch is turned on.

The EN latch allows all switches to be turned off under program control. This becomes useful when two or more DG428s are cascaded to build 16-line and larger multiplexers.





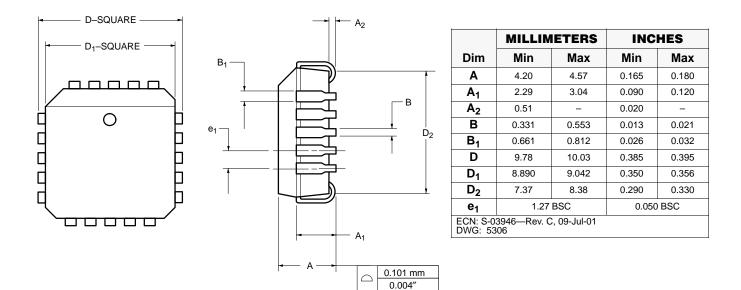
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70063.

Document Number: 70063 S11-1350–Rev. K, 04-Jul-11



Package Information Vishay Siliconix

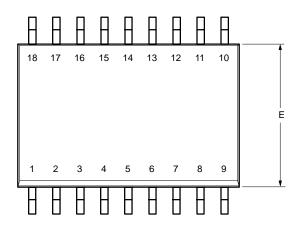
PLCC: 20-LEAD



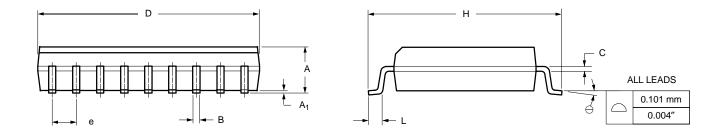


Package Information Vishay Siliconix

SOIC (WIDE-BODY): 18-LEAD



	MILLIM	IETERS	INC	HES			
Dim	Min	Max	Min	Max			
Α	2.15	2.90	0.085	0.114			
A ₁	0.10	0.30	0.004	0.012			
В	0.35	0.45	0.014	0.018			
С	0.23	0.28	0.009	0.011			
D	11.25	12.45	0.443	0.490			
Е	7.25	8.00	0.285	0.315			
е	1.27	BSC	0.050	BSC			
Н	9.80	10.60	0.386	0.417			
L	0.60	1.00	0.024	0.039			
Φ	0°	8°	0°	8°			
ECN: S-03946—Rev. C, 09-Jul-01 DWG: 5302							





Vishay

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