

N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}$ (Ω)	I _D (A)	Q _g (Typ.)		
20	0.003 at $V_{GS} = 4.5 \text{ V}$	29	57		
	0.0042 at V _{GS} = 2.5 V	25	57		

FEATURES

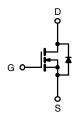
- · Halogen-free available
- TrenchFET[®] Power MOSFETS: 2.5 V Rated



- PWM (Q_{gd} and R_g) Optimized
- 100 % R_g Tested

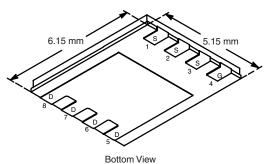
APPLICATIONS

 Low-Side MOSFET in Synchronous Buck DC/DC Converters in Servers and Routers



N-Channel MOSFET

PowerPAK® SO-8



Ordering Information: Si7864ADP-T1-E3 (Lead (Pb)-free)

Si7864ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T	$_{A}$ = 25 °C, unles	ss otherwise n	oted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _{.I} = 150 °C) ^a	T _A = 25 °C	I _D	29	18	
Continuous Diam Current (1) = 130 °C)	T _A = 70 °C		25	14	
Pulsed Drain Current (10 μs Pulse Width)		I _{DM}	60		Α
Continuous Source Current (Diode Conduction) ^a		I _S	4.5	1.6	
Avalanche Current	L = 0.1 mH	I _{AS}	40		
Maximum Dawar Dissination	T _A = 25 °C	- P _D	5.4	1.9	W
Maximum Power Dissipation ^a	T _A = 70 °C		3.4	1.2	VV
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		C

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Marrian una lumation ta Analaianti	t ≤ 10 s	R _{thJA}	18	23		
Maximum Junction-to-Ambient ^a	Steady State		50	65	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.0	1.5		

Notes

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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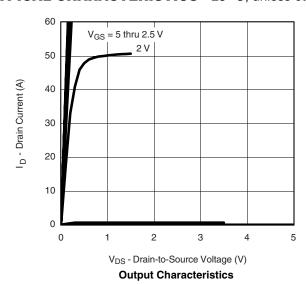
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					<u> </u>		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.6		1.5	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 ^{\circ}\text{C}$			1 5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	30		3	Α	
Drain-Source On-State Resistance ^a	D	$V_{GS} = 4.5 \text{ V}, I_D = 29 \text{ A}$		0.0023	0.003		
	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, I_D = 25 \text{ A}$		0.0032	0.0042	Ω	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 6 \text{ V}, I_{D} = 29 \text{ A}$		70		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = 4.5 \text{ A}, V_{GS} = 0 \text{ V}$		0.70	1.2	V	
Dynamic ^b	<u>'</u>		•	<u>'</u>			
Input Capacitance	C _{iss}			5330		pF	
Output Capacitance	C _{oss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1240			
Reverse Transfer Capacitance	C _{rss}			680			
Total Gate Charge	Q_g			57	85		
Gate-Source Charge	Q_{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 29 \text{ A}$		8.5		nC	
Gate-Drain Charge	Q_{gd}			17			
Gate Resistance	R_g		0.5	1.3	2	Ω	
Turn-On Delay Time	t _{d(on)}			40	60		
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_L = 10 \Omega$		44	65		
Turn-Off Delay Time t _{d(c}		$I_D\cong$ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		150	240	ns	
Fall Time	t _f			72	110		
Source-Drain Reverse Recovery Time	t _{rr}	$I_F = 2.9 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		57	80		

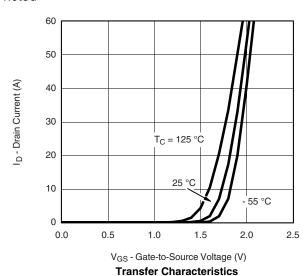
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

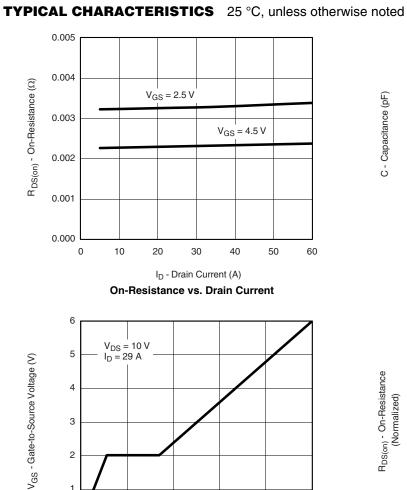


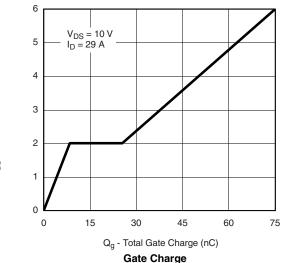


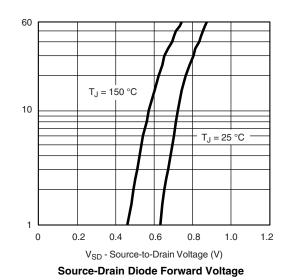


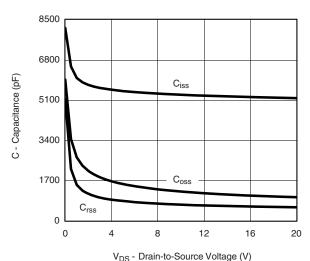


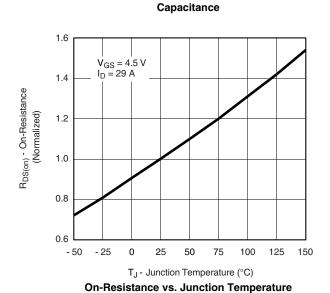


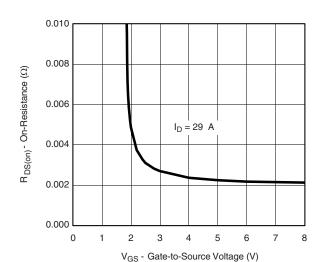












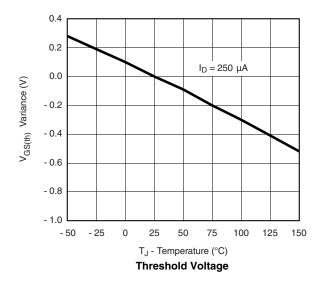
On-Resistance vs. Gate-to-Source Voltage

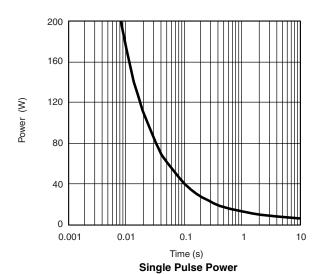
Is - Source Current (A)

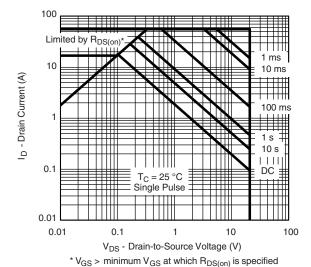
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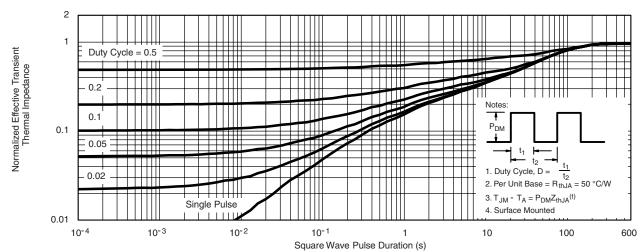
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted







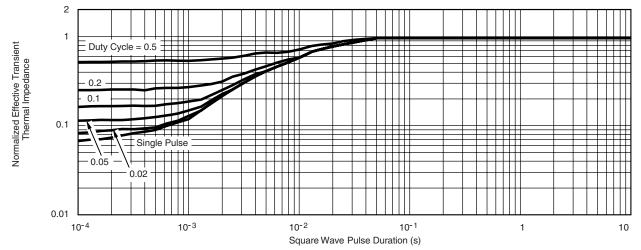
Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73166.

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