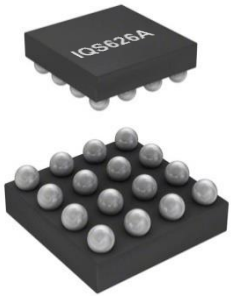
IQS626A DATASHEET

Trackpad, ProxFusion® and Hall-Effect Sensor Controller

Device overview

The **IQS626A** ProxFusion® IC is a 14-channel multi-sensor controller with best in class sensitivity, signal to noise ratio and power consumption. The device offers either:



WLCSP(1.62x1.62)-16 package

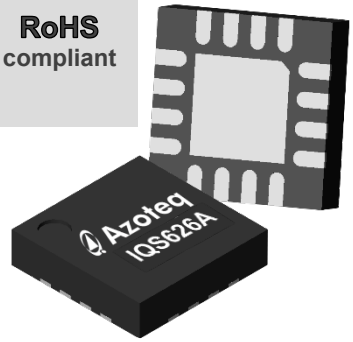
Representation only

- Ultra-low power capacitive wake-up channel with optional associated GPIO output.
- Hall-effect channel with optional associated GPIO output.
- A selectable 2x3 or 3x3 mutual-capacitive trackpad.
- 3 configurable generic ProxFusion® channels, ideal for wear detection with temperature tracking and inductive force sensing.
- A selection of 4 configurable Reset User Interfaces (RUI) with GPIO outputs for autonomous operation without need for configuration by the master device.
  - RUI1
    - Self-Capacitive Channel with GPIO3 Output
    - Hall Channel with GPIO4 Output
    - Temperature Tracking Channel active for Hall Temperature Compensation
  - RUI2
    - Self-Capacitive Channel with GPIO3 Output
    - Touch-Hold Output on GPIO4
  - RUI3
    - I2C Address Strap on GPIO4
  - RUI4
    - GPIO4 Forced Active

Main Features

- Highly flexible 14-channel ProxFusion® controller.
- Each generic channel can be contabd with three different types of external connections or one of two internal options.
- 8 external sensor pad connections:
  - Self/Mutual-Capacitive sensors
  - Self/Mutual-Inductive sensors
  - Dedicated reference sensor for environmental / mechanically sensitive designs
- Internal sensor option:
  - Hall-effect sensor
  - Temperature sensor
- Serial scanning (Single ProxFusion® engine) – up to 14 time-slots
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering

RoHS compliant



QFN(3x3)-16 package

Representation only

- Differential measurements (reference channels)
- Debounce & hysteresis
- Dual direction trigger indication
- Linearization of measurement data

> Built-in user-interface options:
  - Trackpad (2x3 or 3x3 projected trackpad setups) with:
    - 2-dimensional coordinate output,
    - axial flick/swipe, tap and hold gesture detection.
  - Dedicated ultra-low power channel for power mode handling
> Wide Range of Capacitance Detection, Wide Electrode Range of 0 to 200pF.
> Internal sensitivity optimization in high capacitive load conditions.
> Multiple custom signal level event triggers (e.g. proximity, touch, deep touch).
> Capacitive resolution: down to 0.02fF
> Automatic reference channel UI's for temperature and mechanical effects. Assign reference channel to any single or group of channels.
> Options for reduced RF emissions for integration in RF sensitive environments (wide range of charge transfer frequency options).
> I2C Interface with IRQ (RDY) line
> A GPIO output which can be associated with the touch state of any channel. Configurable as open-drain, active low (default) or push-pull, active high.
> Option to configure a GPIO as an address selection pin
> Hall effect sensor standalone output:
  - Product order options for specific power-on GPIO output requirement
  - For requirements that range from a single magnet (zero offset) to multiple magnets (field offset present) – e.g. Single magnet docking vs. dual magnet docking
  - Power-on options from >10mT magnet changes
> Supply voltage: 1.8V (-2%) to 3.6V
> Package options: WLCSP-16 (1.62 x 1.62 x 0.5mm), QFN16 (3 x 3 x 0.8mm)

Applications

> Hall docking detection.
> Small form factor trackpads and sliders.
> Ultra-low power capacitive wake-up and proximity buttons.
> Wear detection with temperature compensation.
> Inductive force sensing.
> Tailored for True Wireless Stereo (TWS) devices.
> Capacitive wake-up, capacitive trackpad/slider, wear detection and magnetic dock detection possible with a single device.
> Touch area coordinate & multi-button design
> Electronic keypads or pin pads

Contents

1 Block diagram

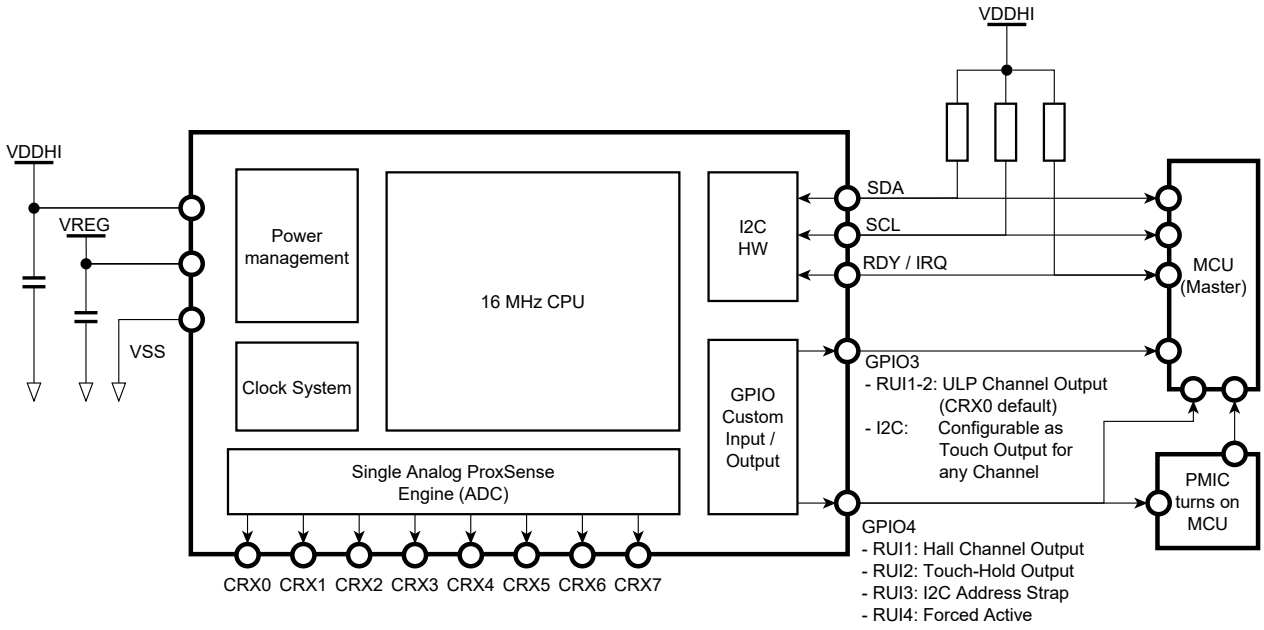
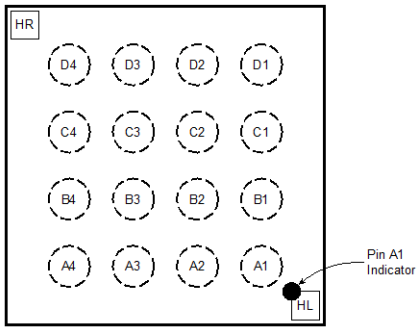


Figure 1.1: Functional block diagram

2 Terminal configuration and function

2.1 WLCSP-16 Pin diagrams

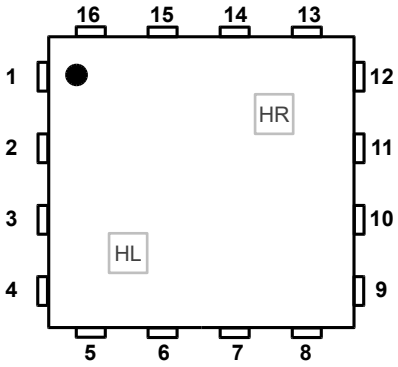


Pin no.	Signal name	Pin no.	Signal name
A1	CRX6	C1	VDDHI
A2	CRX2	C2	GPIO3
A3	CRX0	C3	SDA
A4	CRX5	C4	VSS
B1	CRX4	D1	GPIO4
B2	CRX1	D2	SCL
B3	CRX3	D3	RDY
B4	CRX7	D4	VREG

Area name	Signal name	Area name	Signal name
HR (internal)	HALL RIGHT	HL (internal)	HALL LEFT

Figure 2.1: 16-pin WLCSP package (Top view)

2.2 QFN-16 Pin diagram



Pin no.	Signal name	Pin no.	Signal name
1	GPIO3	9	CRX3
2	GPIO4	10	CRX5
3	VDDHI	11	CRX7
4	CRX6	12	VSS
5	CRX4	13	VREG
6	CRX2	14	RDY
7	CRX1	15	SDA
8	CRX0	16	SCL
		17	TAB - floating

Area name	Signal name	Area name	Signal name
HR (internal)	HALL RIGHT	HL (internal)	HALL LEFT

Figure 2.2: 16-pin QFN package (Top view)

2.3 Pin attributes

Pin no.		Signal name	Signal type[1]	Buffer type	Power source	Reset state after BOR[2]
WLCSP16	QFN16					
A1	4	CRX6	Analog	LVCMOS	VREG	High-Z
A2	6	CRX2	Analog	LVCMOS	VREG	High-Z
A3	8	CRX0	Analog	LVCMOS	VREG	High-Z
A4	10	CRX5	Analog	Analog	VREG	High-Z
B1	5	CRX4	Analog	LVCMOS	VREG	High-Z
B2	7	CRX1	Analog	LVCMOS	VREG	High-Z
B3	9	CRX3	Analog	LVCMOS	VREG	High-Z
B4	11	CRX7	Analog	Analog	VREG	High-Z
C1	3	VDDHI	P	Power	N/A	High-Z
C2	1	GPIO3	O	LVCMOS	VDDHI	High-Z
C3	15	SDA	I/O	LVCMOS	VDDHI	High-Z
C4	12	VSS	P	Power	N/A	High-Z
D1	2	GPIO4	I/O	LVCMOS	VDDHI	High-Z
D2	16	SCL	I/O	LVCMOS	VDDHI	High-Z
D3	14	RDY	I/O	LVCMOS	VDDHI	High-Z
D4	13	VREG	O	Power	VDDHI	High-Z
	17	TAB	Floating	N/A	N/A	N/A

[1] Signal Types: I = Input, O = Output, I/O = Input or Output
[2] High-Z = High-impedance with Schmitt trigger and pullup or pulldown (if available) disabled

2.4 Signal descriptions

Function	Signal name	Pin no.		Pin type	Description
		WLCSP16	QFN16		
ProxFusion®	CRX6	A1	4	I/O	ProxFusion® channel
	CRX2	A2	6	I/O	
	CRX0	A3	8	I/O	
	CRX5	A4	10	I/O	
	CRX4	B1	5	I/O	
	CRX1	B2	7	I/O	
	CRX3	B3	9	I/O	
	CRX7	B4	11	I/O	
GPIO	GPIO4	D1	2	I/O	Custom Output (HALL, Touch&Hold, Forced high on reset) / Address input (high: 0x44, low: 0x45)
	GPIO3	C2	1	O	Custom Touch Out
I^2C	SCL	D2	16	I/O	I^2C clock
	SDA	C3	15	I/O	I^2C data
	RDY (IRQ)	D3	14	O	I^2C event mode interrupt
Power	VDDHI	C1	3	P	Power supply
	VREG	D4	13	O	ProxFusion® regulator external decoupling capacitor
	VSS	C4	12	P	Power ground

3 Schematics, Layout and Component Selection

3.1 Basic Schematic

Figure 3.1 below shows a minimal reference schematic for the most basic of IQS626A applications. Note that the connections of CRX0 through CRX7 will differ substantially for each application. See

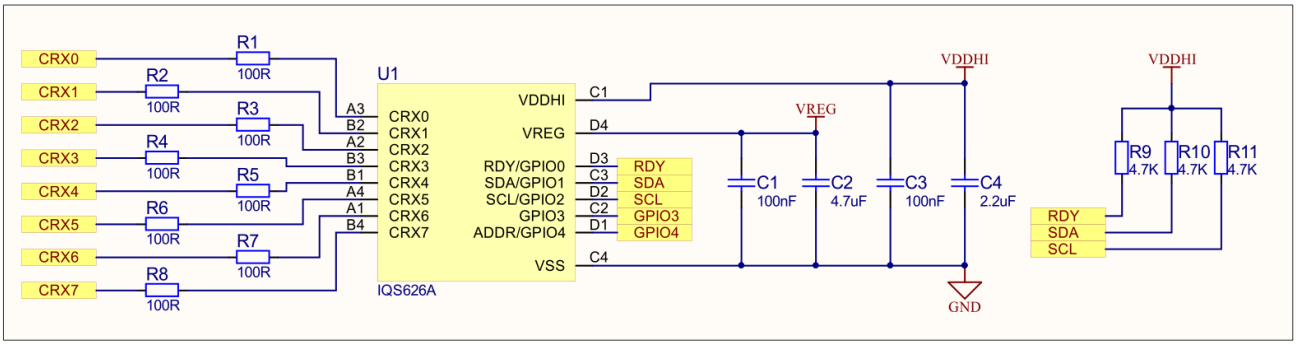


Figure 3.1: Reference Schematic

3.2 Power Rail Capacitors

3.2.1 Power Supply Capacitors

It is recommended to place a 2.2µF and 100pF parallel combination of low-ESR ceramic decoupling capacitors between the VDDHI and VSS nets. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters) with the smaller capacitor being the closer than the larger capacitor. Figure 3.2 illustrates this.

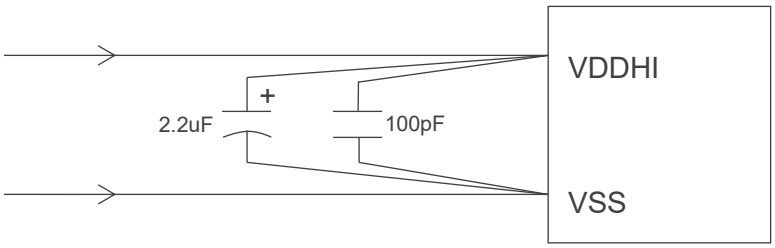


Figure 3.2: Recommended power supply capacitors.

3.2.2 Voltage Regulator Capacitors

The VREG pin requires at least a 1µF capacitor to regulate the LDO voltage regulator internal to the device. It is also recommended to place a 100pF capacitor between VREG and VSS for improved noise immunity. These capacitors should be placed as close to the IC as possible with the smaller capacitor being closer than the larger capacitor. *Figure 3.3* Illustrates this.

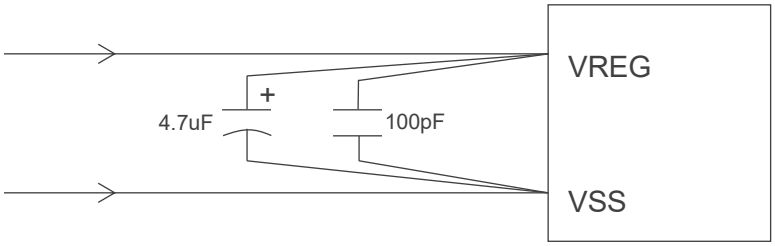


Figure 3.3: Recommended voltage regulator capacitors.

3.2.3 aCapacitor Selection

In section *3.2.1* and section *3.2.2* it is recommended to place 2 capacitors on between both VDDHI and GND and VREG and GND. In both cases a larger value capacitor and a smaller value capacitor is recommended. The larger value capacitors for VDDHI and VREG are respectively referred to as C_{VDDHI} and C_{VREG} in this section. This smaller value capacitors are for noise immunity purposes, the same value should be used for VDDHI and VREG.

3.2.3.1 Low Inline-Resistance Power Supplies

For supplies with low in-line resistance and high current output capability is it recommended to ensure that $C_{VREG} > 2C_{VDDHI}$. This is to prevent a known ESD risk as explained below.

Known risk: The IQS626A will not recover from ESD events is the following conditions are met:

- VDDHI source is present with low impedance path and high current sourcing capability
- $C_{VDDHI} > C_{VREG}$

With these conditions met, the source keeps VDDHI above the BOD level during the ESD event but drains the VREG capacitor during sleep mode causing a unique sleep-mode BOD event keeping the IC in reset. This only recovers when forcing a POR on VDDHI.

Table 3-1 Shows recommended values for C_{VDDHI} and C_{VREG} values for power supplies with low inline-resistance.

Table 3-1: Recommended capacitor values for low inline-resistance power supplies.

Maximum Report Rate (ms)	Minimum		Recommended for General Design	
	C_{VREG} (µF)	C_{VDDHI} (µF)	C_{VREG} (µF)	C_{VDDHI} (µF)
64	2.2	1	4.7	2.2
128	2.2	1		
160	3.3	1.5		
256	3.9	1.5		

3.2.3.2 High Inline-Resistance Power Supplies

For supplies with a high in-line resistance (such as battery with high series resistance) it is recommended to ensure that $C_{VDDHI} > C_{VREG}$ to prevent an unexpected dip on VDDHI when the sensor wakes from sleep-mode and re-charges the VREG capacitor. *Table 3-2* shows recommended capacitor values for power supplies with high inline-resistance.

Table 3-2: Recommended capacitor values for high inline-resistance power supplies.

Maximum Report Rate (ms)	Minimum		Recommended for General Design	
	C_{VREG} (µF)	C_{VDDHI} (µF)	C_{VREG} (µF)	C_{VDDHI} (µF)
64	2.2	2.2	4.7	4.7
128	2.2	2.2		
160	3.3	3.3		
256	3.9	3.3		

4 Electrical Specifications

4.1 Recommended Operating Conditions

Table 4-1: Recommended operating conditions.

Parameter	Description	Min.	Typ.	Max.	Unit
VDDHI	Supply voltage applied at VDDHI pin	1.764		3.6	V
VREG	Regulator output at VREG	1.62		1.7	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	-40		85	ºC
C_{VDDHI}	Recommended capacitor at VDDHI [1]	1[2]	2.2	10	µF
C_{VREG}	Recommended external buffer capacitor at VREG, ESR≤ 200mΩ	0.8	4.7	10	µF
$C_{ELECTRODE}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks	N/A		200	pF

4.2 Absolute maximum ratings

Table 4-2: Absolute maximum ratings.

Parameter	Min.	Max.	Unit
Voltage applied at VDDHI pin to VSS	-0.3	+3.6	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDDHI + 0.3 (3.6V max)	V
Storage temperature, T_{stg}	-40	125	ºC

4.3 Electrostatic Discharge ratings

Table 4-3: Electrostatic ratings.

Parameter	Description		Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[3]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[4]	±500	

4.4 Timing and switching characteristics

4.4.1 Reset levels

Table 4-4: Reset levels.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{BOR, safe}$	Safe BOR power down level[5]	V_{DDHI} slope ≥ 100V/s	0.6			V
V_{DDHI}	Power-up/down level (Reset trigger)	V_{DDHI} slope ≥ 100V/s			1.7	V
V_{REG}	Power-up/down level (Reset trigger)				1.55	V

4.4.2 Miscellaneous timings

Table 4-5: Miscellaneous timings.

Parameter	Description	Min.	Typ.	Max.	Unit
f_{xfer}	Charge transfer frequency (derived from f_{SYS})	-2%		+2%	V

[1] A capacitor tolerance of ±20% or better is required

[2] The minimum value ensures optimal performance in various low power modes that are possible

[3] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

[4] JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

[5] A safe BOR can be correctly generated only if V_{DDHI} drops below this voltage before it rises.

4.4.3 HALL sensing characteristics

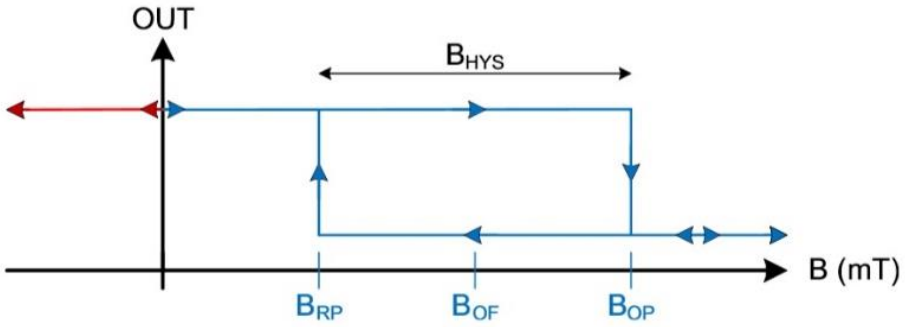


Figure 4.1: Magnet trigger level description (active low output)

Table 4-6: Example power-on magnet detection options.

HALL sensor setup	Output type	B_{RP} (mT)	B_{OP} (mT)[1]	B_{HYS} (mT)	B_{RP} and B_{OP} accuracy (mT) -20°C to 60°C[2]
Threshold Example 1	Direct	9.5	10	0.5	± 4
Threshold Example 3	Direct	42.5	45	2.5	± 18
Adjustable Threshold	I2C / Direct	25 – 100% of B_{OP} (default 95%)	Software register	0 – 75% of B_{OP} (default 5%)	± 40%

4.4.4 I²C

Specified over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Parameter		Test conditions	V_{DDHI}	Min	Typ	Max	Unit
f_{SYS}	System clock frequency			15.68	16.00	16.32	MHz
f_{SCL}	SCL clock frequency		1.8 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	1.8 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	1.8 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		1.8 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		1.8 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	1.8 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter	N/A	1.8 V, 3 V	No pulse suppression filter			ns
t_{LOW}	Clock low time-out	N/A	1.8 V, 3 V	TBD			ms

[1] Preliminary values based on expected single and dual magnet applications. These values are flexible and different ordering options will exist. Typical trigger level at 25degC

[2] Applicable when no temperature compensation is used. When using temperature compensation, accuracy is drastically improved.

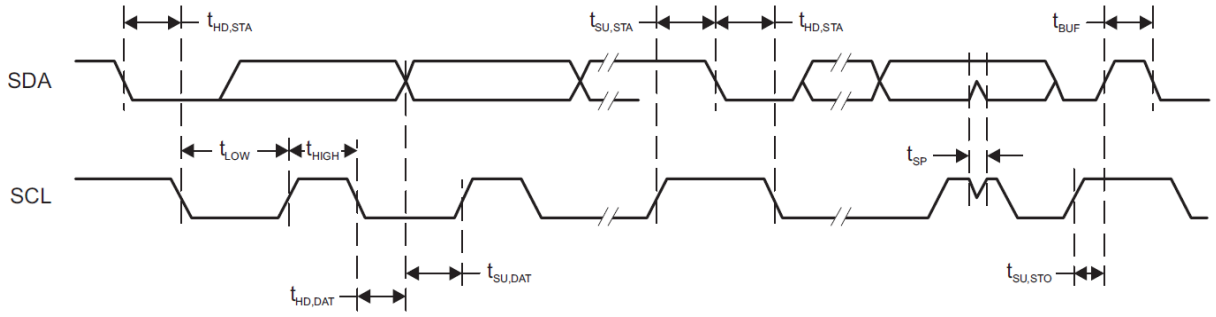


Figure 4.2: I²C mode timing

4.5 Current consumption

4.5.1 Reset User Interfaces

Table 4-7 lists current consumption during RUI operation with no communication. Rui power mode is Normal Power Mode with a Report Rate of 150ms and a Ready Timeout of 30ms. Since the full Ready Timeout time can lapse, the total time for each report cycle is 180ms. For the open drain "Ready Type" measurements, a 4.7kΩ pull-up resistor was used.

Table 4-7: Current consumption during RUI operation before any communication.

Magnetic Field (mT)	Supply Voltage (V)	Ready Type	RUI	Averaged Current (µA)		
				Min.	Typ.	Max.
0	1.8	Open Drain, Active Low	RUI1	-	80.89	-
			RUI2	-	74.91	-
			RUI3	-	TBD	-
			RUI4	-	TBD	-
		Push Pull, Active High	RUI1	-	12.98	-
			RUI2	-	6.13	-
			RUI3	-	TBD	-
			RUI4	-	TBD	-
	3.3	Open Drain, Active Low	RUI1	-	138.21	-
			RUI2	-	132.04	-
			RUI3	-	TBD	-
			RUI4	-	TBD	-
		Push Pull, Active High	RUI1	-	23.65	-
			RUI2	-	15.32	-
			RUI3	-	TBD	-
			RUI4	-	TBD	-
18	1.8	Open Drain, Active Low	RUI1	-	84.41	-
			RUI2	-	74.91	-
			RUI3	-	TBD	-
			RUI4	-	TBD	-
		Push Pull, Active High	RUI1	-	15.53	-
			RUI2	-	6.13	-
			RUI3	-	TBD	-
			RUI4	-	TBD	-
	3.3	Open Drain, Active Low	RUI1	-	139.07	-
			RUI2	-	132.04	-
			RUI3	-	TBD	-
			RUI4	-	TBD	-
		Push Pull, Active High	RUI1	-	20.08	-
			RUI2	-	15.32	-
			RUI3	-	TBD	-
			RUI4	-	TBD	-

Table 4-8 lists current consumption measurements after reset has been acknowledged and Event Mode has been enabled. The IQS626A device is then placed into the required Power Mode and current is measured. No other settings are altered. Since the ready pin is not toggled during this measurement, the Ready Type settings is not listed.

Table 4-8: Current consumption during with default RUI settings and Event Mode enabled.

Magnetic Field (mT)	Supply Voltage (V)	RUI	Averaged Current Consumption (uA)								
			Normal Power Mode (150ms Report Rate)			Low Power Mode (150ms Report Rate)			Ultra-Low Power Mode (256ms Report Rate)		
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
0	1.8	RUI1	-	14.32	-	-	14.32	-	-	3.08	-
		RUI2	-	8.48	-	-	8.48	-	-	2.96	-
		RUI3	-	TBD	-	-	TBD	-	-	TBD	-
		RUI4	-	TBD	-	-	TBD	-	-	TBD	-
	3.3	RUI1	-	14.91	-	-	14.91	-	-	3.61	-
		RUI2	-	9.15	-	-	9.15	-	-	3.61	-
		RUI3	-	TBD	-	-	TBD	-	-	TBD	-
		RUI4	-	TBD	-	-	TBD	-	-	TBD	-
18	1.8	RUI1	-	14.02	-	-	14.02	-	-	3.06	-
		RUI2	-	8.48	-	-	8.48	-	-	2.96	-
		RUI3	-	TBD	-	-	TBD	-	-	TBD	-
		RUI4	-	TBD	-	-	TBD	-	-	TBD	-
	3.3	RUI1	-	14.48	-	-	14.84	-	-	3.72	-
		RUI2	-	9.15	-	-	9.15	-	-	3.61	-
		RUI3	-	TBD	-	-	TBD	-	-	TBD	-
		RUI4	-	TBD	-	-	TBD	-	-	TBD	-

5 Identification

5.1 Revision Identification

The device revision information is included as part of the top-side marking on the device package as shown below. The hardware revision is also stored as shown in the table below:

Description	Address	Offset 0	Offset 1
Product number (1st byte), Version number (2nd byte)	00h	0x51	0x01 (pre-production) 0x02 (production)
Hardware revision (1st byte), Reserved development code (2nd byte)	01h	0x0A (pre-production) 0x2D (production)	Reserved

5.2 WLCSP-16 Device Identification

The device type can be identified from the top-side marking on the device package as shown below:

626A = device name (IQS626A)

zz = configuration / xx = batch code (AA, AB …. ZZ)

v = IC version mark

ppp = product code

● = Pin A1 indicator

5.3 QFN16 Device Identification

The device type can be identified from the top-side marking on the device package as shown below:

626A = device name (IQS626A)

zz = configuration

xx = batch code

v = IC version mark

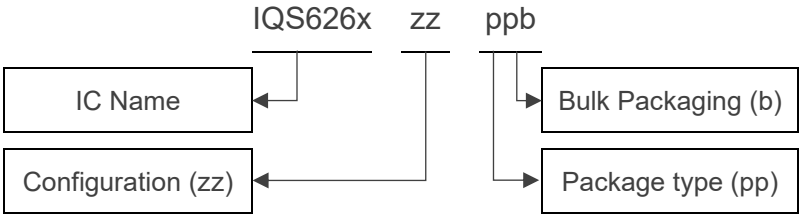
ppp = Product code

● = Pin A1 indicator

A device identification value is also stored as shown in the table above.

6 Ordering information

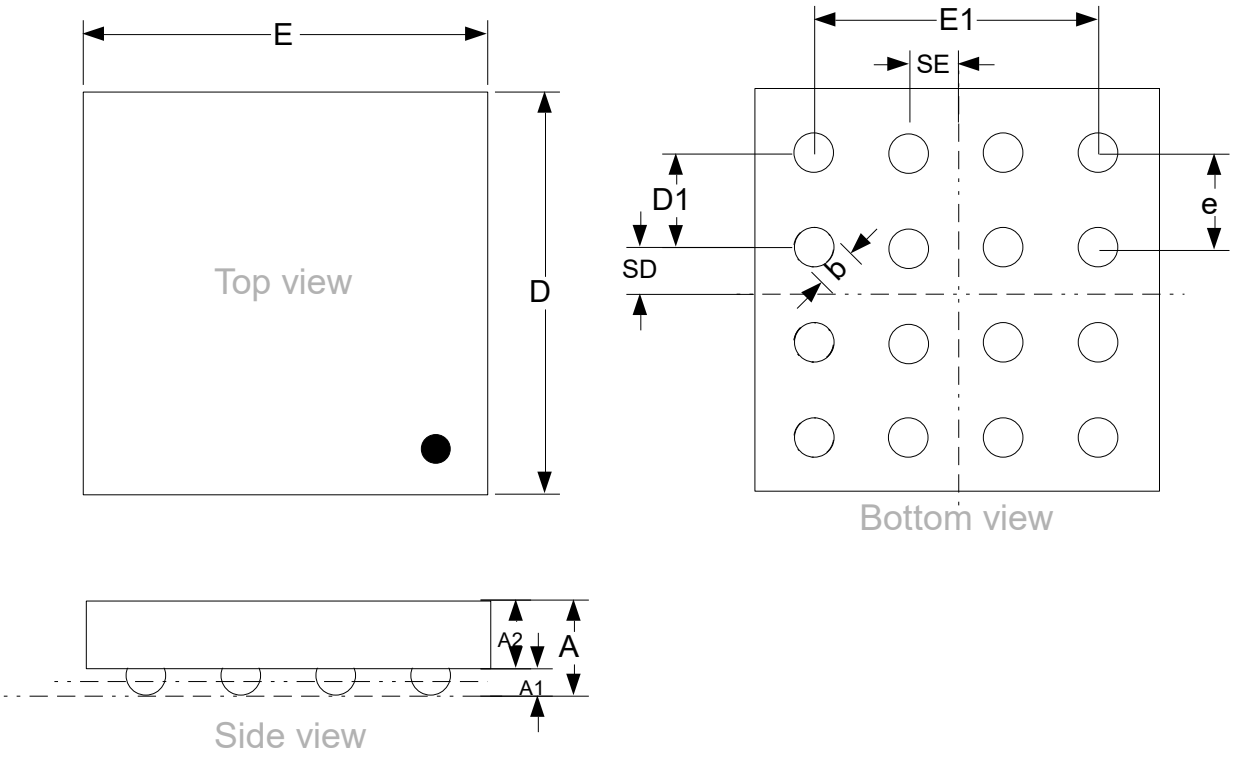
Please check stock availability with your local distributor.



IC NAME	IQS626x	=	IQS626A
CONFIGURATION	zz	=	IC configuration (hexadecimal)
		=	**00** (default) **zz** (Minimum order quantities apply)
PACKAGE TYPE	pp	=	QN: QFN-16 package (special order)
	pp	=	CS: WLCSP-16 package
BULK PACKAGING	b	=	R: Reel (3000pcs/reel) – MOQ = 3000pcs
		=	MOQ = 1 reel (orders shipped as full reels)

7 Package specification

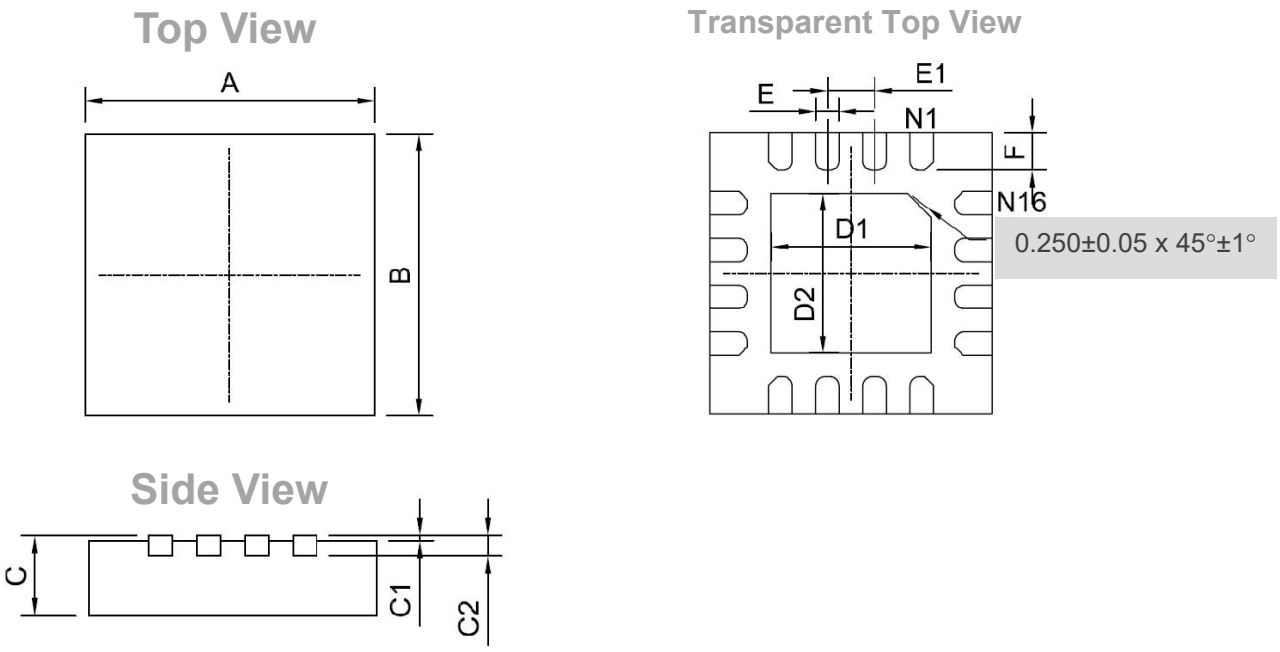
7.1 Package outline description – WLCSP-16



Dimension	[mm]	Dimension	[mm]
A	0.5±0.05	D1	0.4±0.025
A1	0.2±0.015	SD	0.2 BSC
A2	0.3±0.025	E	1.62±0.05
b	0.25±0.025	E1	1.2
D	1.62±0.05	SE	0.2 BSC
		e	0.4 BSC

Figure 7.1: WLCSP(1.62x1.62)–16 Package

7.2 Package outline description – QFN-16



Dimension	[mm]	Dimension	[mm]
A	3.0±0.1	D1	1.7±0.05
B	3.0±0.1	D2	1.7±0.05
C	0.75±0.05	E	0.25±0.05
C1	0.025±0.025	E1	0.5±0.05
C2	0.203±0.05	F	0.4±0.05

Figure 7.2: QFN(3x3)–16 Package

7.3 QFN16 recommended PCB/FPC footprint

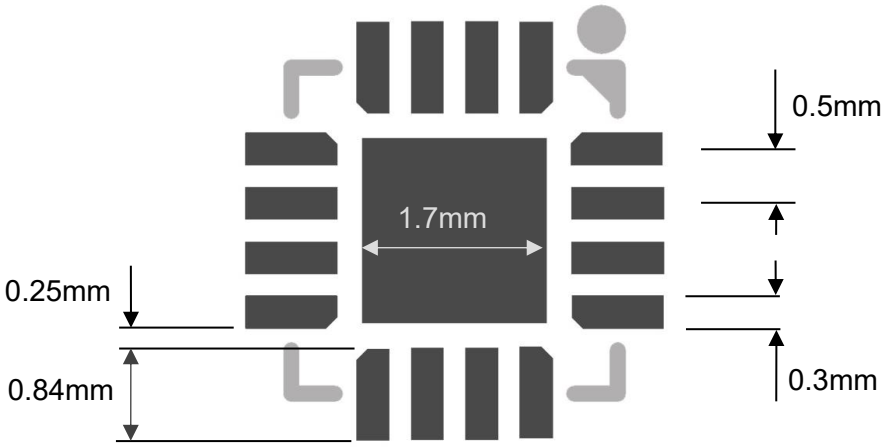


Figure 7.3: IQS626AzzQNR recommended PCB/FPC footprint

7.4 Reflow specification

Table 7-1: WLCSP-16 reflow specifications

Azoteq reflow solder profile	
Device	IQS626A
Package	WLCSP-16 (1.62 x 1.62 x 0.4mm)
Compatibility	Industry standard reflow for Lead-free
Reflow count	Up to 4 times (J-STD-020)

Profile feature	**Value**
Average ramp rate (T_L to T_P)	1-3°C/s
Preheat	
Minimum temperature (T_{SMIN})	130°C
Maximum temperature (T_{SMAX})	200°C
Soak time (T_{SMIN} to T_{SMAX}) t_S	60 - 75s
Ramp-up rate (T_{SMAX} to TL)	1.25°C
Time above liquidus (t_L)	60 - 150s
Liquidous temperature (T_L)	217°C
Peak temperature (T_P)	255 - 260°C
Time within 5°C of actual peak temperature (t_P)	20 - 30s
Ramp down rate	3°C/s max
Time from 25°C of peak temperature	480s max

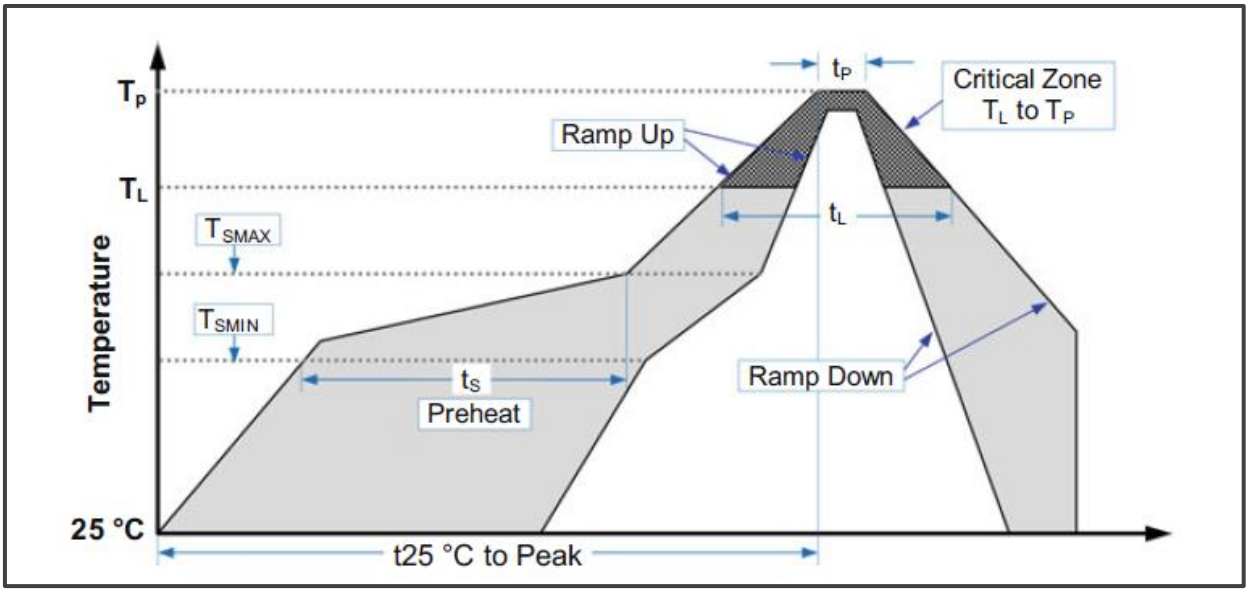


Figure 7.4: WLCSP-16 reflow solder profile

8 Register Map

The IQS626A contains mostly volatile memory which must be configured via the *I2C Interface* after reset in order to achieve the desired device functionality. Herewith follows the complete register map of the IQS626A. For a detailed description of each register, see the *Detailed Register Descriptions* in appendix A.

Some bits in Read-Write registers are marked as Reserved(*val*), such bits must be kept at the value specified by *val*, the key for *val* is as follows:

- 0 –Write to 0
- 1 – Write to 1
- X – Don't Care
- Z – Do not change

8.1 System Information Registers

Table 8-1: System Information Registers

Full Address	Group Name	Item Name (offset 0: bit 7– bit 0)								Item Name (offset 1: bit 7– bit 0)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x00	Version Info	Product Number								Software Version								Read-Only
		0x51 – IQS626A								0x01 – Pre-production firmware 0x02 – Production firmware								
0x01		Hardware Number								Reserved								Read-Only
		Reserved								Not Accessible Any attempt to read or write this byte will access the following byte.								
0x02	Global Flags	System Flags								Global Event Flags								Read-Only
		Show Reset	Reserved		ATI in progress	EVENT	ULP updating all active channels	Power mode (see reg 0x80 bits 5:4)		POWER MODE CHANGE	SYSTEM	REFERENCE CHANNEL	RESERVED	GESTURE	DEEP TOUCH	TOUCH	PROX	
0x03	Gesture Event Flags	Gesture Event Flags (Trackpad)								Reserved								Read-Only
				HOLD	TAP	NEG_Y_FLICK	POS_Y_FLICK	NEG_X_FLICK	_X_FLICK	Not Accessible Any attempt to read or write this byte will access the following byte.								
0x04	Channel States	Channels Proximity State								Channels Proximity Direction								Read-Only
			Generic CH2	Generic CH1	Generic CH0				ULP CH		Generic CH2	Generic CH1	Generic CH0				ULP CH	
0x05		Channels Touch State								Channels Deep Touch State								Read-Only
		Hall CH	Generic CH2	Generic CH1	Generic CH0			TP	ULP CH		Generic CH2	Generic CH1	Generic CH0					
0x06		Reference channels actively used								Reserved								Read-Only
			Generic CH2	Generic CH1	Generic CH0					Not Accessible Any attempt to read or write this byte will access the following byte.								
0x07		Channel compensation minimum flag								Channel compensation maximum flag								Read-Only
		Hall CH	Generic CH2	Generic CH1	Generic CH0			TP	ULP CH	Hall CH	Generic CH2	Generic CH1	Generic CH0			TP	ULP CH	
0x08	Trackpad Coordinates	X Coordinate								Y Coordinate								Read-Only
		0 – 128 (2x3 trackpad); 0 – 255 (3x3 trackpad)								0 – 255								
0x09	Counts & LTA	FILTERED COUNTS ULTRA LOW POWER CHANNEL																Read-Only
0x0A		LONG TERM AVERAGE ULTRA LOW POWER CHANNEL																Read-Only
0x0B		FILTERED COUNTS TRACKPAD CHANNEL 0																Read-Only
0x0C		LONG TERM AVERAGE TRACKPAD CHANNEL 0																Read-Only
0x0D		FILTERED COUNTS TRACKPAD CHANNEL 1																Read-Only
0x0E		LONG TERM AVERAGE TRACKPAD CHANNEL 1																Read-Only
0x0F		FILTERED COUNTS TRACKPAD CHANNEL 2																Read-Only
0x10		LONG TERM AVERAGE TRACKPAD CHANNEL 2																Read-Only
0x11		FILTERED COUNTS TRACKPAD CHANNEL 3																Read-Only
0x12		LONG TERM AVERAGE TRACKPAD CHANNEL 3																Read-Only
0x13		FILTERED COUNTS TRACKPAD CHANNEL 4																Read-Only
0x14		LONG TERM AVERAGE TRACKPAD CHANNEL 4																Read-Only
0x15		FILTERED COUNTS TRACKPAD CHANNEL 5																Read-Only
0x16		LONG TERM AVERAGE TRACKPAD CHANNEL 5																Read-Only

Full Address	Group Name	Item Name (offset 0: bit 7– bit 0)								Item Name (offset 1: bit 7– bit 0)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x17		FILTERED COUNTS TRACKPAD CHANNEL 6																Read-Only
0x18		LONG TERM AVERAGE TRACKPAD CHANNEL 6																Read-Only
0x19		FILTERED COUNTS TRACKPAD CHANNEL 7																Read-Only
0x1A		LONG TERM AVERAGE TRACKPAD CHANNEL 7																Read-Only
0x1B		FILTERED COUNTS TRACKPAD CHANNEL 8																Read-Only
0x1C		LONG TERM AVERAGE TRACKPAD CHANNEL 8																Read-Only
0x1D		FILTERED COUNTS GENERIC CHANNEL 0																Read-Only
0x1E		LONG TERM AVERAGE GENERIC CHANNEL 0																Read-Only
0x1F		FILTERED COUNTS GENERIC CHANNEL 1																Read-Only
0x20		LONG TERM AVERAGE GENERIC CHANNEL 1																Read-Only
0x21		FILTERED COUNTS GENERIC CHANNEL 2																Read-Only
0x22		LONG TERM AVERAGE GENERIC CHANNEL 2																Read-Only
0x23	Hall-Effect Channel Outputs	HALL OUTPUT																Read-Only
0x24		HALL COMMON																Read-Only
0x25		FILTERED COUNTS HALL PLATE 0																Read-Only
0x26		FILTERED COUNTS HALL PLATE 1																Read-Only
0x27	Reference Channel Deltas	REFERENCE CHANNEL DELTA FOR ULP CHANNEL																Read-Only
0x28		REFERENCE CHANNEL DELTA FOR TRACKPAD CHANNELS																Read-Only
0x29		REFERENCE CHANNEL DELTA FOR GENERAL CHANNEL 0																Read-Only
0x2A		REFERENCE CHANNEL DELTA FOR GENERAL CHANNEL 1																Read-Only
0x2B		REFERENCE CHANNEL DELTA FOR GENERAL CHANNEL 2																Read-Only

8.2 General Settings Registers

Table 8-2: General Settings Registers

Full Address	Group Name	Item Name (offset 0: bit 7– bit 0)								Item Name (offset 1: bit 7– bit 0)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x80	Power Mode and System Settings	Power Mode Settings								I²C settings								Read-Write
		Main oscillator change '0' – 16MHz, '1' – 4MHz	Enable CH0 ultra low power (ULP) mode	Auto Power Mode Switching '0' enable '1' disable	Power mode selection (when auto mode switching is disabled) '00' – NP '01' – LP '10' – ULP '11' – Halt mode		NP Segment Update Rate in ULP mode (manage update rate of all channels during ULP mode) '000' – 8, '001' – 13, '010' – 28, '011' – 54, '100' – 89, '101' – 135, '110' – 190, '111' - 256			Reserved (0)	Advanced[1]	Event mode '0' Disable, '1' Enable	Advanced[2]	Advanced[3]	**CMD:** REDO-ATI (Define channels to ATI in reg 0x88 offset 1)	**CMD:** SOFT-RESET	**CMD:** ACK-RESET (Clears "Show reset" – reg 0x02 offset 0 bit 7)	
0x81		Global ProxFusion Settings								Global Event Mask								Read-Write
		Disable ATI Band Check	Trackpad LTA update rate in ULP mode Bits 2:0 = '000' – 2 '001' – 4 '010' – 8 '011' – 16 '100' – 32 '101' – 64 '110' – 128 '111' – 255			ATI_LP (only ATI in LP mode – a more stable time to allow ATI)	GPIO3 touch output channel selection: Bits 2:0 '000' – None '001' – ULP CH0 '010' – TP '011' – TP '100' – Generic CH0 '101' – Generic CH1 '110' – Generic CH2 '111' – Hall CH			Power Mode Change	System	Reference Channel	Reserved	Gesture	Deep-Touch	Touch	Proximity	
0x82		Active channels								Channel Reseed Enable (Enable "LTA Halt time-out" according to reg 0x85 offset 1)								Read-Write
		Hall CH	Generic CH2	Generic CH1	Generic CH0	Reserved (X)	3x3 TP	2x2 TP	ULP CH0	Hall CH	Generic CH2	Generic CH1	Generic CH0		3x3 TP	3x2 TP	ULP CH0	

[1] Advanced setting: Comms during ATI – enable streaming communication during ATI procedure

[2] Advanced setting: Comms in NP – '0' normal event mode, '1' event mode in LP, streaming in NP mode

[3] Advanced settings: Exit I²C window

Full Address	Group Name	Item Name (offset 0: bit 7– bit 0)								Item Name (offset 1: bit 7– bit 0)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x83	Report Rates and Timings	Normal Power Report Rate								Low Power Report Rate								Read-Write
		0 - 255ms								0 - 255ms								
0x84		Ultra-Low Power Report Rate (CH0 only – set "NP Segment Update Rate" for periodic update of other channels)								Power Mode Timer								Read-Write
		(x16) 0 – 4080ms								(x512) 0 – 130 560ms								
0x85		I^2C Window Timeout								LTA Halt Timeout (Proximity / Touch timeout) 0xFF = never timeout								Read-Write
		(x0.5) 0 – 127.5ms Default: 10ms								(x512) 0 – 130 560ms								
0x86	Global Settings	Reference Channel & Other General Settings								Gesture Threshold								Read-Write
		Reference Channel Reseed Level '00' – No Event '01' – In Prox '10' – In Touch '11' – In Deep Touch		Extend Threshold	Enable Reference Channel Tracking UI	Swipe / Flick	Advanced[1]	Trackpad coordinate filter strength '00' 0 (Raw) '01' 1 '10' 2 '11' 3 (Slow)		x1 coordinate								
0x87		Gesture TAP Timeout								Gesture Swipe / Flick Timeout								Read-Write
		(x16) 0 - 4080ms								(x16) 0 - 4080ms								
0x88		**CMD:** Reseed enable **OR** ATI channel selection if "Redo ATI" bit is set Default: "0000 0000" *By default, no channels will ATI when the "Redo ATI" bit is set. Required channels must be selected here.								Reserved								Read-Write
		Hall CH	Generic CH2	Generic CH1	Generic CH0		3x3 TP	3x2 TP	ULP CH	Reserved (X)								
0x89	ULP Channel Settings	ULP Channel Prox Threshold								ULP Channel Touch Threshold								Read-Write
		0 – 255 Counts								x/256 of LTA value								
0x8A		ULP Channel Hysteresis								ULP Channel Counts and LTA Filter Settings								Read-Write
		Reserved (X)			Enable Projected	ULP Touch Hysteresis				Counts Filter Strength_NP		Counts Filter Strength_LP		LTA Filter Strength_NP		LTA filter Strength_LP		
0x8B		ULP Channel ProxSense Settings 0								ULP Channel ProxSense Settings 1								Read-Write
		CS Capacitor Size '0' – 15pF '1' – 60pF	Reserved (0)	Inactive CRx State '0' – Float '1' - Ground	Linearize Counts	Two Sided Detection	Disable count filter '0' = filter '1' = raw	ATI Mode '11' Full ATI '10' Partial '01' Semi-Partial '00' ATI disabled		Increase Charge Cycle Time		Projected mode bias current '00' – 2.5uA '01' – 5uA '10' – 10uA '11' – 20uA		Increase Charge Cycle Time Enable	Sensing frequency selection(16M/4M) '00' 4MHz/1MHz '01' 2MHz/500kHz '10' 1MHz/250kHz '11' 500kHz/ 125kHz		ATI Band '0' = 1/8 '1' = 1/16 counts around the target count	
0x8C		Auto Tuning Implementation (ATI) Base and Target								Reserved								Read-Write
		ATI Base '00' – 75 counts '01' – 100 counts '10' – 150 counts '11' – 200 counts		ATI Target (x32)						Not Accessible Any attempt to read or write this byte will access the following byte.								
0x8D		Channel Multipliers – normal use is read only								Channel Compensation (ATI) – normal use is read only								Read-Write
		Compensation (MSB: bits 9,8)		Coarse Multiplier (ATI)		Fine Multiplier (ATI)				Compensation (LSB: bits 7 – 0)								
0x8E		Channel CRX sense pin selection								Channel TRX transmit pin selection								Read-Write
		CRX7 (bit 7) → CRX0 (bit 0)								TRX7 (bit 7) → TRX0 (bit 0)								
0x8F	Global Trackpad Settings	Trackpad raw counts filter and Hysteresis								Trackpad Auto Tuning Implementation (ATI) Target								Read-Write
		AC filter beta in NP		AC filter beta in LP		Hysteresis amount						ATI Target (x32)						
0x90		Trackpad ProxSense Settings 0								Trackpad ProxSense Settings 1								Read-Write
		CS Capacitor Size '0' – 15pF '1' – 60pF	Reserved(0)	Inactive CRx State '0' – Float '1' - Ground	Linearize Counts	Two Sided Detection	Disable count filter '0' = filter '1' = raw	ATI_mode '11' Full ATI '10' Partial '01' Semi-Partial '00' ATI disabled		Increase Charge Cycle Time		Projected mode bias current '00' – 2.5uA '01' – 5uA '10' – 10uA '11' – 20uA		Increase Charge Cycle Time Enable	Sensing frequency selection(16M/4M) '00' 4MHz/1MHz '01' 2MHz/500kHz '10' 1MHz/250kHz '11' 500kHz/ 125kHz		ATI Band '0' = 1/8 '1' = 1/16 counts around the target count	
0xF10A	I^2C Control Settings	I^2C Control Settings								Reserved								Read-Write
		I^2C End Window	I^2C Disable Stop Condition Handling	I^2C Disable Read Only	I^2C Sleep During Ready Window	Internal use. Retain data when writing	Internal use. Retain data when writing	Internal use. Retain data when writing	Internal use. Retain data when writing	Not Accessible								

[1] Advanced Setting: 8 Count Reseed Offset – After ATI procedure or reseed event, the LTA counts are forced 8 counts higher (self-capacitance) / lower (mutual capacitance) than the actual measured signal counts.

8.3 Trackpad Channel Settings Registers

Table 8-3: Trackpad Channel Settings Registers

(Detailed Description)

Full address per trackpad channel number									Item name (offset 0: bit 7– bit 0)			Item name (offset 1: bit 7– bit 0)	Data Access
0	1	2	3	4	5	6	7	8	Bit 7 ... Bit 0			Bit 7 ... Bit 0	
0x91	0x93	0x95	0x97	0x99	0x9B	0x9D	0x9F	0xA1	Channel Touch Threshold			Auto Tuning Implementation (ATI) Base and Target	Read-Write
									(x1) 0 - 255 counts			(= x + 45) 45 – 300 counts	
0x92	0x94	0x96	0x98	0x9A	0x9C	0x9E	0xA0	0xA2	Channel Multipliers - normal use is read only			Channel Compensation (ATI) – normal use is read only	Read-Write
									Compen-sation (LSB: bits 9,8)	Coarse Multiplier (ATI)	Fine Multiplier (ATI)	Compensation (LSB: bits 7 – 0)	

8.4 Generic Channel Settings Registers

Table 8-4: Generic Channel Settings Registers

(Detailed Description)

Full address per generic channel number			Item name (offset 0: bit 7– bit 0)							Item name (offset 1: bit 7– bit 0)							Data Access
0	1	2	Bit 7 ... Bit 0							Bit 7 ... Bit 0							
0xA3	0xAC	0xB5	Channel Proximity Threshold							Channel Touch Threshold							Read-Write
			(x1) 0 – 255 counts							x/256 of LTA value							
0xA4	0xAD	0xB6	Channel Deep Touch Threshold							Reserved							Read-Write
			x/256 of LTA value							Not Accessible Any attempt to read or write this byte will access the following byte.							
0xA5	0xAE	0xB7	Channel Hysteresis (Proximity has a fixed 4 sample debounce)							Auto Tuning Implementation (ATI) Base and Target							Read-Write
			Deep Touch Hysteresis			Touch Hysteresis				ATI Base '00' – 75 counts '01' – 100 counts '10' – 150 counts '11' – 200 counts	ATI Target (x32)						
0xA6	0xAF	0xB8	Channel Multipliers – normal use is read only							Channel Compensation (ATI) – normal use is read only							Read-Write
			Compensation (MSB: bits 9,8)	Coarse Multiplier (ATI)		Fine Multiplier (ATI)				Compensation (LSB: bits 7 – 0)							
0xA7	0xB0	0xB9	Generic Channel ProxFusion Settings 0							Generic Channel ProxFusion Settings 1							Read-Write
			CS Capacitor Size '0' – 15pF '1' – 60pF	Reserved (0)	Inactive CRx State '0' – Float '1' - Ground	Linearize Counts	Two sided Detection	Disable AC Filter	ATI Mode '11' Full ATI '10' Partial '01' Semi-Partial '00' ATI disabled	Increase Charge Cycle Time [3:2]	Projected mode bias current '00' – 2.5uA '01' – 5uA '10' – 10uA '11' – 20uA	Increase Charge Cycle Time Enable	Sensing frequency selection (16M/4M) '00' 4MHz/1MHz '01' 2MHz/500kHz '10' 1MHz/250kHz '11' 500kHz/ 125kHz	ATI Band '0' = 1/8 '1' = 1/16 counts around the target count				
0xA8	0xB1	0xBA	Generic Channel ProxFusion Settings 2							Generic Channel ProxFusion Settings 3							Read-Write
			CAL Cap size '00' 0.5pF '01' 1.0pF '10' 1.5pF '11' 2.0pF		Enable CAL Cap	Reserved Set '0'	Sensor mode '0000' – Surface '0001' – Projected '1000' – Self inductance '1001' – Mutual inductance '1100' – External (PIR) '1110' – HALL '1111' – Temperature			Reserved (Z)	Reserved (0)	Tx Frequency '00' – FOSC '01' – FOSC/2 '10' – FOSC/4 '11' – FOSC/8	Reserved (0)		Inverse Logic Direction			
0xA9	0xB2	0xBB	Generic Channel ProxFusion Settings 4							Generic Channel Counts and LTA Filter Settings							Read-Write
			Reserved (Z)	Inactive CRx to VReg (If Inactive CRx State = 0)	Increase Charge Cycle Time [1:0]		Reserved (0)	Reserved (0)	Disable Compensation	Static Fine Multipliers	Counts Filter Strength_NP	Counts Filter Strength_LP	LTA Filter Strength_NP	LTA filter Strength_LP			
0xAA	0xB3	0xBC	Channel Rx Selection							Channel Tx Selection							Read-Write
			CRX7 (bit 7) → CRX0 (bit 0)							CRX7 (bit 7) → CRX0 (bit 0)							
0xAB	0xB4	0xBD	Reference Channel Association							Reference Channel Impact Weight (if this channel is associated to reference channel – 0 = no impact, 255 = 200% impact)							Read-Write
			Hall CH	Generic CH2	Generic CH1	Generic CH0			TP	ULP CH0	x/255 * 200 % (0% – 200%)						

8.5 Hall-Effect Channel Settings Registers

Table 8-5 Hall-Effect Channel Settings Registers

(Detailed Description)

Hall channel	Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
	Bit 7							Bit 0	Bit 7							Bit 0	
0xBE	Hall settings								Hall touch threshold								Read-Write
	CS Capacitor Size '0' – 15pF '1' – 60pF	Reserved (0)	Inactive CRx State '0' – Float '1' - Ground	Linearize Counts	Two Sided Detection	Disable AC filter	ATI Mode '11' Full ATI '10' Partial '01' Semi-Partial '00' ATI disabled		x/256 of LTA value								
0xBF	Hall Channel Hysteresis								Auto Tuning Implementation (ATI) Base and Target								Read-Write
	Reserved (0)		Reserved (Z)		Hall Touch Hysteresis				ATI Base '00' – 75 counts '01' – 100 counts '10' – 150 counts '11' – 200 counts		ATI Target (x32)						
0xC0	Channel Multipliers – normal use is read only								Channel Compensation (ATI) – normal use is read only								Read-Write
	Compensation (MSB: bits 9,8)		Coarse Multiplier (ATI)		Fine Multiplier (ATI)				Compensation (LSB: bits 7 – 0)								

9 One Time Programmable Bytes

The IQS626A contains 6 non-volatile One-Time Programmable (OTP) bytes which can be programmed in order to configure various application settings. The majority of the settings configured by the OTP bytes are related to the *Reset User Interfaces* (RUIs).

The OTP bytes can be programmed with a CT210A and the USBProg2 PC software, please contact Azoteq or an affiliated Azoteq sales representative for the USBProg2 software and related instructions.

Herewith follows a summary of the IQS626A OTP bytes, for a detailed description of each byte see the *Detailed One-Time Programmable Byte Descriptions* in appendix B.

Table 9-1: One-Time Programmable Bytes Summary

Byte No.	One-Time Programmable Byte Bits							
	7	6	5	4	3	2	1	0
Byte 0	OSCFREQ	SCAPCRX	I2CADDR	RDYTYPE	GPIOTYPE	RESERVED		
Byte 1	RESERVED							
Byte 2	RESERVED							
Byte 3	HALLATI[1:0]		RESERVED					
Byte 4	HALLTHR[5:0]						RESERVED	
Byte 5	RESERVED				RUIMODE[1:0]		SCAPTHRE[1:0]	

10 I²C Interface

10.1 I²C module specification

The device supports a standard two wire I²C interface with the addition of an RDY (ready interrupt) line. The communications interface of the IQS626A supports the following:

- *Fast-mode (Fm)* standard I²C up to 400kHz.
- Streaming data as well as event mode.
- The master may address the device at any time. If the IQS626A is not in a communication window, the device will return an ACK after which clock stretching may be induced until a communication window is entered. Additional communication checks are included in the main loop in order to reduce the average clock stretching time to a maximum of 1ms.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS626A implements 8bit addressing with two bytes at each address. Two consecutive reads/writes are required in this memory map structure. The two bytes at each address will be referred to as “offset 0” (first byte) and “offset 1” (second byte).

10.2 I²C address

The IQS626A with custom order code offers 2 address options:

- Default: 0x44
    - 0x44: (default) Output option defined on GPIO4
    - 0x44: (special order) GPIO4 defined as address input. Float GPIO4 (internal pull-up defined)
    - 0x46: (special order) GPIO4 defined as address input. GND GPIO4
- Alternate: 0x45 / 0x47
    - 0x45: (special order) Output option defined on GPIO4
    - 0x45: (special order) GPIO4 defined as address input. Float GPIO4 (internal pull-up defined)
    - 0x47: (special order) GPIO4 defined as address input. GND GPIO4

The order code: IQS626A00CSR has a fixed I²C address of 0x44 with no alternate option.

10.3 I³C

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

10.4 I²C Read

To read from the device a *current address read* can be performed. This assumes that the address-command is already setup as desired.

Current Address Read

Start	Control byte		Data n		Data n+1		Stop
S	Addr + READ	ACK		ACK		NACK	S

Figure 10.1: Current Address Read

If the address-command must first be specified, then a *random read* must be performed. In this case, a WRITE is initially performed to setup the address-command, and then a repeated start is used to initiate the READ section.

Random Read

Start	Control byte		Address-command		Start	Control byte		Data n		Stop
S	Addr + WRITE	ACK		ACK	S	Addr + READ	ACK		NACK	S

Figure 10.2: Random Read

10.5 I2C Write

To write settings to the device a *Data Write* is performed. Here the Address-Command is always required, followed by the relevant data bytes to write to the device.

Data Write

Start	Control byte		Address-Command		Data n		Data n+1		Stop
S	Addr + WRITE	ACK		ACK		ACK		ACK	S

Figure 10.3: I2C Data Write

10.6 Stop-bit disable option

For specific I²C master limitations, the IQS626A offers the following:

- I²C Control Settings register (0xF10A) for stop-bit disable functionality,
- The “stop bit disable” bit for ignoring the I²C stop condition from the master. This “ignore” will keep the communication window open.
- The “I²C End Window” condition bit making it possible to set the “stop-bit enable” only once.
  - The command will cause the communication window to close only at the next stop-bit sent from the master.
  - The benefit from using this command is that the “stop-bit disable” does not need to be enabled again at the next communication window.
  - All settings written before and after setting this bit will be applied as long as it is written before any stop bit is sent from the master.
- The RDY timeout period register (0x85, offset 0) can be used for an automatic time-out. The timer will start from the last byte on the bus. In this case no intervention from the master is required to end the communications window.

Customers using an MCU with a binary serial-encoder peripheral which is not fully I²C compatible (but provide some crude serial communication functions) can use this option to configure the

IQS626A so that any auto generated stop command from the serial peripheral can be ignored by the IQS626A I²C hardware. This will restrict the IQS626A from immediately exiting a communication window during event mode (reduced communication only for events) until all required communication has been completed and a stop command can correctly be transmitted. Please refer to the figures below for serial data transmission examples.

Please note:

1. Stop-bit disable and I²C end window condition clearing must be performed at the beginning and of a communication window. The first I²C register to be written to ensure no unwanted communication window termination.
2. Leaving the Stop-bit disabled will result in successful reading and writing of registers but will not execute any commands written over I²C in a communication window being terminated after a RDY timeout and with no IQS recognised stop command.
3. The default RDY timeout period for IQS626A is purposefully long (10.24ms) for slow responding MCU hardware architectures. Please set this register according to your requirements/preference.
4. Use the I²C end window condition (0xF10A, bit7) to purposefully terminate at the next stop-bit condition generated by the master.
5. For any following I²C communication windows, repeat the sequence of first clearing the I²C end window condition (0xF10A, bit7) to prevent exit of the communication window before reading data from applicable event and channel registers.

Stop-bit disable and clear I²C end window condition (bit7)

Communication window open	Start	Control byte		Address-Command		Address-Command		Disable stop-bit		Ignored stop	Continue with reads / writes
RDY = ↓LOW	**S**	**Addr + WRITE**	**ACK**	**0xF1**	**ACK**	**0x0A**	**ACK**	**0x41**	**ACK**	**S**	**…**

Figure 10.4: I2C Stop-bit disable and clear I2C end window condition

Read data of register 0xF10A

Reads / Writes finished	Start	Control byte		Address-Command		Address-Command		Start	Control byte	Read data		Ignored stop	Communication window still open
…	**S**	**Addr + WRITE**	**ACK**	**0xF1**	**ACK**	**0x0A**	**ACK**	**S**	**Addr + READ**	**0x??**	**NACK**	**S**	**RDY = _LOW**

Figure 10.5: Read and retain data of register 0xF10A

Modify-write register 0xF10A

Continue	Start	Control byte		Address-Command		Address-Command		Retain 0xF10A & set end I²C window (bit7)		Stop	Communication window closed
…	S	Addr + WRITE	ACK	0xF1	ACK	0x0A	ACK	0x?? | 0x80	ACK	S	RDY = ↑HIGH

Figure 10.6: Modify-write register 0xF10A to end the communication window

10.7 Watchdog Time-out

The IQS626A is designed to do a watchdog reset if:

- I²C stuck during transmission (number of clock pulses is not a multiple of 9)
- IQS626A was addressed but no further communication initiated, i.e. no I²C events happen (no data, no stop or no start)
- I²C bus remain low shortly after POR
- I²C reset command is called.
- Program flow does not execute as expected (or goes wrong due to something like damaged ROM memory)

The IQS626A program flow waits and does NOT reset in the following cases:

- If VREG does not stabilize
- If the IC is in test mode (for IC testing or IC OTP programming)

10.8 Clock Stretching and Forcing Communications

Communications with the IQS626A can be forced by addressing the IQS626A and waiting for an acknowledgement (ACK) to be returned after clock stretching the host. The following situations will result in forced communications:

10.8.1 IQS626A Clock Stretching During a Communication Window (RDY Low)

When the RDY signal is already low, to report periodic sampled data (streaming mode) or to indicate an event occurrence (event mode), the IQS626A will stretch the clock line (SCL) after the master has written the address command byte to the device. The clock stretch can be attributed to the IQS626A loading data from the buffer. Clock stretching will be induced each time configuring a new address command byte occurs. The timing diagram for this occurrence is shown below in *Figure 10.7*.

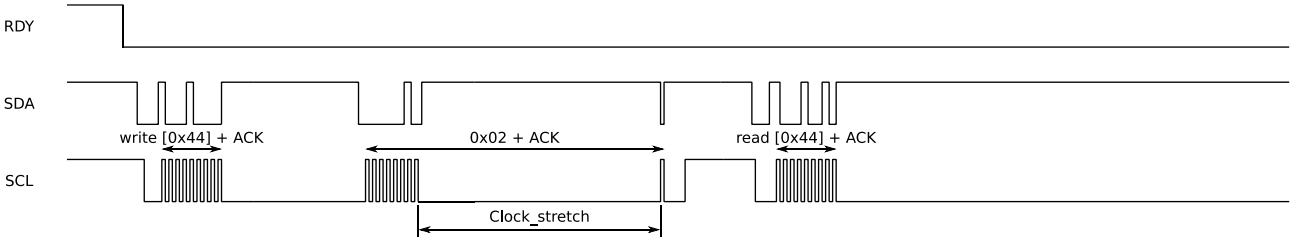


Figure 10.7: Clock Stretching During a Communication Window (RDY Low)

Table 10-1: Clock Stretching Periods During Active Communications (RDY low)

	Minimum	Maximum	Unit
Clock_stretch	60	128	µs

10.8.2 Clock Stretching When MCU Polls IQS626A Without Waiting for RDY Event

The IQS626A will stretch the clock if the master addresses the device outside of a communication window (RDY high). Interrupting the device during ongoing sensor conversions, data processing or inactive (sleep) states will result in slightly longer clock stretching while the IQS626A terminates the task at hand and prepares the communication peripheral to respond. The timing diagram for the event is shown in *Figure 10.8* below.

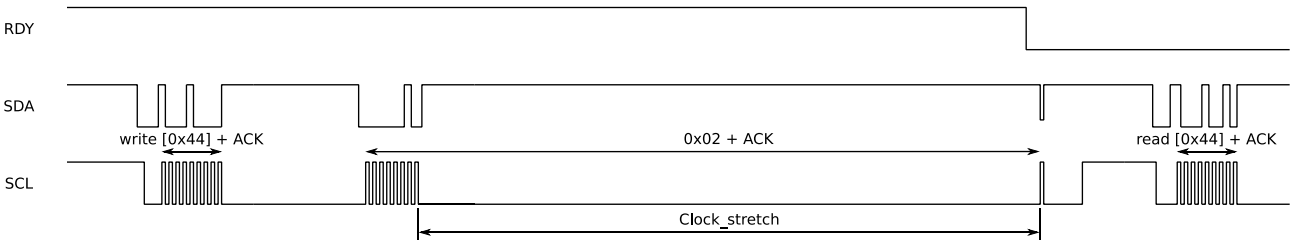


Figure 10.8: Clock Stretching During Inactive Communication (RDY high) Before Opening a Communication Window

Table 10-2: Clock Stretching Periods During Inactive Communications (RDY high)

	Typical	Maximum	Unit
Clock_stretch	250	300	µs

11 Sensor Channels

11.1 Ultra-Low Power Channel

The Ultra-Low Power (ULP) channel is strictly a capacitive channel. It is the only channel for which sensing conversions take place during every report cycle when the device is in ULP mode. Therefore, its primary purpose is to wake the IQS626A from ULP mode, this allows low power operation while also ensuring overall sensor responsiveness.

11.1.1 Channel Outputs

For every sensing conversion performed on the ULP channel, the state information related to the ULP channel is calculated and updated in the register map. This information can be regarded as the channel outputs and it can be read from the register map vias the I2C interface. The ULP channel related outputs are as follows:

- **ULP Channel Filtered Counts**

  This is a 16 bit integer which can be read as 2 bytes from the Filtered Counts Ultra-Low Power Channel register (0x09, offset 0 and 1).

- **ULP Channel Long Term Average**

  This is a 16 bit integer which can be read as 2 bytes from the Long Term Average Ultra-Low Power Channel register (0x0A, offset 0 and 1).

- **ULP Channel Prox State Flag**

  The ULP Channel Prox State flag is represented by the ULP CH0 bit (bit 0) in the Channel Proximity State register (0x04, offset 0). It is set if the Prox Threshold of the channel is currently breeched.

- **ULP Channel Prox Direction Flag**

  The ULP Channel Prox Direction flag is represented by the ULP CH0 bit (bit 0) in the Channel Proximity Direction register (0x04, offset 1). The bit is set if the Channel Prox State flag is set and the channel counts value is larger than the channel LTA value.

- **ULP Channel Touch State Flag**

  The ULP Channel Touch State flag is represented by the ULP CH0 bit (bit 0) in the Channel Touch State register (0x05, offset 0). The bit is set if the Touch Threshold of the channel is currently breeched.

11.1.2 Sensor Modes

Only self-capacitive and mutual-capacitive sensor modes are available for the ULP channel.

11.1.3 CRX Selection

All CRX pins are available to the ULP channel to function as either Receiver (RX) pins or Transmitter (TX) pins.

11.2 Mutual-Capacitive Trackpad

The IQS626A offers 3x2 and 3x3 mutual-capacitive trackpad options. The trackpad itself is a grouping of individual trackpad channels, it consists of 6 channels (TP0 through TP5) if the 3x2 Trackpad (3x2TP) option is enabled and 9 channels (TP0 through TP8) if the both the 3x2 Trackpad and the 3x3 Trackpad (3x3TP) options are enabled.

Note: The 3x3TP is merely an extension of the 3x2TP, therefore the 3x2TP must be enabled before the 3x3TP can be enabled.

Each trackpad channel makes use of a TX pin and an RX pin. The TX/RX combinations for each channel are as follows:

- **3x2 Trackpad:**
  - **TP0:** TX0 + RX0
  - **TP1:** TX0 + RX1
  - **TP2:** TX0 + RX2
  - **TP3:** TX1 + RX1
  - **TP4:** TX1 + RX2
  - **TP5:** TX1 + RX0
- **3x3 Trackpad**
  - **TP6:** TX2 + RX0
  - **TP7:** TX2 + RX1
  - **TP8:** TX2 + RX2

Figure 11.1 and *Figure 11.2* illustrate how the TX and RX nets combine to form the trackpad channels.

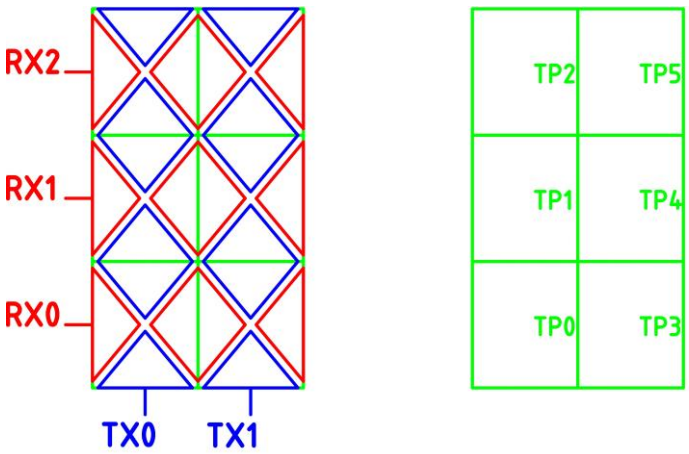


Figure 11.1: 3x2 Trackpad Channel Configuration

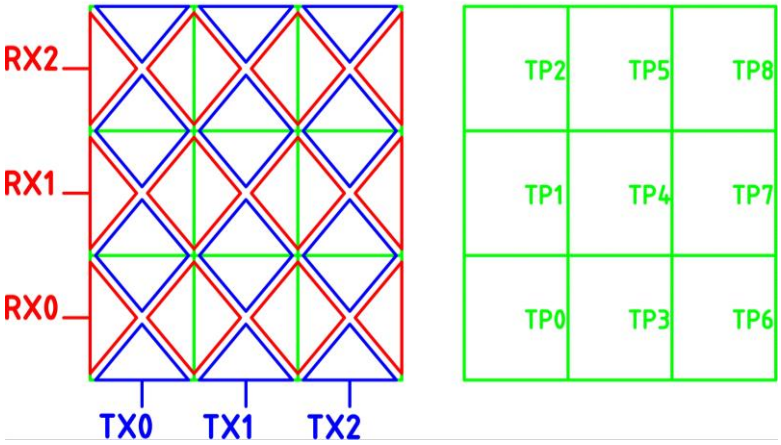


Figure 11.2: 3x3 Trackpad Configuration

11.2.1 Channel Outputs

For every sensing conversion performed on the trackpad, the following state information is updated in the register map for each active trackpad channel.

- **Trackpad Channel Filtered Counts**

  16 bit integer value available at register 0x0B + 2N, where N represents the trackpad channel number.

- **Trackpad Channel Long Term Average**

  16 bit integer values available at register 0x0C + 2N, where N represents the trackpad channel number.

The following information is also updated for the trackpad group as a whole:

- **Trackpad Touch State Flag**

  The Trackpad Channel Touch State flag is represented by the TP bit (bit 1) in the Channel Touch State register (0x05, offset 0). The bit is set if the Touch Threshold on any of the active trackpad channels is currently breeched.

- **Trackpad Gesture Event Flags**

  Gesture event bits are set in the Gesture Event Flags register (0x03, offset 0) if certain gestures are detected on the trackpad, see *Trackpad Gestures* for a description of gesture types. These bits remain set until any amount of bytes are read from register address 0x02. The gesture event bits are as follows:

  - **POS_X_FLICK (Bit 0)**
    Set on detection of a Swipe or Flick gesture in the positive direction of the x-axis.
  - **NEG_X_FLICK (Bit 1)**
    Set on detection of a Swipe or Flick gesture in the negative direction of the x-axis.
  - **POS_Y_FLICK (Bit 2)**
    Set on detection of a Swipe or Flick gesture in the positive direction of the y-axis.
  - **NEG_Y_FLICK (Bit 3)**
    Set on detection of a Swipe or Flick gesture in the negative direction of the y-axis.
  - **TAP (Bit 4)**
    Set on detection of a tap gesture.
  - **HOLD (Bit 5)**

- Set on detection of a hold gesture.

> **Trackpad Coordinates**

X and Y coordinate values are calculated for the trackpad base on the delta values of all active trackpad channels.

- **X Coordinate**
  Read from the X Coordinate register (0x08, offset 0). 0-128 range for 3x2TP and 0-255 range for 3x3TP.
- **Y Coordinate**
  Read from the Y Coordinate register (0x08, offset 1). 0-255 range for both 3x2TP and 3x3TP.

11.2.2 Sensor Modes

The trackpad channels are implemented with the mutual-capacitive sensor mode with no alternate option.

11.2.3 CRX Selection

The trackpad channels have dedicated CRX pin assignments and cannot be changed, these are:

- **3x2 Trackpad:**
  - **TX0:** CRX7
  - **TX1:** CRX5
  - **RX0:** CRX2
  - **RX1:** CRX4
  - **RX2:** CRX6
- **3x3 Trackpad:**
  - **TX2:** CRX3

11.3 Generic Channels

Three generic channels are available on the IQS626A, these are general purpose channels which can be configured to perform a wide variety of additional functions. Some common functions which the generic channels are use for are as follows:

- Capacitive wear detection channel with temperature tracking channel requires 2 channels and 2 CRX pins.
- Inductive force sensing channel, requires 1 channel and 3 CRX pins.
- Additional capacitive buttons, requires 1 channel and 1 CRX pin per button.

11.3.1 Channel Outputs

For every sensing conversion performed on an active generic channel, the following state information is updated in the register map:

> **Generic Channel Filtered Counts**

16 bit integer values available at registers 0x1D, 0x1F and 0x21 for generic channels 0, 1 and 2 respectively.

> **Generic Channel Long Term Average**

16 bit integer values available at registers 0x1E, 0x20 and 0x22 for generic channels 0, 1 and 2 respectively.

> **Generic Channel Prox State Flag**

The Generic Channel x Prox State flags are represented by the Generic CHx bits (bits 4, 5 and 6) in the Channel Proximity State register (0x04, offset 0). The respective bit of each channel is set of the Prox Threshold of the channel is currently breeched.

> **Generic Channel Prox Direction Flag**

The Generic Channel x Prox Direction flags are represented by the Generic CHx bits (bits 4, 5 and 6) in the Channel Proximity Direction register (0x04, offset 1). The respective bit of each channel is set if the Prox State flag of the channel is set and the channel counts value is larger than the channel LTA value.

> **Generic Channel Touch State Flag**

The Generic Channel x Channel Touch State flags are represented by the Generic CHx bits (bits 4, 5 and 6) in the Channel Touch State register (0x05, offset 0). The respective bit of each channel is set if the Touch Threshold of the channel is currently breeched.

> **Generic Channel Deep Touch State Flag**

The Generic Channel x Channel Deep Touch State Flag is represented by the Generic CHx bits (bits 4, 5 and 6) in the Channel Deep Touch State register (0x05, offset 1). The respective bit of each channel is set if the Deep Touch Threshold of the channel is currently breeched.

11.3.2 Sensor Modes

All generic channels can make use of the following sensor modes:

- Self-Capacitive
- Mutual-Capacitive
- Inductive Mode 1
- Inductive Mode 2
- Hall-effect
- Temperature

11.3.3 CRX Selection

All CRX pins are available to the ULP channel to function as either Receiver (RX) pins or Transmitter (TX) pins.

11.4 Hall Channel

The IQS626A provides a specific hall sensing channel which provides a hall state information which is unaffected by the ATI routine. This means that the presence of a magnetic field will always be detectable despite intermittent ATI events.

11.4.1 Channel Outputs

For every sensing conversion performed on the hall channel, the following state information is updated in the register map:

- **Hall Output**

  16 bit integer value available at register 0x23. The Hall Output value is proportional to the strength of the magnetic field which is present, if no magnetic field is present then it will be 0. The sign of the value represents the direction of the magnetic field.

- **Hall Common**

  16 bit integer value available at register 0x24. The hall common value should be very near to the Hall ATI Target and should remain constant at all times. A change in this value indicates saturation within the hall sensing circuitry. Saturation may be resolved by altering the hall channel configuration or reducing the magnetic field strength.

- **Hall Channel Touch State Flag**

  The Hall Channel Touch State flag is represented by the Hall CH bit (bit 7) in the Channel Touch State register (0x05, offset 0). The bit is set if the Hall Output value is higher than the Hall Touch Threshold.

11.4.2 Sensor Modes

Hall channel sensor mode is not selectable and is confined to hall-effect sensing.

11.4.3 CRX Selection

Hall sensing circuitry is internal and thus no CRX pins are required and no CRX selection is available.

12 Special Device Features

12.1 Automatic Tuning Implementation

The Automatic Tuning Implementation (ATI) is a special algorithm which automatically adjusts the Channel Multipliers and the Channel Compensation for each channel in order to obtain their the selected ATI Base and ATI Target counts values. This ensures that channel sensitivity remains more or less the same despite varying environmental conditions, such as temperature, humidity and external load capacitance. The IQS626A allows the user to select between 4 degrees of ATI for each channel by means of the ATI Mode[1:0] bits associated with each channel. The selectable ATI modes are:

- **Full ATI (ATI Mode[1:0] = 0b11)**
  The algorithm automatically selects the Coarse Multiplier, Fine Multiplier and Compensation.
- **Partial ATI (ATI Mode[1:0] = 0b10)**
  The User selects the Coarse Multiplier and the Fine Multiplier. The algorithm automatically selects the Compensation.
- **Semi-Partial ATI (ATI Mode[1:0] = 0b01)**
  The user selects the Coarse Multiplier. The algorithm automatically selects the Fine Multiplier and Compensation.
- **ATI Disabled (ATI Mode[1:0] = 0b00)**
  The user must select the Coarse Multiplier, Fine Multiplier and Compensation.

Recommendations:

- For most applications, the use of “Full ATI” is highly recommended.
- Partial modes are used to ensure uniformity of sensitivity over multiple channels or multiple devices. This should be used with care because it limits the device’s automatic calibration range.
- Disable ATI for unique cases such as debugging or power-on with certain ATI parameters. Preferably these should be “last used” parameters and not fixed for the applications

12.2 Power Modes

12.2.1 Automatic Power Mode Switching

Automatic power mode switching is a time and event-based feature implemented to automatically adjust between the three available power modes. The auto mode switching is enabled by default and can be disabled by clearing the Auto Power Mode Switching bit in the Power Mode Settings (0x80, offset 0) register. Enabling auto power mode switching will allow the IQS626A to switch between power modes normal, low and, if enabled, ultra-low power based on the occurrence of prox or touch events, or the absence thereof, for a fixed period. The sequence and timings of power mode switching is shown in *Figure 12.1* below. The IQS626A will start up in normal power mode and switch to low power and ultimately ultra-low power if no event is recorded on any enabled channels. The inactive period before a power mode switch occurs (from NP to LP or from LP to ULP modes) is defined by the Power Mode Timer (0x84, offset 1) register, in increments of 512ms. If a prox or touch event occurs on a channel while the IQS626A is in low or ultra-low power mode, the IQS626A will switch to normal power mode.

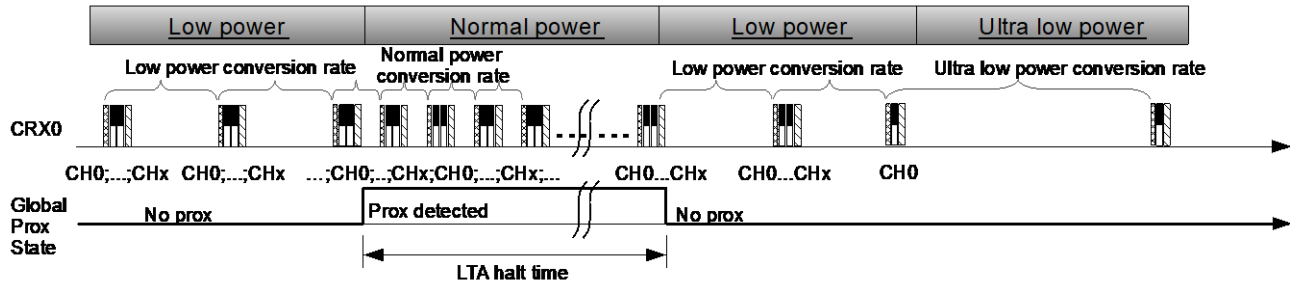


Figure 12.1: Power Mode Switching Timing Diagram

12.2.2 Normal Power (NP) Mode

Normal power mode continuously updates all channels that are enabled. The rate at which updates occur is defined by the Normal Power Mode Report Rate (0x83, offset 0) register. The timing for normal power mode is shown in *Figure 12.2* below.

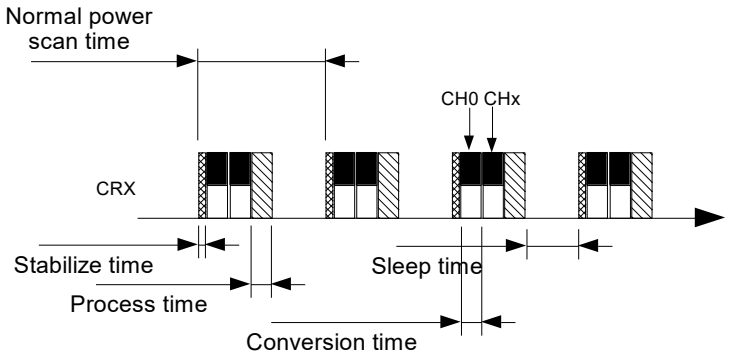


Figure 12.2: Normal Power Mode Conversion Process

12.2.3 Low Power (LP) Mode

The IQS626A will switch from normal power mode to low power mode if no prox or touch events are registered on any enabled channels for the time specified by the Power Mode Timer (0x84, offset 1) register. Low power mode continuously updates all channels that are enabled at a lower sampling rate than normal power. The rate of the updates is defined by the Low Power Mode Report Rate (0x83, offset 1) register. The timing diagram for low power mode is shown in *Figure 12.3* below.

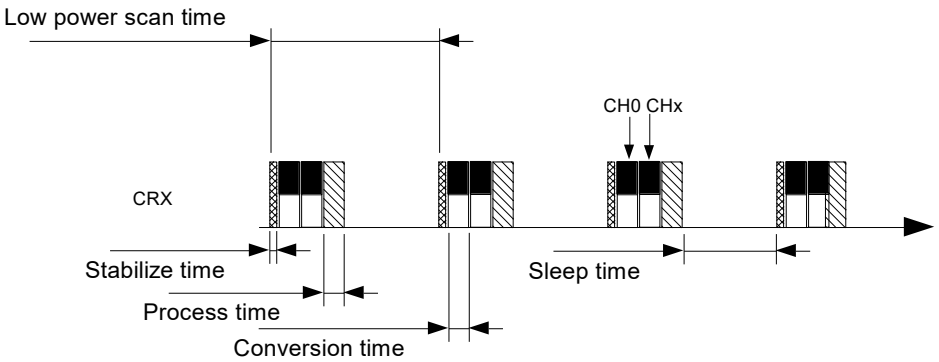


Figure 12.3: Low Power Mode Conversion Process

12.2.4 Ultra-Low Power Mode

The IQS626A will switch from Low Power Mode to Ultra-Low Power (ULP) mode if no prox or touch events are registered on any enabled channels for the time specified by the Power Mode Timer (0x84, offset 1) register. The IQS626A will continuously update Channel 0 at a rate defined by the Ultra-Low Power Mode Report Rate (0x84, offset 0) register. All other enabled channels will be updated every n^{th} report cycle, with n defined by the NP Segment Update Rate[1:0] bits in the Power Mode Settings (0x80, offset 0) register. A diagram of the ultra-low power conversion process (with ULP update rate: n = 4) is shown in *Figure 12.4* below.

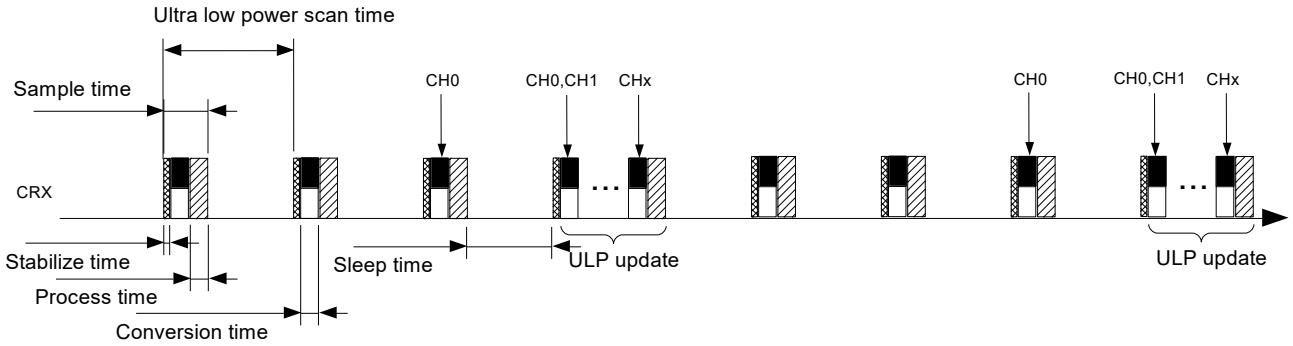


Figure 12.4: Ultra-low Power Mode Conversion Process

12.3 Trackpad Gestures

The IQS626A is able to recognise 4 types of gestures input via the trackpad, these are:

- Swipe or Flick
- Tap
- Hold

When a gesture event is recognised, the Gesture flag (bit 3) will be set in the Global Event Flags register (0x02, offset 1) and the corresponding gesture bit will be set in the Gesture Event Flags register (0x03, offset 0). These bits will remain set until any amount of bytes are read from address 0x02.

For a touch event on the trackpad to be successfully recognised as a gesture, the touch event must adhere to the constraints specified by the Gesture Threshold (0x86, offset 1), Gesture Tap Timeout (0x87, offset 0) and Gesture Swipe/Flick Timeout (0x87, offset 1) registers. A touch event on the trackpad starts whenever the Trackpad Touch State flag changes from a 0 to a 1 (see *Mutual-Capacitive Trackpad*) and ends whenever the Trackpad Touch State flags changes from a 1 to a 0. Below follows a description of each gesture type.

12.3.1 Tap

A tap gesture is recognised when a touch event lasts for a period of time shorter than that specified by the Gesture Tap Timeout register, and neither the X nor the Y coordinates change by an amount of more than half the value contained in the Gesture Threshold register.

If these conditions are met, the TAP bit (bit 4) in the Gesture Event Flags register is set.

12.3.2 Flick

Before a Flick gesture can be recognised, the Swipe/Flick bit (bit 3) in the Reference Channel & General Settings register (0x86, offset 0) must be cleared.

A Flick gesture is recognised when a touch event lasts for a period of time less than that specified by the Gesture Swipe/Flick Timeout register, and the X or the Y coordinates change by an amount larger than or equal to that specified by the Gesture Threshold register.

The touch event must end within the Gesture Swipe/Flick Timeout period for the Flick gesture to be recognised.

If these conditions are met, the POS_X_FLICK (bit 0), NEG_X_FLICK (bit 1), POS_Y_FLICK (bit 2) or NEG_Y_FLICK (bit 3) bit is set in the Gesture Event Flags register, depending on the direction of the movement on the trackpad.

12.3.3 Swipe

Before a Swipe gesture can be recognised, the Swipe/Flick bit (bit 3) in the Reference Channel & General Settings register (0x86, offset 0) must be set.

A Swipe gesture is recognised when the X or Y coordinates change by an amount larger than or equal to that specified by the Gesture Threshold register before the period of time specified by the Gesture Swipe/Flick Timeout register elapses from the start of the touch event.

The touch event does not need to end for the Swipe gesture to be recognised.

If these conditions are met, the POS_X_FLICK (bit 0), NEG_X_FLICK (bit 1), POS_Y_FLICK (bit 2) or NEG_Y_FLICK (bit 3) bit is set in the Gesture Event Flags register, depending on the direction of the movement on the trackpad.

12.3.4 Hold

A hold gesture is recognised whenever a touch event lasts for a period of time more than that specified by both the Gesture Tap Timeout and Gesture Swipe/Flick Timeout registers. The touch event does not need to end for the gesture to be successfully recognised.

If these conditions are met, the HOLD bit (bit 5) in the Gesture Event Flags register is set.

12.4 Reference Channels

Each generic channel of the IQS626A can be assigned to act as a reference channel for any combination of channels (excluding itself) by selecting the respective bits in the Reference Channel Association registers (addresses 0xAB, 0xB4 and 0xBD, offset 0). The channels for which a generic channel acts as a reference channel for are referred to as the associated channels.

When reference channels are assigned, the *Reference Channel Reseed UI* (or Reseed UI) takes immediate effect. *Reference Channel Tracking UI* (or Tracking UI) replaces the Reseed UI when the Enable Reference channel Tracking UI bit (bit 4) in the Global Settings register (Address 0x87, offset 0).

When using reference channels, a reseed level must be selected with the Reference Channel Reseed Level bits (bits [7:6]) in the Reference channel & Other General Settings register (address 0x86, offset 0). The reseed level specifies the maximum state at which the associated channels can be reseeded. For example, if the reseed level is chosen as In Touch, the associated channels can be reseeded when they have no event, when they are in a prox state and when they are in a touch state.

12.4.1 Reference Channel Reseed UI

When the Reseed UI is in effect, a reference channel will trigger a reseed on itself and all of its associated channels if the following reseed conditions are met:

- The delta value on the reference channel breeches the Prox threshold.

- All of the associated channels are within the selected reseed level.

12.4.2 Reference Channel Tracking UI

The Tracking UI implements the Reseed UI and adds LTA adjustment functionality to it. The LTA adjustment works as follows:

- If the reseed conditions, as described in the *Reference Channel Reseed UI*, section are not met then the LTA values of the associated channels are adjusted.
- The LTA values of the associated channels are adjusted by subtracting an adjustment value from it.
- The adjustment value is the delta value of the reference channel multiplied by the Reference Channel Impact Weight (register 0xAB, 0xB4, 0xBD, offset 1).

If the states of the associated channels are altered by the LTA adjustment such that the reseed conditions are met, then a reseed will be performed on the reference channel and all of its associated channels.

13 Reset User Interfaces

A Reset User Interface (RUI) is a mode of operation which is entered into directly after device reset. An RUI has pre-configured settings which are loaded from the non-volatile *Detailed One-Time Programmable* Byt. This allows the IQS626A to enter an operational state and provide outputs according to the selected RUI without requiring any communication from the master. Thus, an RUI is similar a standalone operating mode, except that the I²C communication interface and the ready line remain active, allowing the master to reconfigure the IQS626A at any time.

The IQS626A has 4 RUI options available, the s have the following features:

- **RUI1**
  - Self-Capacitive Channel with GPIO3 Output
  - Hall Channel with GPIO4 Output
  - Temperature Tracking Channel for Hall effect Temperature Compensation
- **RUI2**
  - Self-Capacitive Channel with GPIO3 Output
  - Touch-Hold Output on GPIO4
- **RUI3**
  - I²C Address Strap on GPIO4
- **RUI4**
  - GPIO4 Forced Active

The configuration of the RUIs are defined by the values stored in the One Time Programmable Bytes. The RUIMODE[1:0] bits in *OTPBYTE5* select which RUI is enabled. The subsections below cover all the features of the RUIs and how to configure them.

13.1 RUI System Settings

The system settings are common to all RUIs. Directly after reset the IQS626A operates only in Normal Power Mode until the reset is acknowledged by the master via I²C. The system settings which are applied during this time are listed below. These settings are not configured by the OTP Bytes, but can be changed via I²C after reset.

- **Power Mode:** Normal Power Mode
- **Normal Power Report Rate:** 150ms
- **Auto Power Mode Switching:** Disabled 1
- **Ready Timeout:** 30ms
- **Halt Time:** 40s

All system settings which are configurable by the One Time Programmable Bytes are contained in *OTPBYTE0*, these are described below.

13.1.1 GPIO Type

The GPIOs associated with the RUIs are active high push-pull outputs by default, they can be configured to be active low open-drain outputs by setting the GPIOTYPE bit in *OTPBYTE0*. The

GPIOTYPE bit controls the behaviour of both GPIO3 and GPIO4 for all RUIs which use these pins as outputs.

13.1.2 Ready Type

The Ready pin is an active low open-drain output by default, it can be configured as an active high push-pull output by setting the RDYTYPE bit in *OTPBYTE0*.

13.1.3 I²C Address

The default I²C address is 0x44, it can be set to 0x45 by setting the I2CADDR bit in *OTPBYTE0*.

13.1.4 Main Oscillator Frequency

The main oscillator runs at 16MHz by default, it can be reduced to 4MHz by setting the MOSCFREQ bit in *OTPBYTE0*. Note that setting the main oscillator to 4MHz will affect all time related system settings by multiplying all time settings and dividing all frequency settings by 4.

13.2 Self-Capacitive Channel with GPIO3 Output

This feature is included in RUIs 1 and 2. The Ultra-Low Power (ULP) channel is configured as a self-capacitive channel which outputs Filtered Counts and LTA values as per its standard operation. The touch state of the channel is output on GPIO3, that is, GPIO3 will be set to its active state, as selected with the GPIOTYPE bit in *OTPBYTE0*, whenever the touch threshold on the ULP channel is breached. Conversely, if the touch threshold is not breached, GPIO3 will be in its inactive state.

Settings applied to the ULP channel upon reset are listed below, these settings are not configured by the One Time Programmable Bytes, but can be changed via I²C after reset.

- **Sensor Mode:** Self-Capacitive
- **Base Value:** 100
- **ATI Target:** 576
- **ATI Mode:** Full
- **Proximity Threshold:** 8
- **Conversion Timer Prescaler:** 1/4
- **Prox Cs Size:** 15pF
- **Touch Hysteresis:** 8.20% (Index 5)

Further settings, which are configured by the OTP Bytes, are covered below.

13.2.1 Self-Capacitive Channel CRX Pins

By default, the CRX0 pin is assigned to the ULP channel. The ULP channel can be configured to use CRX2, CRX4, CRX5, CRX6 and CRX7 simultaneously by setting the SCAPCRX bit in *OTPBYTE0*. By setting the SCAPCRX bit, the ULP channel uses all the CRX pins which are normally assigned to the 2x3 Trackpad, this means that the touch detection will be done with the trackpad electrodes if a trackpad is connected. This does not affect the trackpad, the trackpad can still be configured and used as normal.

13.2.2 Self-Capacitive Channel Touch Threshold

The default touch threshold value assigned to the ULP channel is 16. Touch threshold values of 16, 4, 8 and 32 can be selected with the SCAPTHR[1:0] bits in *OTPBYTE5*. The selected value is loaded into the ULP Channel Touch Threshold register, the register value is then used to determine the touch threshold value in terms of counts as follows:

$$ULPTT_{CS} = \left(\frac{ULPTT_{REG}}{256}\right) \times ULP_{LTA} \qquad 13.1$$

Where $ULPTT_{CS}$ is the ULP channel touch threshold in terms of counts, $ULPTT_{REG}$ is the ULP Channel Touch Threshold register value as selected by SCAPTHR[1:0] and ULP_{LTA} is the ULP channel LTA value. Equation *13.1* is applied after every conversion cycle, therefore, $ULPTT_{CS}$ changes dynamically with ULP_{LTA}.

13.3 Hall Channel with GPIO4 Output

This feature is included only in RUI1, the hall channel is enabled and it outputs the Hall Output and Hall Common values as per its standard operation. The touch state of the hall channel is output on GPIO4, that is, GPIO4 will be set to its active state, as selected with the GPIOTYPE bit in *OTPBYTE0*, whenever the touch threshold on the hall channel is breached. Conversely, if the touch threshold is not breached, GPIO4 will be in its inactive state.

Settings applied to the Hall channel upon reset are listed below, these settings are not configured by the One Time Programmable Bytes, but can be changed via I^2C after reset.

- **Sensor Mode:** Hall 3
- **ATI Mode:** Partial
- **Conversion Timer Prescaler:** 1/2
- **Prox Cs Size:** 15pF
- **Touch Hysteresis:** 5.47% (Index 4)

Further settings which are configured by the OTP Bytes are covered below.

13.3.1 Hall Channel ATI Target

A value of 416, 544, 672 or 800 can be selected for the Hall Channel ATI Target with the HALLATI[1:0] bits in *OTPBYTE3*.

13.3.2 Hall Channel Touch Threshold

The Hall Channel Touch Threshold (HTT_{CS}) for RUI1 is calculated from the HALLTHR[5:0] bits contained in *OTPBYTE4*. Firstly, the value for the Hall Touch Threshold register is calculated from HALLTHR[5:0] and saved to the register:

$$HTT_{REG} = (4 \times HALLTHR[5:0]) + 3 \quad 13.2$$

Where HTT_{REG} represents the value stored in the Hall Touch Threshold register. The touch threshold value, in terms of counts, is then calculated from HTT_{REG}:

$$HTT_{CS} = (2 \times HTT_{REG}) + 1 \quad 13.3$$

Where HTT_{CS} represents the hall touch threshold in terms of counts. A direct relationship between HTT_{CS} and HALLTHR[5:0] is then:

$$HTT_{CS} = (8 \times HALLTHR[5:0]) + 7 \quad 13.4$$

The value of HALLTHR[5:0] can be calculated from the desired threshold value as follows:

$$HALLTHR[5:0] = \frac{HTT_{CS} - 7}{8} \quad 13.5$$

WARNING:

Hall Temperature Compensation is enabled for RUI1, therefore HTT_{CS} as calculated in this section is not directly used to determine the touch state. HTT_{CS} is used to calculate $adjHTT_{CS}$ as explained in the Hall Temperature Compensation section. $adjHTT_{CS}$ is then used to determine the touch state.

If Hall Temperature Compensation is disabled then HTT_{CS} is used to determine the touch state.

13.4 Temperature Tracking Channel

This feature is only included in RUI1. Channel GEN2 is configured as a temperature tracking channel which facilitates the Hall Temperature Compensation functionality. The channel outputs 2 values:

- **Temperature Channel Filtered Counts**:

  The Temperature Channel Filtered Counts (T_{CS}) is the 16 bit filtered counts value of channel GEN2 when it is in temperature sensing mode. It can be read from the Generic Channel 2 Filtered Counts register at memory address 0x21.

- **Temperature Channel Reference Value:**

  The Temperature Channel Reference Value (T_{REF}) is the 16 bit value which represents the value of T_{CS} at the desired reference temperature. It replaces the LTA value of channel GEN2 and can be read from the Generic Channel 2 Long Term Average register at memory address 0x22.

Settings applied to the Temperature Tracking channel upon reset are listed below, these settings are not configured by the OTP Bytes, but can be changed via I²C after reset.

- **Sensor Mode:** Temperature
- **Coarse Multiplier:** 0
- **ATI Mode:** Disabled
- **Conversion Timer Prescaler:** 1/2

- **CS Capacitor Size:** 15pF

13.5 Hall Temperature Compensation

The aim of the Hall Temperature Compensation feature is to ensure that the touch state of the hall channel is accurately determined at all times. It is true for all sensing modes that the counts value on the channel will drift as the temperature changes. For the hall channel, this means that the Hall Output may become greater than or less than the Hall Touch Threshold as the counts value changes. Thus resulting in a change in the Hall Touch State even though the magnetic field has remained unchanged.

The Hall Temperature Compensation feature strives to adjust the Hall Channel Touch Threshold in such a way that HTT_{CS} increases or decreases proportionally to the Hall Output, in so doing, maintaining the correct touch state for the channel.

All devices which make use of the Hall Temperature compensation feature are factory calibrated to ensure correct operation.

13.6 Touch-Hold Output on GPIO4

This feature is implemented only in RUI2, it outputs an active pulse on GPIO4 when there is a prolonged touch of 5s on the self-capacitive channel. GPIO4 remains in its active state, as selected with the GPIOTYPE bit in OTPBYTE0, for 30ms before returning to the inactive state.

13.7 I²C Address Strap on GPIO4

This feature is implemented only in RUI3, GPIO4 acts as an input with which the I²C address, as selected with the I2CADDR bit in *OTPBYTE0*, can be altered. If GPIO4 is connected to VSS then bit 1 of the I²C address is set, that is, 0x44 becomes 0x46 and 0x45 becomes 0x47. GPIO4 is only checked upon reset and thus the I²C address cannot be changed during runtime. GPIO4 should be left floating or connected to VDDHI if the selected I²C address is to remain unaltered.

13.8 GPIO4 Forced Active

If RUI4 is selected then GPIO4 will be forced into the active state as selected with the GPIOTYPE bit in *OTPBYTE0*. GPIO4 will remain in the active state until otherwise configured.

	USA	Asia	South Africa
Physical Address	11940 Jollyville Suite 120-S Austin TX 78750 USA	Room 501A, Block A, T-Share International Centre, Taoyuan Road, Nanshan District, Shenzhen, Guangdong, PRC	1 Bergsig Avenue Paarl 7646 South Africa
Postal Address	11940 Jollyville Suite 120-S Austin TX 78750 USA	Room 501A, Block A, T-Share International Centre, Taoyuan Road, Nanshan District, Shenzhen, Guangdong, PRC	PO Box 3534 Paarl 7620 South Africa
Tel	+1 512 538 1995	+86 755 8303 5294 ext 808	+27 21 863 0033
Email	info@azoteq.com	info@azoteq.com	info@azoteq.com

Visit www.azoteq.com
for a list of distributors and worldwide representation.

Patents as listed on www.azoteq.com/patents-trademarks/ may relate to the device or usage of the device.

Appendix A. Detailed Register Descriptions

Version Info

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Full address	Group name	Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x00	Version Info	Product number								Software version								Read-Only
		0x51 – IQS626A								0x01 – Pre-production firmware 0x02 – Production firmware								
0x01		Hardware number								Reserved								Read-Only
		Reserved								Not Accessible Any attempt to read or write this byte will access the following byte.								

- Specific product checks can be done via registers 0x00 – 0x01
- It is recommended to responsibly check for any firmware or hardware changes at start-up.
- Any changes in this regard will be clearly communicated via a product change notice.

Global Flags

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x02	Global flags	System Flags & Power mode flags								Global Event flags								Read-Only
		Show Reset	Reserved		ATI in progress	EVENT	ULP UPDATE	Power mode (see reg 0x80 bits 5:4)		POWER MODE CHANGE	SYSTEM	REFERENCE CHANNEL	RESERVED	GESTURE	DEEP-TOUCH	TOUCH	PROX	

- **Show reset:**
  - "1" indicates the IQS626A has gone through a reset condition and should be initialized again.
- **ATI in progress:**
  - ATI is a procedure that is done to tune the channel for a target sensing performance. During this procedure it is possible to communicate with the device (via RDY window OR I^2C polling). More on ATI.
- **EVENT:**
  - An indicator that an event has occurred. The power mode timer will be reset in this case.
- **ULP update:**
  - Indication of a sensing update on all active channels during ULP mode.
  - During an update event, the LTA (long-term average) counts are updated for all active channels.
  - If there is a valid state change on any of the active channels, normal power will be entered
- **Power mode:** Report of the currently active power mode
  - "00": Normal power (NP) – all channels sampled fast
  - "01": Low power (LP) – all channels samples slow
  - "10": Ultra low power (ULP) – ULP CH0 sampled slow and other channels slowly updated in the background.
  - "11": N/A
- **Global event flags:**
  - POWER MODE – Power mode change has occurred according to the mode timer.
  - SYSTEM – A re-calibration event (ATI), reseed (LTA is made equal to "counts") or reset event has occurred.
  - REFERENCE CHANNEL – A change on a reference channel has occurred and will be applied to a sensing channel. More on reference channels
  - RESERVED
  - GESTURE – A gesture has occurred on the trackpad
  - DEEP TOUCH – An active channel has triggered a "deep touch" threshold
  - TOUCH - An active channel has triggered a "touch" threshold
  - PROX - An active channel has triggered a "proximity" threshold

Gesture Event Flags

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x03	Global flags	Gesture (Trackpad) event flags								Reserved								Read-Only
				HOLD	TAP	NEG_Y_FLICK	POS_Y_FLICK	NEG_X_FLICK	POS_X_FLICK	Not Accessible Any attempt to read or write this byte will access the following byte.								Read-Only

- **Gesture event flags for trackpad implementations:**
  - HOLD – Any sensing element in the “trackpad” has been in touch condition for a time longer than the longest of the tap and swipe gesture time-outs as set in register 0x8A.
  - TAP – Any sensing element in the “trackpad” has received a touch condition for a period shorter than defined in register 0x8A.For full specification of tap event requirements, see register 0x8A definition
  - NEG_Y_FLICK – A flick or swipe detected from top to bottom, depending on the trackpad selected.
  - POS_Y_FLICK - A flick or swipe detected from bottom to top, depending on the trackpad selected.
  - NEG_X_FLICK – A flick or swipe detected from right to left, depending on the trackpad selected.
  - POS_X_FLICK - A flick or swipe detected from left to right, depending on the trackpad selected.

Channel States

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x04	Global flags	Channel Proximity State								Channel Proximity Direction								Read-Only
			Generic CH2	Generic CH1	Generic CH0				ULP CH		Generic CH2	Generic CH1	Generic CH0				ULP CH	
0x05		Channels Touch State								Channels Deep Touch State								Read-Only
		Hall CH	Generic CH2	Generic CH1	Generic CH0			TP	ULP CH		Generic CH2	Generic CH1	Generic CH0				ULP CH	
0x06		Reference Channels Actively Used								Reserved								Read-Only
			Generic CH2	Generic CH1	Generic CH0					Not Accessible Any attempt to read or write this byte will access the following byte.								
0x07		Channel Compensation Minimum Flag								Channel Compensation Maximum Flag								Read-Only
		Hall CH	Generic CH2	Generic CH1	Generic CH0			TP	ULP CH	Hall CH	Generic CH2	Generic CH1	Generic CH0			TP	ULP CH	

- **Channels Proximity State:**
  - When a proximity event has occurred, this register will be updated and report on the proximity state of all channels.
  - “0” – No proximity, “1” – Channel x in proximity.
- **Channels Proximity Direction:**
  - When a threshold trigger is made with the “count value” above the LTA (long term average reference), this bit will be set.
  - With the “count value” below the LTA, this bit will be cleared.
- **Channels Touch State:**
  - When a touch event has occurred, this register will be updated and report on the touch state of all channels.
  - “0” – No touch, “1” – Channel x in touch.
- **Channels Deep Touch State:**
  - When a deep touch event has occurred, this register will be updated and report on the deep touch state of all channels.
  - “0” – No touch, “1” – Channel x in deep touch.
- **Reference Channels Actively Used:**
  - When a reference channel is setup and a REFERENCE CHANNEL event is registered, this register will report which reference channels are actively used.
- **Channel Compensation Minimum Flag:**
  - When a minimum value of 0 compensation is assigned by the ATI algorithm to a specific channel, this register will report which channels they are and possibly not operational.
- **Channel Compensation maximum Flag:**
  - When a maximum value of 1024 compensation is assigned by the ATI algorithm to a specific channel, this register will report which channels they are and possibly not operational.

Trackpad Coordinates

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0x08		X coordinate	Y coordinate	Read-Only
		0 – 128 (2x3 trackpad); 0 – 255 (3x3 trackpad)	0 – 255	

- **X Coordinate:**
  - When a 2x3 element trackpad is assigned, this register will report the weighted X coordinate ranging from 0 - 128.
  - When a 3x3 element trackpad is assigned, this register will report the weighted X coordinate ranging from 0 - 255.
- **Y Coordinate:**

- When either a 2x3 or a 3x3 element trackpad is assigned, this register will report the weighted Y coordinate ranging from 0 - 255.

Counts and LTA

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x09 - 0x22	Raw Counts & LTA	FILTERED COUNTS CHANNEL X (ULP CH0, TP CH's 0 – 9, GEN CH's 0 - 2)																Read-Only
		LONG TERM AVERAGE CHANNEL X (ULP CH0, TP CH's 0 – 9, GEN CH's 0 - 2)																Read-Only

- **Raw Counts & LTA:**
  - The counts reported here are considered the "raw" output of the sensor.
  - The Long Term Average (LTA) value are derived from the raw counts by filtering with a slow IIR filter during inactive states. During activation states the LTA is halted.

Hall-Effect Channel Outputs

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0x23	Hall-effect channel	HALL OUTPUT	Read-Only
0x24		HALL COMMON	Read-Only
0x25		FILTERED COUNTS HALL PLATE 0	Read-Only
0x26		FILTERED COUNTS HALL PLATE 1	Read-Only

- **Hall Output:**
  - This output is the calculated differential offset value between the two Hall-effect plates.
- **Hall Common:**
  - This output is the common or baseline counts of the two Hall-effect plates.
- **Filtered Hall Plate Counts:**
  - These are the two filtered count values for plates 0 and 1.

Reference Channel Deltas

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0x27	Reference Channel Deltas	REFERENCE CHANNEL DELTA FOR ULP CHANNEL	Read-Only
0x28		REFERENCE CHANNEL DELTA FOR TRACKPAD CHANNELS	Read-Only
0x29		REFERENCE CHANNEL DELTA FOR GENERAL CHANNEL 0	Read-Only
0x2A		REFERENCE CHANNEL DELTA FOR GENERAL CHANNEL 1	Read-Only
0x2B		REFERENCE CHANNEL DELTA FOR GENERAL CHANNEL 2	Read-Only

- **Reference Channel Deltas:**
  - The delta values contained in these registers are the values which are subtracted from the LTA values of the respective channels if the respective channel has a reference channel assigned to it. This value is obtained by multiplying the delta value of the reference channel assigned with the respective channel with the Reference Channel Impact Weight (registers 0xAB, 0xB4 and 0xBD).
  - If no reference channel is assigned to the respective channel then the value reads 0.

Power Mode and System Settings

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Full address	Group name	Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x80	Power Mode and System Settings	Power Mode Settings								General settings & commands								Read-Write
		Main oscillator change '0' – 16MHz, '1' – 4MHz	Enable ultra low power (ULP) mode	Auto Power Mode Switching '0' enable '1' disable	Power mode selection (when auto mode switching is disabled) '00' – NP '01' – LP '10' – ULP '11' – Halt mode	ULP Update rate (multiples of ULP sampling rate) '000' – 8, '001' – 13, '010' – 28 '011' – 54, '100' – 89, '101' – 135, '110' – 190, '111' - 256				Reserved (0)	Advanced[1]	Event mode '0' Disable, '1' Enable	Advanced[2]	Advanced[3]	**CMD:** REDO-ATI (Define channels to ATI in reg 0x88 offset 1)	**CMD:** SOFT-RESET	**CMD:** ACK-RESET (Clears "Show reset" – reg 0x02 offset 0 bit 7)	

- **Main oscillator change:**
  - The default of 16MHz allows for rapid charge transfers and other sampling modes.
  - The optional 4MHz allows for slow charge transfers in highly resistive environments with larger capacitive loads in the charge transfer path.
- **Enable CH0 ultra low power (ULP) mode:**
  - By default, automatic power mode switching will only switch between normal power (NP) mode and low power (LP) mode.
  - By setting this bit another power mode step will be available from LP mode to ULP mode.
  - In ULP mode only ULP CH0 will be actively sensed while other channels will be updated at a slower rate (ULP update rate).
- **Auto Power Mode Switching:**
  - If enabled the IQS626A will automatically step power modes if there are no events.
  - For auto-mode switching there should be no user events within a defined time window (register 0x84 offset 1).
  - Custom sampling rates can be defined for each mode.
- **Power mode selection:**
  - NP – Normal power. The power mode intended for use during event changes to allow for a quick response.
  - LP – Low power. The power mode intended for lower power consumption via a fixed sampling period for all channels.
  - ULP – Ultra low power. The power mode intended for use with a proximity or touch wake-up on CH0. Only CH0 is sampled at a regular interval for a defined wake-up response. Other channels are updated via the "ULP update rate" which periodically updates all channels to keep track of drift and channel states.
  - Halt mode – No sensing done on any channel.
- **ULP update rate:**
  - During ULP mode, active channels other than CH0 require to be updated. This is done at a lower rate than CH0 sampling. The rate is defined as a "normal power segment update rate". The update will occur once for every x samples of ULP CH0. Options for "x" are as defined below:

Bit option	Update rate – x – no. of ULP samples (ULP CH0) before all channels are updated
'000'	2
'001'	4
'010'	8
'011'	16
'100'	32
'101'	64
'110'	128
'111'	255

- **Event mode enable:**
  - '0' – Event mode disabled: A communication window will be given after each sample ("streaming mode"). These windows will be indicated on the RDY pin for efficient communications and sampling.
  - '1' – Event mode enabled: A communication window will only be given when an event has occurred that is not masked in register 0x81, offset 1. This window will be indicated on the RDY pin.
    When an event has occurred, a communication window will be given after each sample, until register 0x02 is read.
- **Command REDO-ATI:** Force an ATI event on all or specific channels by setting this bit along with a selection of channels in reg 0x88 offset 1
- **Command SOFT RESET:** Force a software reset condition, clearing all settings made and reverting back to default values for all registers.
- **Command ACK RESET:** Acknowledge the "show reset" bit from register 0x02 here. The "show reset" bit will be cleared after this command.

[1] Advanced setting: Comms during ATI – enable streaming communication during ATI procedure

[2] Advanced setting: Comms in NP – '0' normal event mode, '1' event mode in LP, streaming in NP mode

[3] Advanced Setting: Exit I²C window – End the current communication window and return to sensing operations.

Power Mode and System Settings

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
0x81	Power Mode and System Settings	Global ProxFusion Settings								Global Event Mask (prevent the following event types from being generated)								Read-Write
		Disable ATI Band Check	Trackpad LTA update rate in ULP mode Bits 2:0 = '000' – 2 '001' – 4 '010' – 8 '011' – 16 '100' – 32 '101' – 64 '110' – 128 '111' – 255			ATI_LP (only ATI in LP mode – a more stable time to allow ATI)	GPIO3 touch output channel selection Bits 2:0 = '000' – None '001' – ULP Channel 0 '010' – Trackpad '011' – Trackpad '100' – Generic Channel 0 '101' – Generic Channel 1 '110' – Generic Channel 2 '111' – Hall Channel			Power Mode Change	System (eg ATI, RESET)	Refer-ence channel	Reserve d	Gesture (egSwipe, tap)	Deep-Touch	Touch	Proximity	
0x82		Active Channels								Channel Reseed Enable (Enable "LTA Halt time-out" according to reg 0x85 offset 1)								Read-Write
		Hall CH	Generic CH2	Generic CH1	Generic CH0		3x3 TP	2x3 TP	ULP CH0	Hall CH	Generic CH2	Generic CH1	Generic CH0			TP	ULP CH0	

- **Disable ATI Band Check**
  - '0' ATI band check is enabled.
  - '1' ATI band check is disabled.
  - When the ATI band check is disabled, no ATI will take place when the LTA value for any channel falls outside the selected ATI band for the channel.
  - When the ATI band check is disabled, the ATI Band bit (bit 0) in all Channel ProxFusion Settings 1 registers (addresses 0x88, 0x8B, 0x90, 0xA7, 0xB0 and 0xB9, offset 1) is ignored.
- **Trackpad LTA update rate in ULP mode:**
  - During ULP mode, trackpad channel's LTA values need to be updated. This is done at a lower rate than ULP CH0 sampling. The rate is defined as a "normal power segment update rate". The update will occur once for every x samples of ULP CH0. Options for "x" are as defined below:

Bit option	Update rate – x – no. of ULP CH0 samples before trackpad LTA's are updated
'000'	2
'001'	4
'010'	8
'011'	16
'100'	32
'101'	64
'110'	128
'111'	255

- **ATI_LP**
  - Only allow auto-ATI if the power mode is LP
  - This allows for the ATI algorithm to run only when the proximity or touch states on all active channels are stable.
- **GPIO3 touch output channel selection**
  - The GPIO3 pin can become the touch flag output of any channel.
  - Select any one channel here.
- **Global event mask**
  - Event reporting can be customized here
  - When a bit is set '1', the event will not be reported via RDY indication and event flags.
  - When a bit is cleared '0', the event will be reported via RDY indication and event flags.
  - Event flags will remain set and RDY indication will repeat with each sample until the event flag register is read .
- **Active channels**
  - Choose to activate up to 14 channels.
  - Each channel activated does sensing in a different time-slot.
  - Each time-slot (channel) can be set up in registers 0x8C to 0xC3.
  - Each time-slot can be set up to use any sensing technology from external sensing modes to internal sensors.
  - CH0 is special because it is used as a wake-up channel in ULP mode.
- **Channel reseed enable**
  - Reseed = clear touch and proximity conditions by making LTA (long-term average) = channel counts.
  - "Reseed enable" = Reseed will be done automatically (on the specific channels) after the timer in 0x85 offset 1 runs out.
  - The timer is reset with any events on any of the channels with reseed enabled. When all channels remain in a steady state, the reseed is executed at the same time on all channels.

Report Rates and Timings

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)	Item name (offset 1: bit 7– bit 0)	Data Access
0x83	Report rates and timings	Normal Power Report Rate	Low Power Report Rate	Read-Write
		0-255ms	0-255ms	
0x84		Ultra-Low Power Report Rate (CH0 only – set "NP Segment Update Rate" for periodic update of other channels)	Power Mode Timer	Read-Write
		(x16) 0 – 4080ms	(x512) 0 – 130 560ms	
0x85		RDY time-out	LTA Halt timeout (Proximity / Touch timeout) 0xFF = never timeout	Read-Write
		(x0.512) 0 – 127.5ms Default: 10.24ms	(x512) 0 – 130 560ms	

- **Normal power report rate**
  - Report rate may be chosen in increments of 1ms.
  - A report rate of 0ms and other low values will result in a best effort to do sampling as fast as possible.
  - As a reference, 8 channels doing capacitive sensing (target count = 1000) at 2MHz will take a minimum time of 4ms to complete.
- **Low power report rate**
  - Report rate may be chosen in increments of 1ms.
- **Ultra-low power report rate**
  - Report rate may be chosen in increments of 16ms.
  - Active sensing only done for the ULP CH0.
  - All other channels are updated according to the "ULP update rate" in register 0x80 offset 0 bits 2-0.
- **Power mode timer**
  - Automatic power mode stepping will be done when this timer runs out.
  - The timer will reset when any user event occurs (user event = threshold trigger/release).
  - Power mode timer may be set in increments of 512ms.
- **RDY time-out**
  - A dedicated communication window is given by the RDY window period.
  - This register defines this period.
  - Default: 10.24ms
  - If the RDY window is missed, the IC will still rapidly respond to I^2C address polling.
  - The RDY time-out may be set in increments of 0.512ms.
- **LTA Halt timeout**
  - This timer will cause a reseed on all channels with reseed enabled (register 0x82 offset 1).
  - An exception is 0xFF that will block the potential time-out.
  - LTA Halt timeout may be set in increments of 512ms.

Global Settings

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)						Item name (offset 1: bit 7– bit 0)	Data Access
0x86	Global settings	Reference Channel & Other General Settings						Swipe Gesture Threshold	Read-Write
		Reference Channel Reseed Level '00' – No Event '01' – In Prox '10' – In Touch '11' – In Deep Touch	Extend Thresholds	Enable Reference Channel Tracking UI	Swipe / Flick	Advanced[1]	Trackpad coordinate filter strength '00' 0 (Raw) '01' 1 '10' 2 '11' 3 (Slow)	x1 coordinate	
0x87		Gesture Tap Timeout						Gesture Swipe / Flick Timeout	Read-Write
		(x16) 0 - 4080ms						(x16) 0 - 4080ms	

- **Reference Channel Reseed Level**
  - Specifies the state up to which the reference channel will reseed the associated channel. Higher selection values include the states of the lower selection values.
    - '00' No Event
    - '01' In Proximity
    - '10' In touch
    - '11' In Deep Touch
- **Extend thresholds**
  - This option multiplies all the touch and deep-touch thresholds by 4.
- **Enable Reference Channel Tracking UI**
  - Setting this bit enables the Reference Channel Tracking UI
  - When enabled, this UI will have no effect if the associated sensing channel DOES NOT have a proximity/touch condition.
  - If the associated sensing channel DOES have a proximity/touch condition, the following will happen:
    - The LTA of the reference channel will be halted for the duration of the proximity/touch.
    - The delta on the reference channel will be subtracted from the LTA of the sensing channel.
    - The delta used will have a channel specific "weight" assigned and may be from 0% to 200% of the reference channel delta.
- **Gesture UI selection:**
  - '0' – Flick UI: Gesture must include a touch release. This UI is less prone to unintentional gestures and typically applies cases where safety or water immunity is important.
  - '1' – Swipe UI: Gesture will be generated as soon as the threshold and time conditions are met. This UI will give an improved user experience via optimal responsiveness.
- **Trackpad coordinate filter strength**
  - Trackpad coordinate filter.
  - Values range from raw ('00') to strong & slow ('11') as shown above.
  - Filter is applied for "flick" and "swipe" gesture detection.
  - This filter does not affect "tap" gesture detection, normal channel filters apply in this case.
- **SWIPE gesture threshold**
  - A swipe gesture coordinate change must be more than the gesture threshold chosen here.
  - Validated for both X and Y directions.
- **TAP timeout on slider**
  - A tap (touch & release) within a certain time bound must also adhere to the restriction below.
  - A trackpad coordinate change bound is also applied to the tap gesture. A tap will be rejected if the coordinate change is too big.
  - Tap coordinate shift limit = 0x86, offset 1 (Swipe gesture threshold) divide by 2.
- **SWIPE gesture timeout**
  - A swipe gesture must be below the gesture time-out.

[1] Advanced Setting: 8 Count Reseed Offset – After ATI procedure or reseed event, the LTA counts are forced 8 counts higher (self-capacitance) / lower (mutual capacitance) than the actual measured signal counts.

Global settings

(Back to memory map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
0x88	Global settings	**CMD:** Reseed enable **OR** ATI channel selection if "Redo ATI" bit is set Default: "0000 0000" *By default, no channels will ATI when the "Redo ATI" bit is set. Required channels must be selected here.								Reserved								Read-Write
		Hall CH	Generic CH2	Generic CH1	Generic CH0	Reserved (X)	3x3 TP	3x2 TP	ULP CH0									

- **Command: Reseed / Redo-ATI**
  - By setting only the bits here, a reseed (LTA = sensor count value) will be executed on corresponding channels
  - By setting bits here along with register 0x80 offset 1 bit 2 (Redo ATI command) in the same communication window, the corresponding channels will re-ATI after receiving a valid stop command.
  - Note: If the "reseed" action causes the LTA to fall outside of the "ATI band" (register 0x81 offset 0 bit 7), a re-ATI will be triggered automatically.

ULP Channel Settings

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)			Item name (offset 1: bit 7– bit 0)				Data Access
0x89	ULP channel 0 settings	ULP Channel Prox Threshold			ULP Channel Touch Threshold				Read-Write
		0 – 255 Counts			x/256 of LTA value				
0x8A		ULP Touch Hysteresis			ULP Channel Counts and LTA Filter Settings				Read-Write
		Reserved (X)	Enable Projected	ULP Touch Hysteresis	Counts Filter Strength_NP	Counts Filter Strength_LP	LTA Filter Strength_NP	LTA filter Strength_LP	

- **ULP Channel Prox Threshold**
  - Defines the threshold for Prox state detection.
  - The register value defines the threshold in units of counts.
  - When the channel enters the Prox state, updating of the channel's LTA value will be halted.
- **ULP Channel Touch Threshold**
  - Defines the threshold for Touch state detection.
  - The register value defines the Touch threshold, in terms of counts, according to the formula below:

$$Counts\ Threshold = Register\ Value \times \frac{LTA}{256}$$

- **Enable Projected**
  - Enables projected mode sensing for the ULP channel 0
- **ULP Touch Hysteresis:**
  - The release threshold will be adjusted according to the table below:

Bit setting	Threshold Adjustment Value	Threshold Adjustment Percentage
"0000"	0/256	0.00%
"0001"	1/256	0.39%
"0010"	3/256	1.17%
"0011"	8/256	3.13%
"0100"	14/256	5.47%
"0101"	21/256	8.20%
"0110"	31/256	12.11%
"0111"	42/256	16.41%
"1000"	55/256	21.48%
"1001"	69/256	27.95%
"1010"	85/256	33.20%
"1011"	103/256	40.23%
"1100"	123/256	48.05%
"1101"	144/256	56.25%
"1110"	167/256	65.23%
"1111"	195/256	75.00%

  - The new release threshold in terms of counts will be:

$$Adjusted\ Counts\ Threshold = TRUNC\big(Counts\ Threshold\ \times (1 - \ Threshold\ Adjustment\ Value)\big)$$

- **ULP Channel 0 Raw count and LTA filter settings**
  - Filter strength choices:
    - Weak & fast offers best response rate (Count filter)
    - Weak & fast offers best environmental tracking (LTA filter – prevents a false touch or proximity)
    - Strong & slow offers noise rejection in low SNR cases like proximity sensing (Count filter)
    - Strong & slow offers best performance if detection distance is required to be accurate even for a slow approach (LTA filter – prevent environmental tracking of a slow approach)
  - LTA filter strength (LP)
    - 00 – 5 (weak & fast)
    - 01 – 6
    - 10 – 7
    - 11 – 8 (strong & slow)
  - LTA filter strength (NP)
    - 00 – 7 (weak & fast)
    - 01 – 8
    - 10 – 9
    - 11 – 10 (strong & slow)
  - Count filter strength (LP)
    - 00 – 0 (no filtering)
    - 01 – 1
    - 10 – 2
    - 11 – 3 (strong & slow)
  - Count filter strength (NP)
    - 00 – 1 (weak & fast)
    - 01 – 2
    - 10 – 3
    - 11 – 4 (strong & slow)

ULP Channel Settings

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)							Item name (offset 1: bit 7– bit 0)					Data Access
0x8B	ULP channel 0 settings	ULP Channel ProxSense Settings 0							ULP Channel ProxSense Settings 1					Read-Write
		CS Capacitor Size ‘0’ – 15pF ‘1’ – 60pF	Reserved(0)	Inactive CRx State ‘0’ – Float ‘1’ - Ground	Linearize Counts	Two Sided Detection	Disable count filter ‘0’ = filter ‘1’ = raw	ATI Mode ‘11’ Full ATI ‘10’ Partial ‘01’ Semi-Partial ‘00’ ATI disabled	Increase Charge Cycle Time	Projected mode bias current ‘00’ – 2.5uA ‘01’ – 5uA ‘10’ – 10uA ‘11’ – 20uA	Increase Charge Cycle Time	Sensing frequency selection(16M/4M) ‘00’ 4MHz / 1MHz ‘01’ 2MHz/ 500kHz ‘10’ 1MHz/ 250kHz ‘11’ 500 / 125kHz	ATI Band ‘0’ = 1/8 ‘1’ = 1/16 counts around the target count	

- **CS Capacitor Size**
  - Selects the size of the internal sampling capacitor to use.
    - 0 – 15pF
    - 1 – 60pF
- **Inactive CRx State**
  - CRx pins not used for the current channel are set to this state.
    - 0 – Float inactive CRx pins.
    - 1 – Ground inactive CRx pins.
- **Linearize counts**
  - Counts are automatically linearized.
  - Setting this bit will automatically inverse the logic direction for the ULP channel.
- **Two Sided Detection**
  - Setting this bit will allow Prox, Touch and Deep Touch thresholds to be breeched in both directions.
  - If this bit is cleared then thresholds will breech in one direction while LTA follows rapidly in the other direction.
- **Disable count filter**
  - Disable all filtering of the raw count values that result directly from the charge transfer measurements or other sensor modes.
- **Increase Charge Cycle Time**
  - Increases the Charge Cycle Transfer Time.
  - A larger value results in a longer charge cycle time.
  - See AZD102 for more information about the charge cycle time.
- **Projected mode bias current:**
  - For projected capacitance sensing
- **Increase Charge Cycle Time Enable**
  - Enables the Increase Charge Cycle Time functionality.
- **Sensing frequency:**
  - Select a higher frequency for optimized time and function in some cases
  - Select a lower frequency to reach optimal charge transfers characteristics in capacitive sensing modes containing higher resistance paths and large load capacitors
- **ATI Band**
  - ‘0’ = 1/8
  - ‘1’ = 1/16
  - Recommended value ‘0’ (1/8).
  - Example: 1/8*Target = 0.125*800 = 100; Thus, a band of 100counts above and below the target value is monitored.
  - A band of ‘1’ (1/16) could help in some safety critical applications where very accurate sensitivity is required. If such case the ATI algorithm will converge into a smaller band.

ULP Channel Settings

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)	Item name (offset 1: bit 7– bit 0)	Data Access
0x8C		Auto Tuning Implementation (ATI) Base Value and Target	Reserved	Read-Write
		Base '00' – 75 counts '01' – 100 counts '10' – 150 counts '11' – 200 counts ATI Target (x32) counts	Not Accessible Any attempt to read or write this byte will access the following byte.	
0x8D		Channel Multipliers – normal use is read only	Channel Compensation (ATI) – normal use is read only	Read-Write
		Compensation (MSB: bits 9,8) Coarse Multiplier (ATI) Fine Multiplier (ATI)	Compensation (LSB: bits 7 – 0)	
0x8E		Channel CRX sense pin selection	Channel TRX transmit pin selection	Read-Write
		CRX7 (bit 7) → CRX0 (bit 0)	TRX7 (bit 7) → TRX0 (bit 0)	

- **Channel CRX enable**
  - Choose external sense pad connections here
  - By selecting more than one external pad per channel, a “distributed channel” is formed
  - This register has different functions for different sensor modes:
    - Self-capacitance mode:
      - Each CRX is an external pin
      - Each pin is used for charge transfer “charge” and “discharge” operations
      - CRX1 has a reserved circuit connected, do not include CRX1 in designs where even performance is required over various pins. A slightly less sensitive CRX1 may result when compared to other pins
    - Projected capacitance mode:
      - Each CRX pin is an external pin
      - Each pin is used as a sensitive receiver for projected capacitance
- **Channel TX enable**
  - Choose more external sense pad connections here
  - This register has different functions for different sensor modes:
    - Self-capacitance mode:
      - Each TRX is an external pin definition of the CRX pin state when the pin is not part of any active channel
      - With the corresponding bit set, undefined CRX pins will be GND during sensing conversions of other channels
    - Projected capacitance mode:
      - Each TX pin is an external pin
      - Each pin is used as a transmit pin for projected capacitance

Global Trackpad Settings

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)			Item name (offset 1: bit 7– bit 0)		Data Access
0x8F	Global trackpad settings	Trackpad raw counts filter and Hysteresis			Trackpad Auto Tuning Implementation (ATI) Target		Read-Write
		Count filter beta NP	Count filter beta LP	Hysteresis amount	Reserved	ATI Target (x32)	

- **Raw count and LTA filter settings**
  - Filter strength choices:
    - Weak & fast offers best response rate.
    - Strong & slow offers noise rejection in low SNR cases.
  - Count filter strength (NP)
    - 00 – 1 (weak & fast)
    - 01 – 2
    - 10 – 3
    - 11 – 4 (strong & slow)
  - Count filter strength (LP)
    - 00 – 0 (no filtering)
    - 01 – 1
    - 10 – 2
    - 11 – 3 (strong & slow)
- **Hysteresis for Touch**
  - The release threshold will be adjusted according to the table below:

Bit setting	Threshold % adjustment	Threshold change percentage
“0000”	0/256	0.00%
“0001”	1/256	0.39%
“0010”	3/256	1.17%
“0011”	8/256	3.13%
“0100”	14/256	5.47%
“0101”	21/256	8.20%
“0110”	31/256	12.11%
“0111”	42/256	16.41%
“1000”	55/256	21.48%
“1001”	69/256	27.95%
“1010”	85/256	33.20%
“1011”	103/256	40.23%
“1100”	123/256	48.05%
“1101”	144/256	56.25%
“1110”	167/256	65.23%
“1111”	195/256	75.00%

  - The release threshold will be (Threshold - %Hysteresis) * LTA/256

Global Trackpad Settings

(Back to Register Map)

Full address	Group name	Item name (offset 0: bit 7– bit 0)							Item name (offset 1: bit 7– bit 0)					Data Access
		Trackpad ProxSense Settings 0							Trackpad ProxSense Settings 1					Read-Write
0x90		CS Capacitor Size ‘0’ – 15pF ‘1’ – 60pF	Reserved(0)	Inactive CRx State ‘0’ – Float ‘1’ - Ground	Linearize Counts	Two Sided Detection	Disable count filter ‘0’ = filter ‘1’ = raw	ATI Mode ‘11’ Full ATI ‘10’ Partial ‘01’ Semi-Partial ‘00’ ATI disabled	Increase Charge Cycle Time	Projected mode bias current ‘00’ – 2.5uA ‘01’ – 5uA ‘10’ – 10uA ‘11’ – 20uA	Increase Charge Cycle Time Enable	Sensing frequency selection(16M/4M) ‘00’ 4MHz / 1MHz ‘01’ 2MHz/ 500kHz ‘10’ 1MHz/ 250kHz ‘11’ 500 / 125kHz	ATI Band ‘0’ = 1/8 ‘1’ = 1/16 counts around the target count	

- **CS Capacitor Size**
  - Selects the size of the internal sampling capacitor to use.
    - 0 – 15pF
    - 1 – 60pF
- **Inactive CRx State**
  - CRx pins not used for the current channel are set to this state.
    - 0 – Float inactive CRx pins.
    - 1 – Ground inactive CRx pins.
- **Linearize counts**
  - Counts are automatically linearized.
  - Setting this bit automatically inverses the logic direction for the trackpad channel.
- **Two Sided Detection**
  - Setting this bit will allow Prox, Touch and Deep Touch thresholds to be breeched in both directions.
  - The trackpad will still ATI if the counts move too far in the opposite direction as the intended logic direction.
- **Disable count filter**
  - Disable all filtering of the raw count values that result directly from the charge transfer measurements.
- **Increase Charge Cycle Time**
  - Increases the Charge Cycle Transfer Time.
  - A larger value results in a longer charge cycle time.
  - See AZD102 for more information about the charge cycle time.
- **Projected mode bias current:**
  - For projected capacitance sensing
- **Increase Charge Cycle Time Enable**
  - Enables the Increase Charge Cycle Time functionality.
- **Sensing frequency:**
  - Select a higher frequency for optimized time and function in some cases
  - Select a lower frequency to reach optimal charge transfers characteristics in capacitive sensing modes containing higher resistance paths and large load capacitors
- **ATI Band**
  - ‘0’ = 1/8
  - ‘1’ = 1/16
  - Recommended value ‘0’ (1/8).
  - Example: 1/8*Target = 0.125*800 = 100; Thus, a band of 100counts above and below the target value is monitored.
  - A band of ‘1’ (1/16) could help in some safety critical applications where very accurate sensitivity is required. If such case the ATI algorithm will converge into a smaller band.

I²C Control Settings

(Back to Register Map)

0xF10A	I²C Control Settings	I²C Control Settings									Read-Write
		I²C End Window	I²C Disable Stop Condition Handling	I²C Disable Read Only	I²C Sleep During Ready Window	Internal use. Retain data when writing	Internal use. Retain data when writing	Internal use. Retain data when writing	Internal use. Retain data when writing	Not Accessible	

- **I²C End Window:**
  - Setting this bit ends the communication window when the I²C Disable Stop Condition Handling bit is set.
- **I²C Disable Stop Condition Handling:**
  - Setting this bit causes the IQS626A to ignore stop commands from the master. The communication window must then be closed by setting the I²C End Window bit.
- **I²C Disable Read Only:**
  - Setting this bit allows Read Only bytes to be modified.
- **I²C Sleep During Ready Window:**
  - When this bit is set the IQS626A will enter a low power mode after opening the communication window. It should set if the user does not intend to perform communication during every ready window or if delays between the start of a communication window and the start of communication are expected. This results in reduced power consumption, however, the IQS626A will clock stretch slightly longer when it is first addressed.

Trackpad Channel settings

(Back to Register Map)

Full address per trackpad channel number									Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
0	1	2	3	4	5	6	7	8	Bit 7							Bit 0	Bit 7							Bit 0	
0x91	0x93	0x95	0x97	0x99	0x9B	0x9D	0x9F	0xA1	Channel Touch Threshold (x1) 0 - 255 counts								Auto Tuning Implementation (ATI) Base (= x + 45) 45 – 300 counts								Read-Write
0x92	0x94	0x96	0x98	0x9A	0x9C	0x9E	0xA0	0xA2	Channel Multipliers – normal use is read only								Channel Compensation (ATI) – normal use is read only								Read-Write
									Compen-sation (MSB: bits 9,8)	Coarse Mutliplier (ATI)	Fine Multiplier (ATI)						Compensation (LSB: bits 7 – 0)								

- **2x3 Trackpad Channel Allocation:**
  - Trackpad channels 0 – 5 is activated and setup according to registers 0x91 – 0x9C.
  - The layout should be as follow:
    - Rx0: Use CRX2
    - Rx1: Use CRX4
    - Rx2: Use CRX6
    - Tx0: Use CRX7
    - Tx1: Use CRX5

❖ TP0 = Rx0 + Tx0 ❖ TP1 = Rx1 + Tx0 ❖ TP2 = Rx2 + Tx0
❖ TP3 = Rx0 + Tx1 ❖ TP4 = Rx1 + Tx1 ❖ TP5 = Rx2 + Tx1

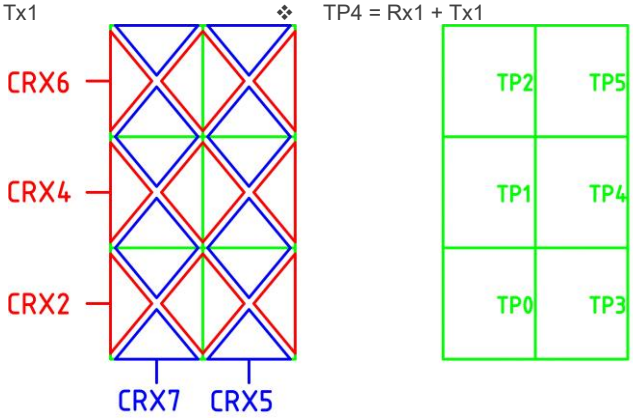

Figure 13.1: 2x3 Trackpad implementation

- **3x3 Trackpad Channel Allocation:**
  - Trackpad channels 0 – 8 is activated and setup according to registers 0x91 – 0xA2.
  - The layout should be as follow:
    - Rx0: Use CRX2
    - Rx1: Use CRX4
    - Rx2: Use CRX6
    - Tx0: Use CRX7
    - Tx1: Use CRX5
    - Tx2: Use CRX3 (additional to the 2x3 TP)

❖ TP0 = Rx0 + Tx0
❖ TP3 = Rx0 + Tx1
❖ TP6 = Rx0 + Tx2
❖ TP1 = Rx1 + Tx0
❖ TP4 = Rx1 + Tx1
❖ TP7 = Rx1 + Tx2
❖ TP2 = Rx2 + Tx0
❖ TP5 = Rx2 + Tx1
❖ TP8 = Rx2 + Tx2

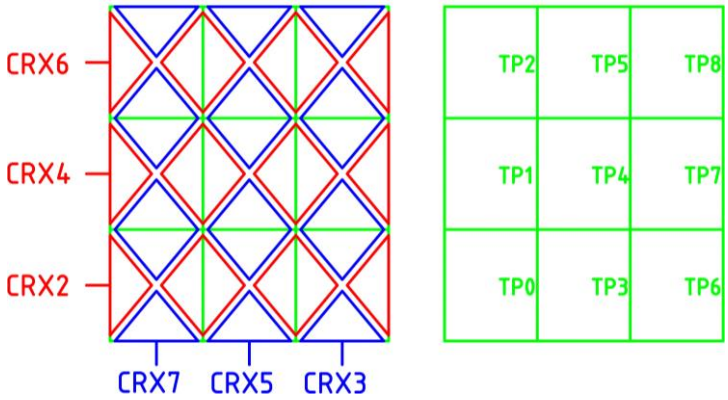

Figure 13.2: 3x3 Trackpad implementation

- **Channel Touch and Deep Touch Threshold**
  - Defines the thresholds for Touch and Deep Touch state detection.
  - When the channel enters the Touch state, updating of the channel's LTA value will be halted.
  - The register value defines the Touch threshold, in terms of counts, according to the formula below:

$$Counts\ Threshold = Register\ Value \times \frac{LTA}{256}$$

Generic Channel settings

(Back to Register Map)

Full address per generic channel number			Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
0	1	2	Bit 7							Bit 0	Bit 7							Bit 0	
0xA3	0xAC	0xB5	Channel Prox Threshold (x1) 0 – 255 counts								Channel Touch Threshold x/256 of LTA value								Read-Write
0xA4	0xAD	0xB6	Channel Deep Touch Threshold x/256 of LTA value								Reserved Not Accessible Any attempt to read or write this byte will access the following byte.								Read-Write
0xA5	0xAE	0xB7	Channel Hysteresis (Proximity has a fixed 4 sample debounce) Deep Touch Hysteresis				Touch Hysteresis				Auto Tuning Implementation (ATI) Base and Target ATI Base '00' – 75 counts '01' – 100 counts '10' – 150 counts '11' – 200 counts				ATI Target (x32)				Read-Write
0xA6	0xAF	0xB8	Channel Multipliers – normal use is read only Compensation (MSB: bits 9,8)		Coarse Multiplier (ATI)		Fine Multiplier (ATI)				Channel Compensation (ATI) – normal use is read only Compensation (LSB: bits 7 – 0)								Read-Write

- **Channel Prox Threshold**
  - Defines the threshold for Prox state detection.
  - The register value defines the threshold in units of counts.
  - When the Prox threshold is breeched, updating of the channel's LTA value will be halted.
- **Channel Touch and Deep Touch Threshold**
  - Defines the thresholds for Touch and Deep Touch state detection.
  - The register value defines the Touch threshold, in terms of counts, according to the formula below:

$$Counts\ Threshold = Register\ Value \times \frac{LTA}{256}$$

- **Touch and Deep Touch Hysteresis:**
  - The release threshold will be adjusted according to the table below:

Bit setting	Threshold Adjustment Value	Threshold Adjustment Percentage
"0000"	0/256	0.00%
"0001"	1/256	0.39%
"0010"	3/256	1.17%
"0011"	8/256	3.13%
"0100"	14/256	5.47%
"0101"	21/256	8.20%
"0110"	31/256	12.11%
"0111"	42/256	16.41%
"1000"	55/256	21.48%
"1001"	69/256	27.95%
"1010"	85/256	33.20%
"1011"	103/256	40.23%
"1100"	123/256	48.05%
"1101"	144/256	56.25%
"1110"	167/256	65.23%
"1111"	195/256	75.00%

  - The new release threshold in terms of counts will be:

$$Adjusted\ Counts\ Threshold = TRUNC(Counts\ Threshold\ \times (1 - \ Threshold\ Adjustment\ Value))$$

Generic Channel settings

(Back to Register Map)

Full address per generic channel number			Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
0	1	2	Bit 7							Bit 0	Bit 7							Bit 0	
			Generic Channel ProxFusion Settings 0								Generic Channel ProxFusion Settings 1								Read-Write
0xA7	0xB0	0xB9	CS Capacitor Size '0' – 15pF '1' – 60pF	Reserved (0)	Inactive CRx State '0' – Float '1' - Ground	Linearize Counts	Two Sided Detection	Disable count filter '0' = filter '1' = raw	ATI Mode '11' Full ATI '10' Partial '01' Semi-Partial '00' ATI disabled		Increase Charge Cycle Time [3:2]		Projected mode bias current '00' – 2.5uA '01' – 5uA '10' – 10uA '11' – 20uA		Increase Charge Cycle Time Enable	Sensing frequency selection (16M/4M) '00' 4MHz / 1MHz '01' 2MHz/500kHz '10' 1MHz/250kHz '11' 500 / 125kHz		ATI Band '0' = 1/8 '1' = 1/16 counts around the target count	

- **CS Capacitor Size:**
  - Selects the size of the internal sampling capacitor to use.
    - 0 – 15pF
    - 1 – 60pF
- **Inactive CRx State:**
  - CRx pins not used for the current channel are set to this state.
    - 0 – Float inactive CRx pins.
    - 1 – Ground inactive CRx pins.
- **Linearize counts:**
  - Setting this bit enables counts linearization.
  - This will cause the delta to form in the opposite direction, therefore, the Inverse Logic Direction bit should also be set if Two Sided Detection is not enabled.
- **Two Sided Detection:**
  - Setting this bit will allow Prox, Touch and Deep Touch thresholds to be breeched in both directions.
  - If this bit is cleared then thresholds will breech in one direction while LTA follows rapidly in the other direction.
- **Increase Charge Cycle Time [3:2]:**
  - Works in conjunction with Increase Charge Cycle Time [1:0] to increase the charge cycle time.
  - A larger value of Increase Charge Cycle Time [3:0] results in a longer charge cycle time.
  - See AZD102 for more information about the charge cycle time.
- **Disable count filter:**
  - Disable all filtering of the raw count values that result directly from the charge transfer measurements.
- **Projected mode bias current:**
  - For projected capacitance sensing
- **Increase Charge Cycle Time Enable:**
  - Enables the Increase Charge Cycle Time functionality.
- **Sensing frequency:**
  - Select a higher frequency for optimized time and function in some cases
  - Select a lower frequency to reach optimal charge transfers characteristics in capacitive sensing modes containing higher resistance paths and large load capacitors
- **ATI Band**
  - '0' = 1/8
  - '1' = 1/16
  - Recommended value '0' (1/8).
  - Example: 1/8*Target = 0.125*800 = 100; Thus, a band of 100counts above and below the target value is monitored.
  - A band of '1' (1/16) could help in some safety critical applications where very accurate sensitivity is required. If such case the ATI algorithm will converge into a smaller band.

Generic Channel settings

(Back to Register Map)

Full address per generic channel number			Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
0	1	2	Bit 7							Bit 0	Bit 7							Bit 0	
0xA8	0xB1	0xBA	Channel ProxFusion Settings 2								Channel ProxFusion Settings 3								Read-Write
			Internal Load Capacitor Size ‘00’ 0.5pF ‘01’ 1.0pF ‘10’ 1.5pF ‘11’ 2.0pF		Enable Internal Load Capacitor	Reserved (0)	Sensor mode ‘0000’ – Surface ‘0001’ – Projected ‘1000’ – Self inductance ‘1001’ – Mutual inductance ‘1100’ – External (PIR) ‘1110’ – HALL ‘1111’ – Temperature				Reserved (Z)	Reserved (0)	Tx Frequency ‘00’ – FOSC ‘01’ – FOSC/2 ‘10’ – FOSC/4 ‘11’ – FOSC/8		Reserved (0)		Inverse Logic Direction	

- **Internal Load Capacitor Size Selection:**
  - Selects the size of the internal load capacitance to be added to the sensor channel.
  - Only in effect if the “Enable Internal Load Capacitor” bit is set. Otherwise load capacitance is 0pF.
- **Enable Internal Load Capacitor**
  - Enable the small internal capacitance (0.5 – 2pF range) to the sensor.
- **Sensor mode**
  - **Self-capacitance**
    - Excitation and measurements are done on the same pin
    - Any pin can be used for self-capacitance measurements
  - **Projected capacitance**
    - Projected channel setup has a very flexible implementation on the IQS626A
    - Any of the 8 channels may be any combination of TX pins and CRX pins
    - Self-capacitance may be selected for one channel and projected capacitance for another, giving more information about a trigger than available on a single sensing mode
  - **Self-inductance**
    - Please contact Azoteq for application guidance
  - **Mutual inductance**
    - Please contact Azoteq for application guidance
  - **External (PIR)**
    - External mode allows for the detection of very small changes in current or voltage from an external element such as a PIR element or piezo element
  - **HALL**
    - An internal HALL pad offers the ability to detect the HALL effect and make use of the IQS626A’s multi direction, multi threshold trigger levels
    - No external connections are required for this mode
  - **Temperature**
    - An internal temperature sensor can be used to track temperature changes.
- **Tx Frequency**
  - Selects the transfer pin switching frequency for sensor modes which use a Tx pin.
    - 0b00 – FOSC
    - 0b01 – FOSC/2
    - 0b10 – FOSC/4
    - 0b11 – FOSC/8
- **Inverse Logic Direction**
  - Setting this bit will cause the Prox, Touch and Deep Touch threshold detection to take place in the opposite direction.
  - If Two Sided detection is not enabled then the LTA will follow the counts value rapidly in the in the direction opposite to the detection direction.

Generic Channel settings

(Back to Register Map)

Full address per generic channel number			Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
0	1	2	Bit 7							Bit 0	Bit 7							Bit 0	
			Channel ProxFusion Settings 4								Channel raw counts and filter settings								Read-Write
0xA9	0xB2	0xBB	Reserved (Z)	Inactive CRx to VReg (If Inactive CRx State = 0)	Increase Charge Cycle Time [1:0]		Reserved (0)	Reserved (0)	Disable Compensation	Static Fine Multipliers	Counts Filter Strength_NP		Counts Filter Strength_LP		LTA Filter Strength_NP		LTA filter Strength_LP		

- **Inactive CRx to Vreg**
  - This bit is only effective if the Inactive CRx State in bit in the Channel ProxFusion Settings 0 register is cleared (set to float inactive CRx pins).
  - CRx pins not used for the current channel are set to this state.
    - 0 – Float inactive CRx pins.
    - 1 – Tie Inactive CRx pins to VReg.

- **Increase Charge Cycle Time [1:0]**
  - Works in conjunction with Increase Charge Cycle Time [3:2] to increase the charge cycle time.
  - A larger value of Increase Charge Cycle Time results in a longer charge cycle time.
  - See AZD102 for more information about the charge cycle time.

- **Disable Compensation**
  - Disables the compensation value, the result is that only the coarse and fine multiplier values will affect the counts.
  - The ATI Mode should be set to Disable when using this feature.

- **Static Fine Multipliers**
  - Setting this bit connects the fine multipliers to the sampling capacitor throughout the sensing period. This results in optimal current consumption for constant current sensing modes.
  - It is recommended to set this bit for constant current sensing modes such as hall sensing, temperature sensing and external current sensing.

- **Raw count and LTA filter settings**
  - Filter strength choices:
    - Weak & fast offers best response rate (Count filter)
    - Weak & fast offers best environmental tracking (LTA filter – prevents a false touch or proximity)
    - Strong & slow offers noise rejection in low SNR cases like proximity sensing (Count filter)
    - Strong & slow offers best performance if detection distance is required to be accurate even for a slow approach (LTA filter – prevent environmental tracking of a slow approach)
  - LTA filter strength (LP)
    - 00 – 5 (weak & fast)
    - 01 – 6
    - 10 – 7
    - 11 – 8 (strong & slow)
  - LTA filter strength (NP)
    - 00 – 7 (weak & fast)
    - 01 – 8
    - 10 – 9
    - 11 – 10 (strong & slow)
  - Count filter strength (LP)
    - 00 – 0 (no filtering)
    - 01 – 1
    - 10 – 2
    - 11 – 3 (strong & slow)
  - Count filter strength (NP)
    - 00 – 1 (weak & fast)
    - 01 – 2
    - 10 – 3
    - 11 – 4 (strong & slow)

Generic Channel settings

(Back to Register Map)

Full address per generic channel number			Item name (offset 0: bit 7– bit 0)								Item name (offset 1: bit 7– bit 0)								Data Access
0	1	2	Bit 7							Bit 0	Bit 7							Bit 0	
0xAA	0xB3	0xBC	Channel Rx Selection								Channel Tx Selection								Read-Write
			CRX7 (bit 7) → CRX0 (bit 0)								CRX7 (bit 7) → CRX0 (bit 0)								
0xAB	0xB4	0xBD	Reference Channel Association								Reference Channel Impact Weight (if this channel is associated to reference channel – 0 = no impact, 255 = 200% impact)								Read-Write
			Hall CH	Generic CH2	Generic CH1	Generic CH0			TP	ULP CH0	x/255 * 2 (0% – 200%)								

- **Channel Rx Enable:**
  - Choose external sense pad connections here
  - By selecting more than one external pad per channel, a “distributed channel” is formed
  - This register has different functions for different sensor modes:
    - Self-capacitance mode:
      - Each CRX is an external pin
      - Each pin is used for charge transfer “charge” and “discharge” operations
      - CRX1 has a reserved circuit connected, do not include CRX1 in designs where even performance is required over various pins. A slightly less sensitive CRX1 may result when compared to other pins
    - Projected capacitance mode:
      - Each CRX pin is an external pin
      - Each pin is used as a sensitive receiver for projected capacitance
    - HALL sensor mode:
      - No CRX pins are externally connected
      - CRX register is re-purposed for HALL channel setup
      - Select CRX0 for the HALL pad
      - Select CRX0 and CRX6 for the inverse HALL pad
      - For HALL sensor mode, all other CRX bits should be set to ‘0’
      - Two channels, “HALL pad” and “inverse HALL” pad is required for accurate HALL effect detection
- **Channel TX Enable**
  - Choose more external sense pad connections here
  - This register has different functions for different sensor modes:
    - Self-capacitance mode:
      - Each TRX is an external pin definition of the CRX pin state when the pin is not part of any active channel
      - With the corresponding bit set, undefined CRX pins will be GND during sensing conversions of other channels
    - Projected capacitance mode:
      - Each TX pin is an external pin
      - Each pin is used as a transmit pin for projected capacitance
    - HALL sensor mode:
      - No CRX pins are externally connected
      - Select all TX pins for defining the state of unused external pins
- **Reference Channel Association**
  - Setting these bits will turn the respective generic channel into a reference channel with the associated channels corresponding to the selected bits.
- **Reference Channel Impact Weight**
  - When the Reference Channel Tracking UI is enabled, the LTA adjustment value is calculated as the product of the reference channel delta and the weight selected by this register. The formula is as follows:

$$Adjustment\ Value = Reference\ Channel\ Delta \times Reference\ Channel\ Impact\ Weight$$

where

$$Reference\ Channel\ Impact\ Weight = \frac{2 \times Register\ Value}{256}$$

Hall Channel settings

(Back to Register Map)

Hall channel	Item name (offset 0: bit 7– bit 0)							Item name (offset 1: bit 7– bit 0)							Data Access
	Bit 7						Bit 0	Bit 7						Bit 0	
0xBE	Hall settings							Hall Touch Threshold							Read-Write
	CS Capacitor Size '0' – 15pF '1' – 60pF	Reserved (0)	Inactive CRx State '0' – Float '1' - Ground	Linearize Counts	Two Sided Detection	Disable Count Filter	ATI_mode '11' Full ATI '10' Partial '01' Semi-Partial '00' ATI disabled	x/256 of LTA value							
0xBF	Hall channel hysteresis							Auto Tuning Implementation (ATI) Base Value and Target							Read-Write
	Reserved (0)		Reserved (Z)		Hall Touch Hysteresis			ATI base value '00' – 75 counts '01' – 100 counts '10' – 150 counts '11' – 200 counts		ATI Target (x32) counts					
0xC0	Channel Multipliers – normal use is read only							Channel Compensation (ATI) – normal use is read only							Read-Write
	Compensation (MSB: bits 9,8)		Coarse operating point (ATI)		Fine operating point (ATI)			Compensation (LSB: bits 7 – 0)							

- **CS Capacitor Size**
  - Selects the size of the internal sampling capacitor to use.
    - 0 – 15pF
    - 1 – 60pF
- **Inactive CRx State**
  - CRx pins not used for the current channel are set to this state.
    - 0 – Float inactive CRx pins.
    - 1 – Ground inactive CRx pins.
- **Linearize counts**
  - Setting this bit enables counts linearization.
  - This will cause the delta to form in the opposite direction, therefore, the Inverse Logic Direction bit should also be set if Two Sided Detection is not enabled.
- **Two Sided Detection**
  - Setting this bit will allow Prox, Touch and Deep Touch thresholds to be breeched in both directions.
- **Disable Count Filter**
  - Setting this bit disables the filter on the Hall Output value. The Hall Output will then be a raw and independent value for each conversion.
- **Hall Touch Threshold**
  - Defines the threshold for Touch state detection.
  - The register value defines the Touch threshold, in terms of counts, according to the formula below:

$$Counts\ Threshold = Register\ Value \times \frac{LTA}{256}$$

- **Hall Touch Hysteresis:**
  - The release threshold will be adjusted according to the table below:

Bit setting	Threshold Adjustment Value	Threshold Adjustment Percentage
"0000"	0/256	0.00%
"0001"	1/256	0.39%
"0010"	3/256	1.17%
"0011"	8/256	3.13%
"0100"	14/256	5.47%
"0101"	21/256	8.20%
"0110"	31/256	12.11%
"0111"	42/256	16.41%
"1000"	55/256	21.48%
"1001"	69/256	27.95%
"1010"	85/256	33.20%
"1011"	103/256	40.23%
"1100"	123/256	48.05%
"1101"	144/256	56.25%
"1110"	167/256	65.23%
"1111"	195/256	75.00%

  - The new release threshold in terms of counts will be:

$$Adjusted\ Counts\ Threshold = TRUNC(Counts\ Threshold\ \times (1 - \ Threshold\ Adjustment\ Value))$$

Appendix B. Detailed One-Time Programmable Byte Descriptions

One-Time Programmable Byte 0 (OTPBYTE0)

Bit No.	7	6	5	4	3	2	1	0
Assignment	MOSCFREQ	SCAPCRX	I2CADDR	RDYTYPE	IOTYPE	RESERVED		

Bit 7 – MOSCFREQ: Main Oscillator Frequency selection bit

Selects the main Oscillator Frequency

0: 16MHz

1: 4MHz

Bit 6 - SCAPCRX: Self Capacitive Channel CRX Pin selection bit

Selects the Self Capacitive Channel CRX Pins to be used.

0: CRX0

1: CRX2, CRX4, CRX5, CRX6, CRX7 (All 2x3 TP CRX pins)

Bit 5 - I2CADDR: I²C Address selection bit

Selects the 7-bit I²C Address which the IQS626 will respond to.

0: 0x44

1: 0x45

Bit 4 - RDYTYPE: Ready Type selection bit

Selects Ready Type to be used.

0: Open-Drain - Active Low

1: Push-Pull - Active High

Bit 3 - GPIOTYPE: GPIO Type selection bit

Selects GPIO Type to be used.

0: Push-Pull - Active High

1: Open-Drain - Active Low

One-Time Programmable Byte 3 (OTPBYTE3)

Bit No.	7	6	5	4	3	2	1	0
Assignment	HALLATI[7:6]							

Bits 7:6 - HALLATI[1:0]: Hall Channel ATI Target selection bits

Selects the Hall Channel ATI Target when RUI1 is enabled.

0b00: 416

0b01: 544

0b10: 672

0b11: 800

One-Time Programmable Byte 4 (OTPBYTE4)

Bit No.	7	6	5	4	3	2	1	0
Assignment	HALLTHR[5:0]						RESERVED	

Bits 7:2 - HALLTHR[5:0]: Hall Channel Touch Threshold assignment bits

Assigns the *Hall Channel Touch Threshold* (HTT_{CS}) of the hall channel when RUI1 is enabled.

HTT_{CS} Range: 7-511

HTT_{CS} is calculated from HALLTHR[5:0] as follows:

$$HTT_{CS} = (8 \times HALLTHR[5:0]) + 7 \quad (13.6)$$

The value of HALLTHR[5:0] can be calculated from the desired threshold value as follows:

$$HALLTHR[5:0] = \frac{HTT_{CS} - 7}{8} \quad (13.7)$$

One-Time Programmable Byte 5 (OTPBYTE5)

Bit No.	7	6	5	4	3	2	1	0
Assignment	RESERVED				RUIMODE[1:0]		SACPTHR[1:0]	

Bits 3:2 - RUIMODE[1:0]: Reset User Interface Mode selection bits

Selects the Reset User Interface (RUI) to be used.

0b00:	RUI1	*Self-Capacitive Channel with GPIO3 Output*
		Hall Channel with GPIO4 Output
		Temperature Tracking Channel
		Hall Temperature Compensation
0b01:	RUI2	*Self-Capacitive Channel with GPIO3 Output*
		Touch-Hold Output on GPIO4
0b10:	RUI3	*I2C Address Strap on GPIO4*
0b11:	RUI4	*GPIO4 Forced Active*

Bits 1:0 - SCAPTHR[1:0]: Self Capacitive Channel Threshold selection bits

Selects the Self Capacitive Channel Touch Threshold (ULPTT CS).

0b00: 16

0b01: 4

0b10: 8

0b11: 32

The touch threshold in terms of counts is calculated as follows:

$$ULPTT_{CS} = \left(\frac{ULPTT_{REG}}{256}\right) \times ULP_{LTA} \quad (13.8)$$

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