

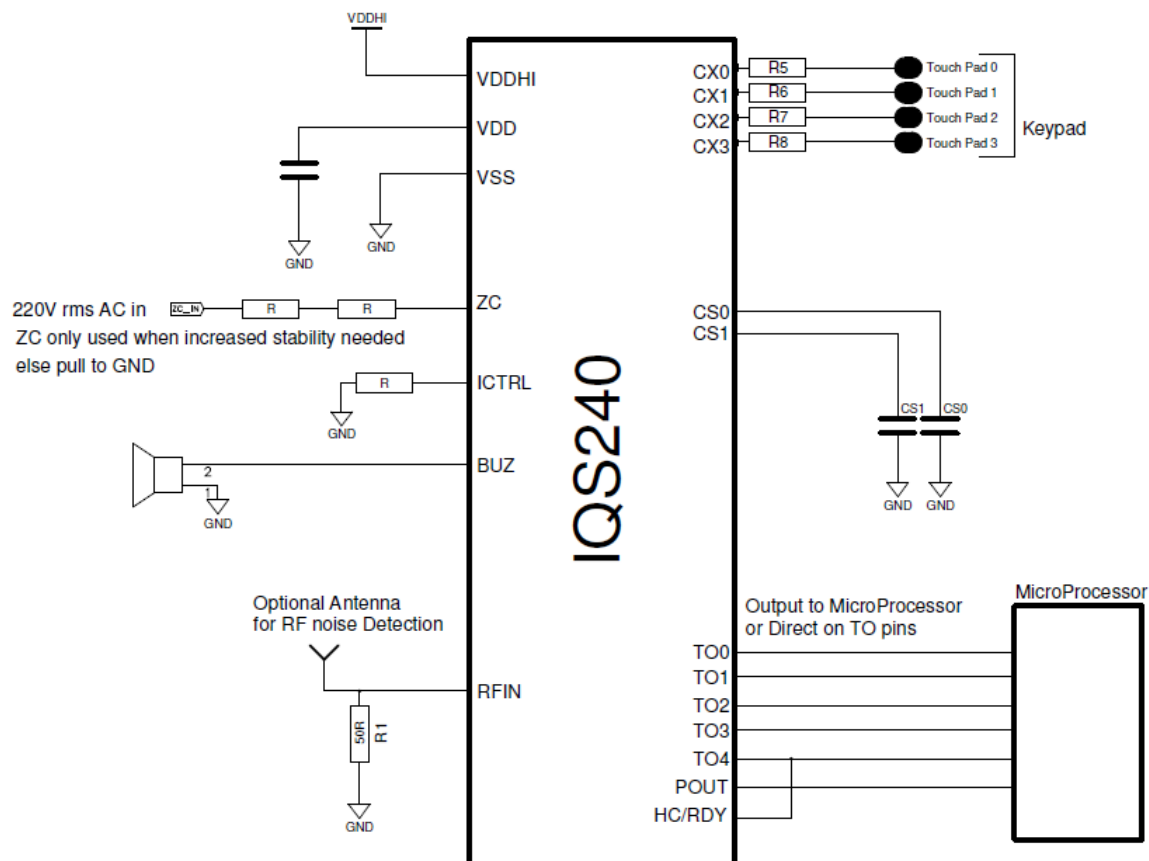


IQS240 Evaluation Kit

IQS240EV02 (AZP100 PCB)

**IQS240 Features****4-Channel Touch Sensor with advanced Proximity detection capability**

- Class leading proximity sensitivity
- Direct, Coded and Serial Operation
- Automatic Environment Compensation
- On-Chip Integrated Series regulator
- On-Chip Digital Signal Processing
- Synchronisable to external source (including AC supply voltage)
- Suitable for various dielectric overlays
- Detect Touch through an overlay of up to 7mm
- User selectable Proximity and Touch sensitivity settings
- Low Power Mode suitable for battery applications (27uA)
- Available in SO-20 and QFN4x4-20 packages

**Figure 1: Typical Connection Diagram for IQS240****IQS240EV02 Evaluation Kit**



IQS240 is offered in SO-20 and QFN(4x4)-20 packages. The module is assembled with an SO-20 device.

Standalone Mode: Connect V⁺ and V⁻ to supply voltage or flip switch to ON position if optional battery kit is supplied. (Note: Remove battery before connecting to PSU). Connecting the unit to a grounded supply will improve stability and sensitivity.

Debug Mode: Module can be connected to VisualProxSense on the SPI header to evaluate the real-time working of the IQS technology (see Application Note for further details: “AZD006 – Visual ProxSense overview”).

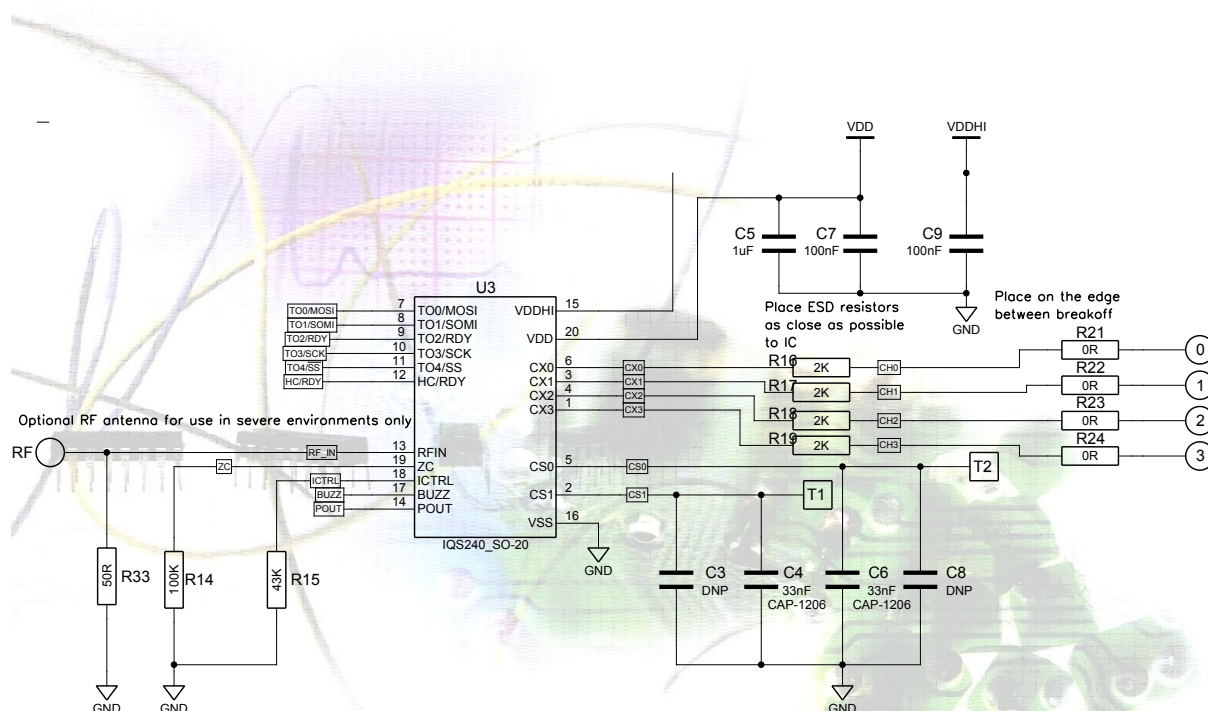


Figure 2: IQS240 Reference Design

The module is designed such that the keypad section may be reversed from the main board. This allows the main unit to be connected to a project keypad for prototyping.

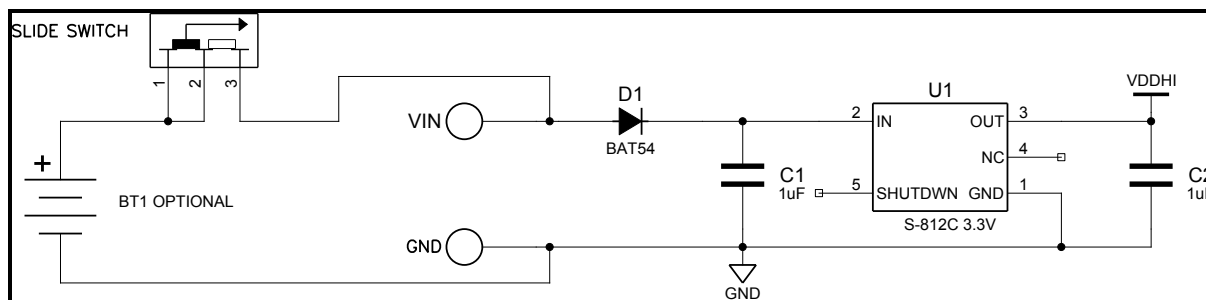


Figure 3 Optional: Regulator stage (with reverse voltage protection).

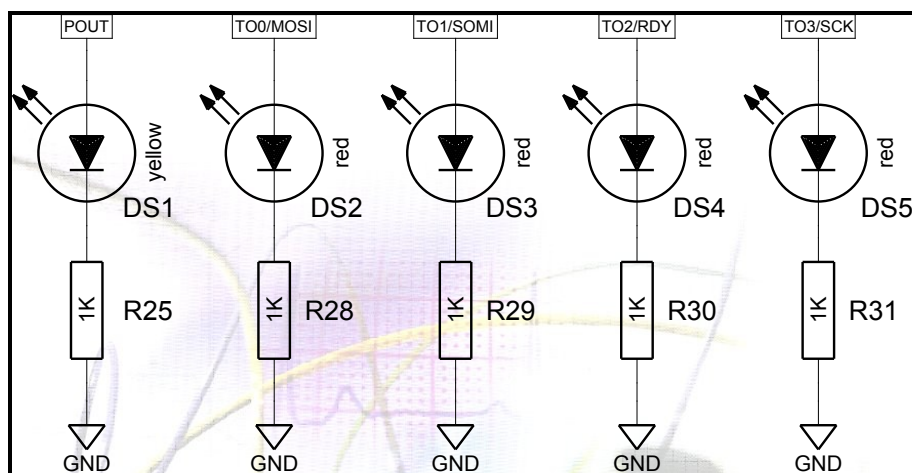


Figure 4: Optional LEDs to indicate active outputs in direct and coded mode (1 Proximity and 4 Touch indicators).

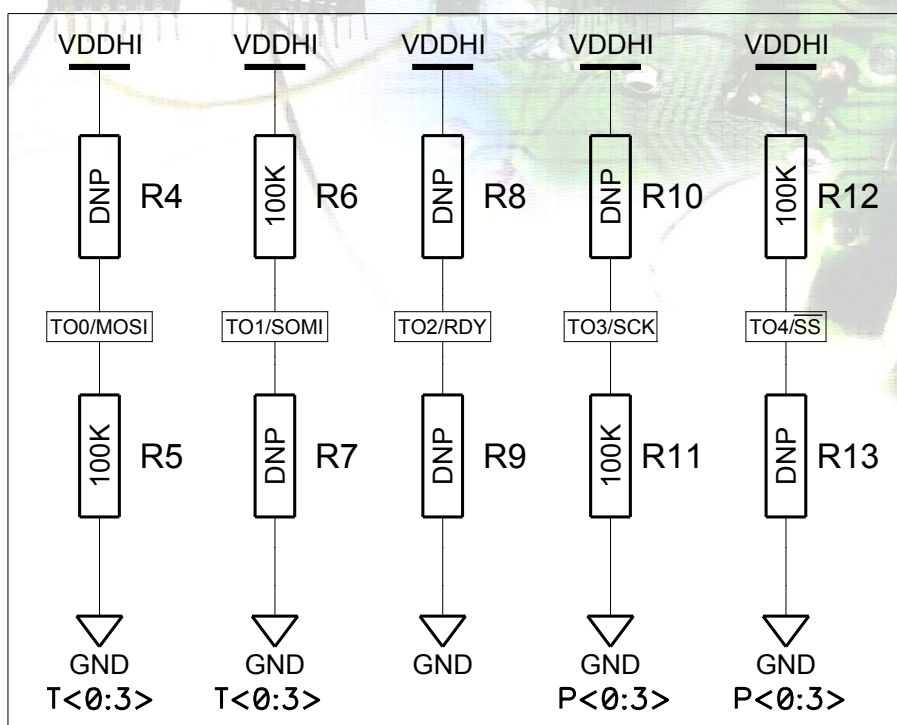


Figure 5: Optional external selections for prototyping. (See datasheet). Typically these settings will be programmed on-chip in mass production, negating the need for these resistors.

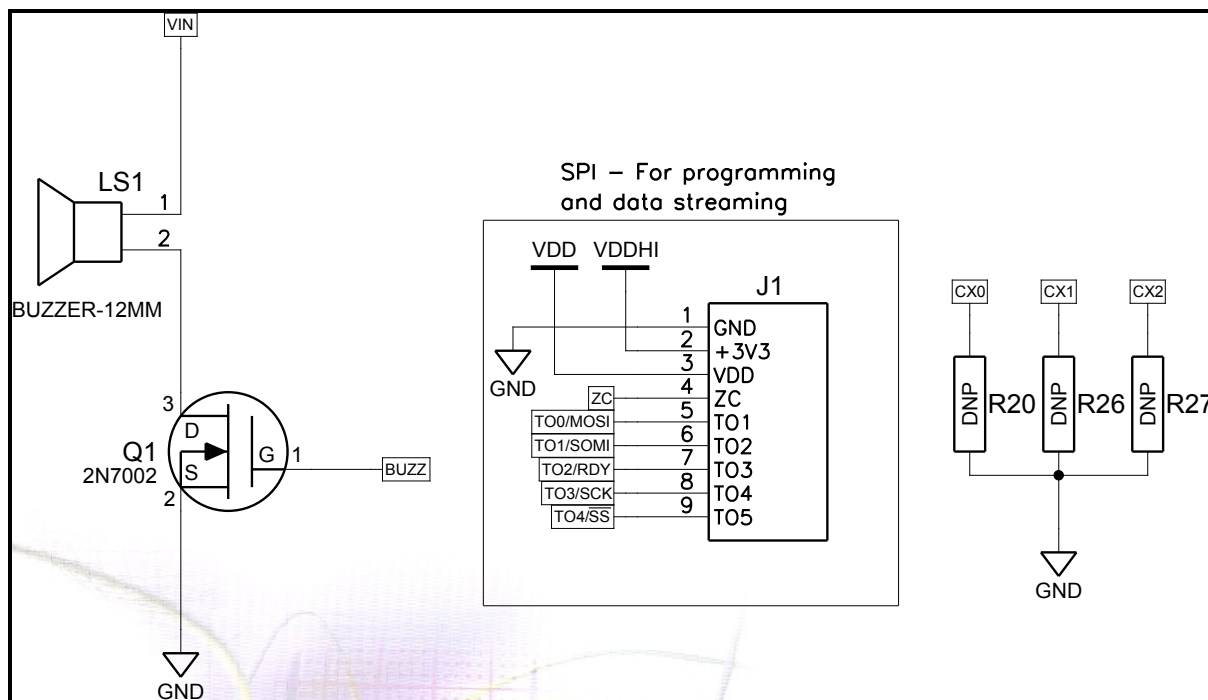


Figure 6: Optional: Buzzer, SPI Header and resistors to disable channels.

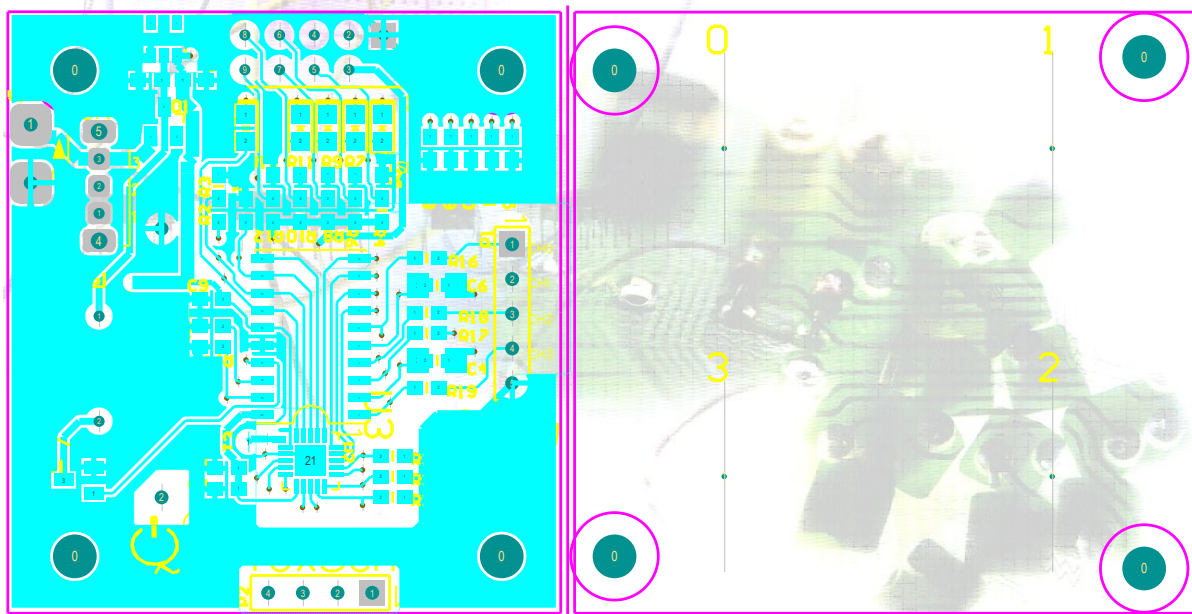


Figure 7: Top layer component placement

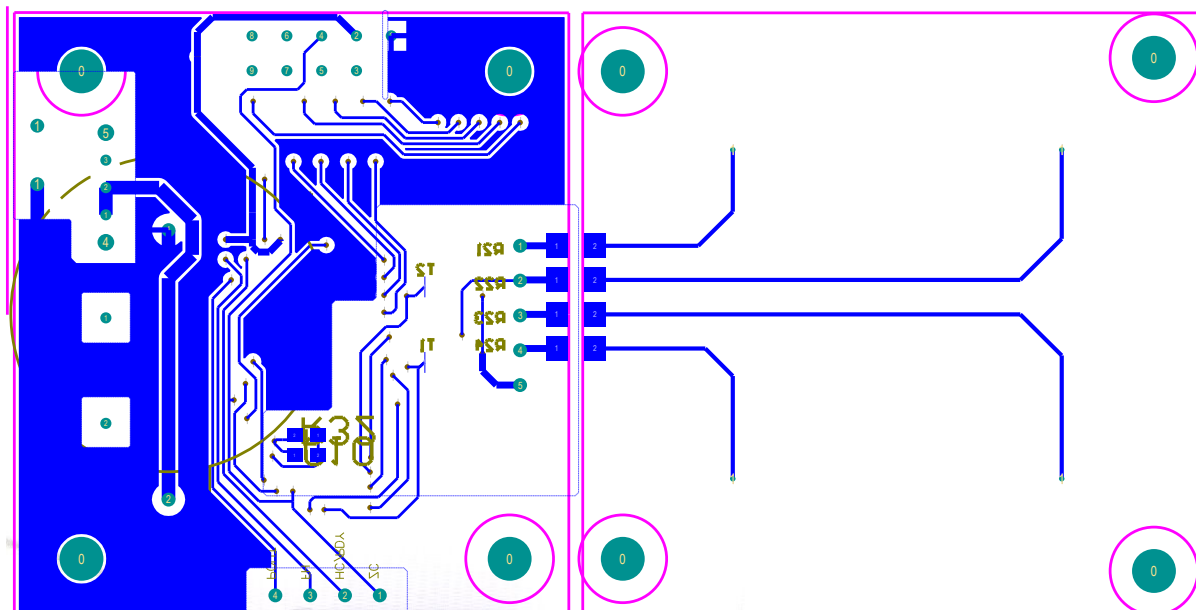


Figure 8: Bottom layer component placement

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