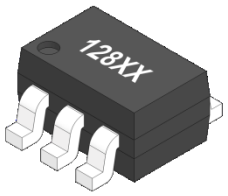
IQS128 / IQS128L Datasheet

IQ Switch® - ProxSense® Series

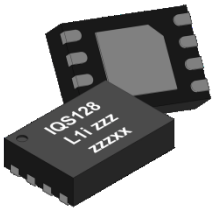
Single Channel Capacitive Proximity/Touch Controller

The IQS128 / IQS128L ProxSense® IC is a fully integrated capacitive sensor implementing Dynamic Calibration (DYCAL™) technology: intelligent hysteresis to allow for sensor drift even during sensor activation.

IQS128 TSOT23-6



IQS128L DFN8 (2x3)



RoHS compliant

Features

- DYCAL™ : Intelligent Hysteresis
- **I**nternal **C**apacitor **I**mplementation (ICI) – reference capacitor on-chip
- **A**utomatic **T**uning **I**mplementation (ATI) - Automatic adjustment for optimal sensor performance
- Supply voltage: 2.95V to 5.5V
- Minimum external components
- 1-Wire open drain data streaming option
- Advanced on-chip digital signal processing
- User selectable (OTP):
  - External synchronisation control or
  - External control over filter operation
  - I/O Sink or Source selection
  - Time-out for stuck key
  - Proximity and Touch sensitivity selections
  - IQS128L: Low Power options available

Keys:	Touch:	5mm x 5mm or larger (overlay thickness dependent)
	Proximity:	Various electrical options (wire / PCB trace / ITO / conductive foil)
Dielectric:	Material:	Various non-metal materials (i.e. glass, plastic, painted surfaces)
	Thickness:	6 mm plastic, 10 mm glass for touch. Very thick overlay possible for proximity

Applications

- Occupancy sensors
- SAR qualification for Tablet PC's
- On-ear detection for mobile phones
- 3D glasses
- Personal Media Players
- White goods and appliances
- Human Interface Devices
- Proximity activated backlighting
- Any applications where a touch and proximity condition can prevail for an extended period of time with or without a host controller

Advantages

- Allows for sensor drift in periods of activation and non-activation
- Improved digital filtering to reduce external noise
- Minimal power consumption (<7µA) when in standby mode (Charge Halt).

Available Options

T_A	TSOT23-6	DFN8 (2x3)
-40°C to 85°C	IQS128	IQS128L

Contents

1 Overview

1.1 Device variations

Device	Package	Functionality								
		DYCAL			LP modes	RF Noise Detection	Pulse on CTRL (Input)	DYCAL Output	ATI Base	Touch Debounce
		Release Threshold	Filter operation	Block ATI						
IQS128	TSOT23-6	75%	Normal	-	-	Available	Reseed	TOUT	4 values	3
IQS128L	DFN8(2x3)	75% & 87.5%	Updated	3sec after exiting TM	4 Power Modes	-	Re-ATI	POUT or TOUT	8 values	2

Please note: Except for the functional variations stated above, there also exist differences between the proximity and touch thresholds for the IQS128L version. More on this in Sections 6.4 & 6.5.

1.2 Device

The IQS128 and IQS128L ICs will be referred to as IQS128/IQS128L throughout the datasheet, unless they have different functionality, where it will be explicitly stated and explained.

The IQS128/IQS128L is a single channel capacitive proximity and touch device which employs an internal voltage regulator and reference capacitor (Cs).

The IQS128/IQS128L device has a dedicated pin for the connection of a sense electrode (Cx) and output pin for proximity and touch events on OUT. The polarity of the output pins can be configured. A 1-wire open drain data streaming protocol is implemented for debugging purposes.

Special device configuration can be done by setting one time programmable (OTP) options.

The device automatically tracks slow varying environmental changes via various signal processing algorithms and has an Automatic Tuning Implementation (ATI) algorithm to calibrate the device to the sense electrode.

DYCAL™ (Dynamic Calibration) is a special form of hysteresis that can track slow varying environmental change even while the sensor is in a touch state.

The *charge transfer* method of capacitive sensing is employed on the IQS128/IQS128L. (The charge transfer principle is thoroughly described in the application note: “AZD004 - Azoteq Capacitive Sensing”.)

1.3 Operation

The device has been designed to be used in applications where proximity is required and touch conditions can prevail for an extended period of time which may result in uncompensated drift in conventional capacitive sensors.

A low threshold is used to detect the proximity of an object, with a higher threshold for touch detection.

Dynamic Calibration is performed when a TOUCH condition is detected for longer than $T_{DYNACAL}$. The hysteresis algorithm will now check for the release condition of the touch, while still tracking environmental changes

1.4 Applicability

All specifications, except where specifically mentioned otherwise, provided by this datasheet are applicable to the following ranges:

- Temperature:-40C to +85C
- Supply voltage (V_{DDHI}): 2.95V to 5.5V

2 Pin-Out

The IQS128 is available in a TSOT23-6 package and the IQS128L is available in a DFN8(2x3) package.

2.1 IQS128

2.1.1 Pin-out

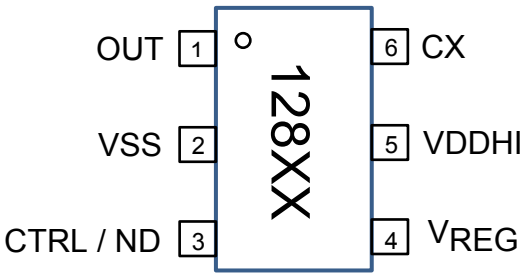
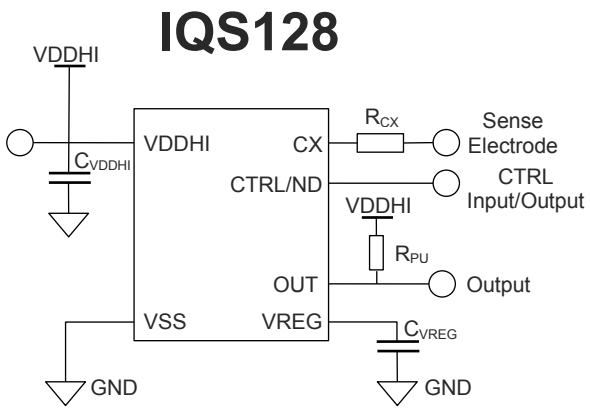


Figure 2.1 Pin-out of IQS128 package

Table 2.1 Pin-out description

IQS128			
Pin	**Name**	**Type**	**Function**
1	OUT	Digital Out	Output
2	VSS	Ground	GND Reference
3	CTRL / ND	Digital Input/Output	Control input or proximity output / ND pin
4	VREG	Analogue Output	Internal Regulator Pin (Connect 1µF bypass capacitor)
5	VDDHI	Supply Input	Supply Voltage Input
6	CX	Analogue	Sense Electrode

2.1.2 Schematic



Note: A 100pF capacitor can be places in parallel with the existing capacitors between VDDHI and GND as well as between VREG and GND for added RF immunity.

Figure 2.2 Typical application schematic of IQS128

2.1.3 Typical values

Component	Value
C_{VREG}	1uF
R_{CX}	470 Ω (typical)
R_{PU}*	4.7 kΩ (typical)
C_{VDDHI}	1uF

* R_{PU} is only needed if device is setup in active Low state.

2.2 IQS128L

2.2.1 Pin-out

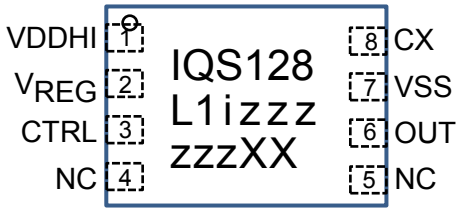


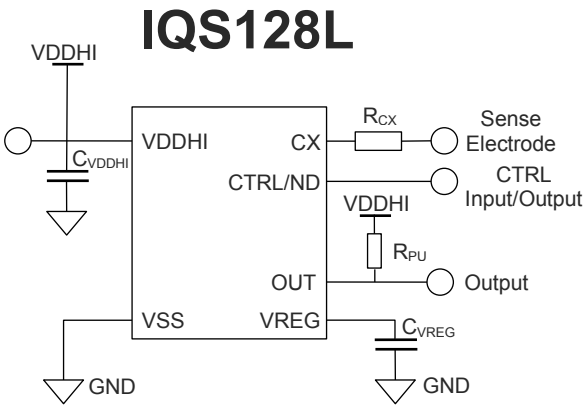
Figure 2.3 Pin-out of IQS128L package

Table 2.2 Pin-out description

IQS128L			
Pin	**Name**	**Type**	**Function**
1	VDDHI	Supply Input	Supply Voltage Input
2	VREG	Analogue Output	Internal Regulator Pin (Connect 1µF bypass capacitor)
3	CTRL	Digital Input/Output	Control input or proximity output
4	NC	-	No Connect
5	NC	-	No Connect
6	OUT	Digital Out	Output
7	VSS	Ground	GND Reference
8	CX	Analogue	Sense Electrode

2.2.2 Schematic

Figure 2.4 Typical application schematic of IQS128L



Note: A 100pF capacitor can be places in parallel with the existing capacitors between VDDHI and GND as well as between VREG and GND for added RF immunity.

2.2.1 Typical values

Component	Value
C_{VREG}	1uF
R_{CX}	470 Ω (typical)
R_{PU}	4.7 kΩ (typical)
C_{VDDHI}	1uF

* R_{PU} is only needed if device is setup in active Low state.

3 User Configurable Options

Table 4.1 and Table 4.2 list the user configurable settings.

The device is fully functional in its default state, but some applications may require alternative configuration settings. These settings are enabled by configuring One Time Programmable (OTP) user options.

Configuration can be done on packaged devices or in-circuit. In-circuit configuration may be limited by values of external components chosen.

Popular configurations are available ex-stock – please check with the local distributor for availability. Azoteq can supply pre-configured devices for large quantities.

3.1 Configuring Devices

Azoteq offers a Configuration Tool (CTxxx) and accompanying software (USBProg.exe) that can be used to program the OTP user options for prototyping purposes. More details regarding the configuration of the device with the USBProg program is explained by application note: "AZD007 – USBProg Overview" which can be found on the Azoteq website.

Alternative programming solutions for the IQS128/IQS128L also exist. For further enquiries regarding this, please contact Azoteq at ProxSenseSupport@azoteq.com or the local distributor.

3.1.1 IQS128 User Selectable Options

Table 3-1: IQS128 Bank 0 User Selectable Options

Bit	7	6	5	4	3	2	1	0
Name	T_{THR2}	T_{THR1}	T_{THR0}	P_{THR1}	P_{THR0}	ND	LOGIC	EXT_CTRL
Default	0	0	0	0	0	0	0	0

bit 7-5 — **T_{THR}<2:0>:** Touch Thresholds (counts) — -Section 6.5
000 = 16
001 = 40
010 = 60
011 = 90
100 = 130
101 = 200
110 = 340
111 = 500

bit 4-3 — **P_{THR}<1:0>:** Proximity Thresholds (counts) — -Section 0
00 = 4
01 = 8
10 = 12
11 = 16

bit 2 — **ND:** RF Noise Detection — -Section 6.3.1
0 = Disable RF Noise Detect
1 = Enable RF Noise Detect

bit 1 — **LOGIC:** Output logic select (Only when STREAMING mode is disabled) — -Section 6.7
0 = [1]Software Open Drain Active Low
1 = Active High

bit 0 — **EXT_CTRL:** Selects external control option on OUT — -Section 6.1
0 = Charge Halt
1 = Halt LTA filter

[1] Only applicable for OUT pin. If CTRL is configured as output, it is a push-pull output.

Table 3-2: IQS128 Bank 1 User Selectable Options

Bit	7	6	5	4	3	2	1	0
Name	STREAMING	~	~	T_{HALT1}	T_{HALT0}	~	~	CTRL_DIRECTION
Default	0	0	0	0	0	0	0	0

bit 7 **STREAMING**: 1-wire streaming protocol -Section 0
0 = Disabled
1 = Enabled

bit 6-5 **Unimplemented**

bit 4-3 **T_{THALT}<1:0>:** Filter Halt Settings -Section 6.7
00 = Always
01 = 18s
10 = 60s
11 = 3s

bit 2-1 **Unimplemented**

bit 0 **CTRL_DIRECTION:** Configures Control pin as input or output
0 = Input for external control from MCU (used with Bank0-bit 0) -Section 0
1 = Output Mode Operation

Table 3-3: IQS128 Bank 2 User Selectable Options

Bit	7	6	5	4	3	2	1	0
Name	~	~	~	~	~	ATI_{BASE1}	ATI_{BASE0}	~
Default	~	~	~	~	~	0	0	~

bit 7-4 **Unimplemented**

bit 2-1 **ATI_{BASE}<1:0>:** Base value selections -Section 8.1
00 = 200 counts
01 = 100 counts
10 = 150 counts
11 = 250 counts

bit 0 **Unimplemented**

3.1.2 IQS128L User Selectable Options

Table 3-4: IQS128L Bank 0 User Selectable Options

Bit	7	6	5	4	3	2	1	0
Name	T_{THR2}	T_{THR1}	T_{THR0}	P_{THR1}	P_{THR0}	ND	LOGIC	EXT_CTRL
Default	0	0	0	0	0	0	0	0

bit 7-5 **T_{THR}<2:0>:** Touch Thresholds (counts) -Section 6.5
000 = 40
001 = 60
010 = 100
011 = 200
100 = 360
101 = 500
110 = 700
111 = 900

bit 4-3 **P_{THR}<1:0>:** Proximity Thresholds (counts) -Section 0
00 = 4
01 = 8
10 = 16
11 = 32

bit 2 **Unimplemented**

bit 1 **LOGIC:** Output logic select (Only when STREAMING mode is disabled) -Section 6.7
0 = [2]Software Open Drain Active Low
1 = Active High

bit 0 **EXT_CTRL:** Selects external control option on OUT -Section 6.1
0 = Charge Halt
1 = Halt LTA filter

[2] Only applicable for OUT pin. If CTRL is configured as output, it is a push-pull output.

Table 3-5: IQS128L Bank 1 User Selectable Options

Bit	7	6	5	4	3	2	1	0
Name	STREAMING	LP1	LP0	T_{HALT1}	T_{HALT0}	~	~	CTRL_DIRECTION
Default	0	0	0	0	0	0	0	0

bit 7 **STREAMING**: 1-wire streaming protocol -Section 0
0 = Disabled
1 = Enabled

bit 6-5 **LP<1:0>:** Low Power Mode timings -Section 6.8
00 = 9.01ms (Boost Power Mode)
01 = 27ms (Normal Power Mode)
10 = 100ms (Low Power Mode 1)
11 = 300ms (Low Power Mode 2)

bit 4-3 **T_{HALT}<1:0>:** Filter Halt Settings -Section 6.7
00 = Always
01 = 18s
10 = 60s
11 = 3s

bit 2-1 **Unimplemented**

bit 0 **CTRL_DIRECTION:** Configures Control pin as input or output -Section 0
0 = Input for external control from MCU (used with Bank0-bit 0)
1 = Output Mode Operation

Table 3-6: IQS128L Bank 2 User Selectable Options

Bit	7	6	5	4	3	2	1	0
Name	~	~	DYCAL_OUTPUT	RELEASE_THRES	ATI_{BASE2}	ATI_{BASE1}	ATI_{BASE0}	~
Default	~	~	0		0	0	0	~

bit 7-6 **Unimplemented**

Bit5 **DYCAL_OUTPUT:** OUT pin will react with the detection of a -Section 9.2
0 = Proximity
1 = Touch

bit4 **RELEASE_THRES:** Release Threshold - DYCAL (% of Touch Threshold) -Section 9.1
0 = 75%
1 = 87.5%

bit 3-1 **ATI_{BASE}<3:0>:** Base value selections -Section 8.1
000 = 200 counts
001 = 250 counts
010 = 300 counts
011 = 350 counts
100 = 400 counts
101 = 550 counts
110 = 700 counts
111 = 850 counts

bit 0 **Unimplemented**

4 Measuring capacitance using the *Charge Transfer* method

The *charge transfer* method of capacitive sensing is employed on the IQS128/IQS128L. (The charge transfer principle is thoroughly described in the application note: "AZD004 - Azoteq Capacitive Sensing".)

A charge cycle is used to take a measurement of the capacitance of the sense electrode (connected to Cx) relative to ground. It consists of a series of pulses charging Cx and discharging Cx to the reference capacitor, at the charge transfer frequency (FCX - refer to Section 10). The number of the pulses required to reach a trip voltage on the reference capacitor is referred to as **counts (CS)** which is the instantaneous capacitive measurement. The CS value is used to determine if either a physical contact or a proximity event has occurred based on the change in CS detected. The typical values of CS, without a touch or a proximity condition range between 1344 and 1865, although higher and lower CS can be used based on the application requirements. With CS larger than +/-1865 the gain of the system may become too high causing unsteady CS.

The IQS128/IQS128L schedules a charge cycle every t_{SAMPLE} seconds to ensure regular samples for processing of results. The duration of the charge cycle is defined as t_{CHARGE} and varies according to the CS required to reach the trip voltage. Other activities, such as data streaming (if device is in streaming mode), are completed between charge cycles.

Please note: Attaching a probe to the Cx pin will increase the capacitance of the electrode and therefore the CS. This may have an immediate influence on the CS (decrease t_{CHARGE} – thus CS) and cause a proximity or a touch event. After t_{HALT} seconds the system will adjust to accommodate for this change. If the total load on Cx, with the probe attached is still lower than the maximum Cx load the system will continue to function normally after t_{HALT} seconds with the probe attached.

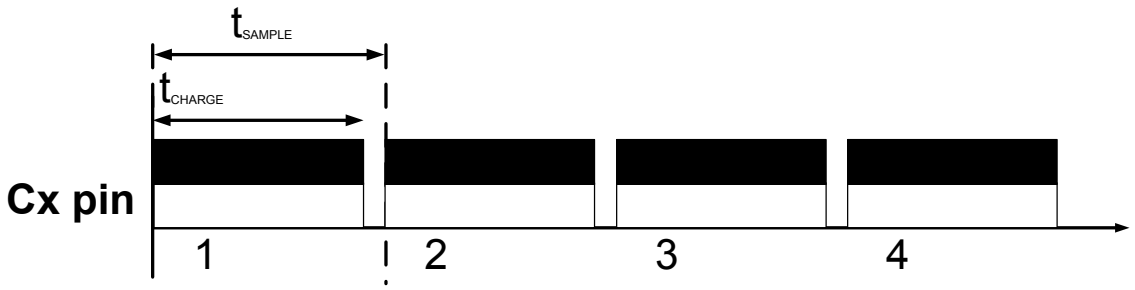


Figure 4.1 Charge cycles as can be see on CX

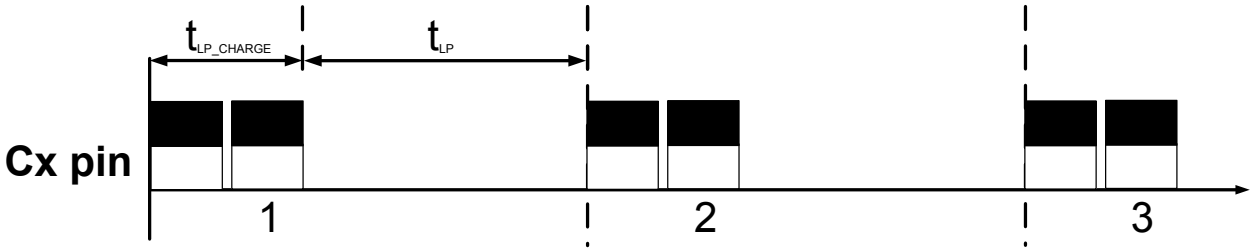


Figure 4.2 Charge cycles as charged in LP modes (IQS128L only)

5 DYCAL™

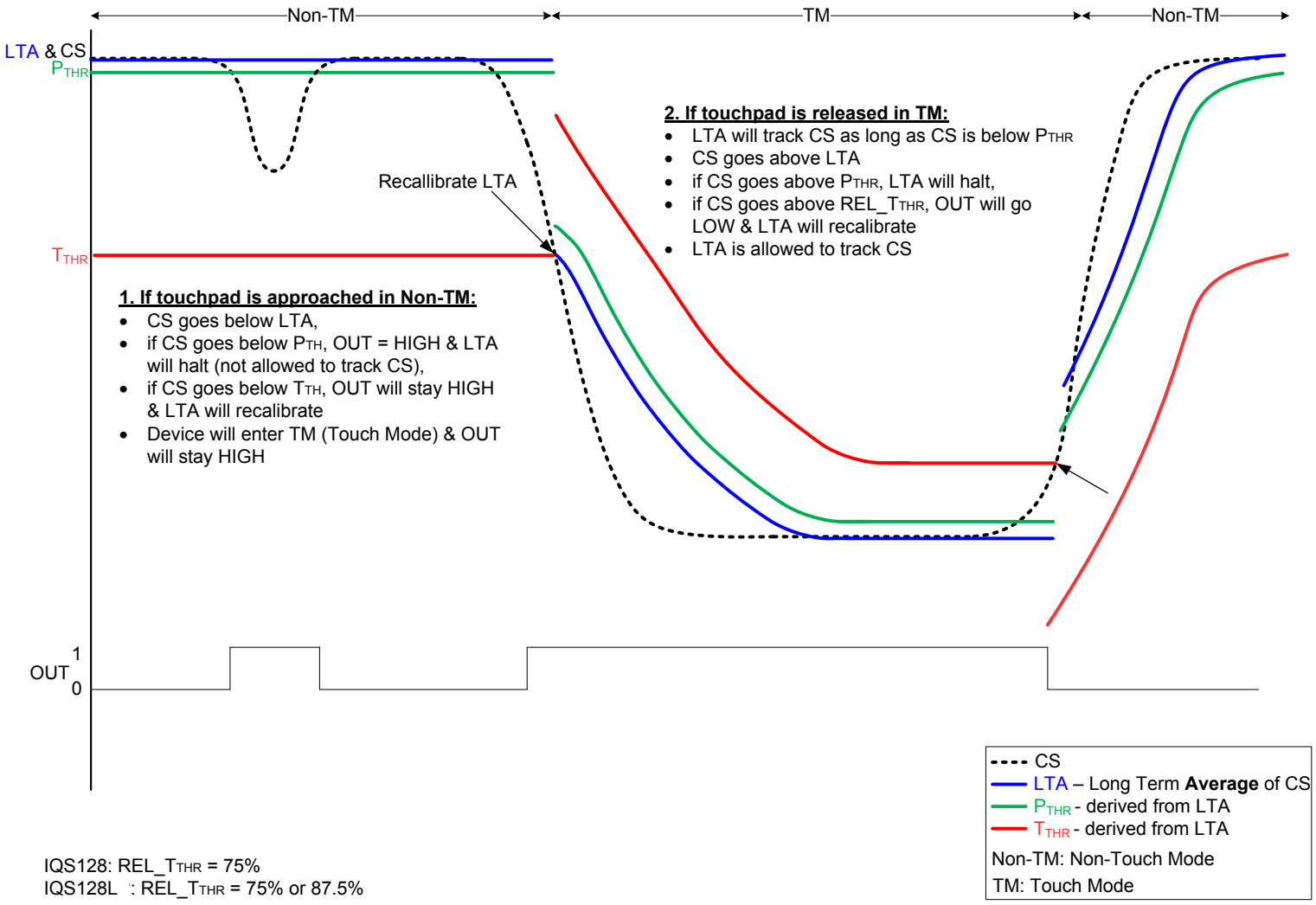


Figure 5.1 DYCAL Operation

5.1 Operating Principle

Figure 5.1 is a visual representation of the DYCAL functionality. The OUT pin is used to indicate the status of a DYCAL event (both a proximity and a touch event). The DYCAL functionality is summarised below.

5.2 Non-Touch Mode

The OUT pin is activated on the successful detection of a proximity event and will remain activated for the duration of the proximity event, permitting that this event is not longer than the filter halt timings. The LTA will be halted in this time.

As soon as a touch condition is detected (CS below T_{THR}), the controller will dynamically re-calibrate its LTA to the halted LTA – T_{THR}. The IC is now in Touch Mode.

5.3 Touch Mode

After the re-calibration of the LTA, it will follow the CS and be allowed to track slow varying environmental changes. If the CS were to exceed the LTA by a release threshold (REL_T_{THR}) the touch detection will stop and the OUT pin will return to its original state.

6 Configurable Settings

This section describes the user configurable options of the IQS128/IQS128L in more detail.

User programmable options are selected by configuring the OTP selections. Please refer to section 3 for an overview of the configurable settings.

6.1 EXT_CTRL: External Control

The user has the option to control some parameters of the IQS128/IQS128L from an external source. The IC can be used in default mode (CTRL unconnected) or the user can use the CTRL pin to select whether the master should halt the charge transfers (i.e. stop operation) or to halt LTA filter tracking on the IQS128/IQS128L.

6.1.1 Charge Halt

If CTRL is sampled high for longer than $T_{EXT\_HALT,}$ the charge conversion cycle will be halted, once the current conversion has been completed. The device will remain in this standby mode until the CTRL line is sampled low again. An automatic reseed is performed directly after CTRL is released to compensate for any environmental changes which might have occurred during the standby mode.

6.1.2 Halt LTA filter

When configured in this mode, CTRL can be used to control the LTA halt times when sampled high. The CTRL pin has precedence over the configurations bits selected for the halt timings.

If CTRL is sampled high for longer than T_{EXT_HALT}, the filter will be halted until this pin is sampled low.

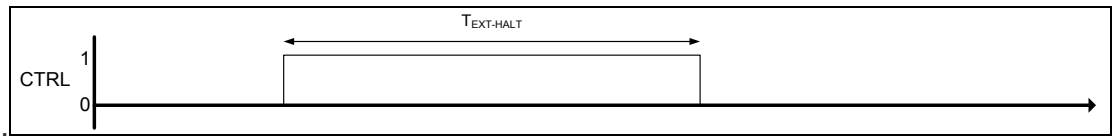


Figure 6.1 Master Output signal on CTRL pin to Halt Operation or Filter Halt

6.1.3 Pulse on CTRL:

The pulse on the CTRL pin needs to adhere to the following timing constraints:

$25ms < T_{PULSE} < 35ms$

6.1.3.1 IQS128: Reseed

A reseed condition can be initiated by generating a pulse on the CTRL pin. The LTA will be reset to the CS, forcing the OUT pin to its original state.

If the CS value is outside its allowable limits, the device will force an ATI event to reset the system sensitivity. (Please refer to section 8 for more detail).

6.1.3.2 IQS128L: re-ATI

A re-ATI condition can be initiated by generating a pulse on the CTRL pin. This function can be issued at any time.

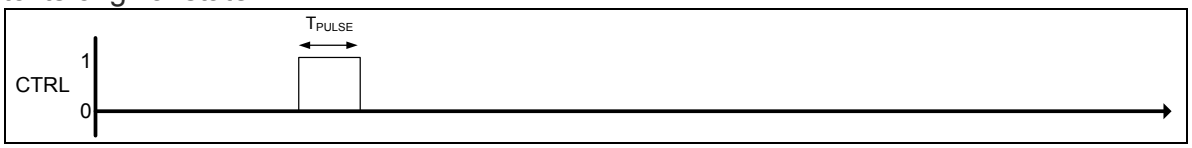


Figure 6.2 Master Output signal on CTRL to force a Reseed Condition

6.2 LOGIC

The logic used by the device can be selected as active HIGH or active LOW. The output pins OUT and CTRL will function based on this selection.

Configuration: Bank0 bit1: Logic Output Selection

Bit	Selection
0	Software Open Drain Active Low
1	Active High

A software open drain output is implemented for the OUT pin when configured in active low mode. The voltage on the pull-up resistor is limited to the IQS128/IQS128L supply voltage. A 4k7-10kΩ resistor between OUT and VDDHI is recommended.

6.3 RF Noise on IQS128/IQS128L

6.3.1 ND: RF Noise Detection (IQS128)

The IQS128 has RF Noise Detect (ND) functionality. (This option is not available on the IQS128L.) If ND function is enabled, the IQS128 is able to detect RF Noise on the CTRL / ND pin. Further details on the working of this can be found in the Application Notes: AZD015 and AZD015b.

6.3.2 IQS128/IQS128L RF Noise Immunity

The IQS128/IQS128L has advanced immunity to RF noise sources such as GSM cellular telephones, DECT, Bluetooth and WIFI devices. Design guidelines should however be followed to ensure the best noise immunity. The design of capacitive sensing applications can encompass a large range of situations but as a summary the following should be noted to improve a design:

- A ground plane should be placed under the IC, except under the Cx line.
- All the tracks on the PCB must be kept as short as possible.
- The capacitor between VDDHI and VSS as well as between VREG and VSS, must be placed as close as possible to the IC.
- A 100 pF capacitor should be placed in parallel with the 1uF capacitor between VDDHI and VSS. Another 100 pF capacitor can be placed in parallel with the 1uF capacitor between VREF and VSS.
- If the device is too sensitive for a specific application a parasitic capacitor (max 5pF) can be added between the Cx line and ground.
- Proper sense electrode and button design principles must be followed.
- Unintentional coupling of sense electrode to ground and other circuitry must be limited by increasing the distance to these sources.
- In some instances a ground plane some distance from the device and sense electrode may provide significant shielding from undesired interference.

When the capacitance between the sense electrode and ground becomes too large the sensitivity of the device may be influenced.

6.4 $P_{THR[1:0]}$ Proximity Threshold

The IQS128/IQS128L has 4 proximity threshold settings indicated in CS. The proximity threshold is selected by the designer to obtain the desired sensitivity and noise immunity. A proximity event is triggered if the CS diverges more than the selected count from the LTA for 6 consecutive cycles.

IQS128

Configuration: Bank0 bit 4-3

P_{TH1}:P_{TH0}:Proximity Thresholds

Bit	Selection	
00	4	(Most sensitive)
01	8	
10	12	
11	16	(Least sensitive)

IQS128L

Configuration: Bank0 bit 4-3

P_{THR1}:P_{THR0}:Proximity Thresholds

Bit	Selection	
00	4	(Most sensitive)
01	8	
10	16	
11	32	(Least sensitive)

6.5 $T_{THR[2:0]}$ Touch Threshold

The IQS128/IQS128L has 8 touch threshold settings indicated in CS. The touch threshold is selected by the designer to obtain the desired touch sensitivity. A touch event is triggered if the CS diverges more than the selected count from the LTA for 2 consecutive cycles.

In the NO-TOUCH state the CS must diverge more than the touch threshold value below the LTA. Operating in the TOUCH STATE, the CS must diverge more than REL_T_{THR} of the touch threshold value above the LTA.

The following equation is used to determine if a touch or release event occurred.

NO TOUCH STATE: LTA – CS <= T_{THR}

TOUCH STATE: CS - LTA >= REL_T_{THR}

IQS128

Configuration: Bank0 bit 7-5 T_{THR2}:T_{THR0} Touch Thresholds

Bit	Selection	
000	16	(Most sensitive)
001	40	
010	60	
011	90	
100	130	
101	200	
110	340	
111	500	(Least sensitive)

IQS128L

Configuration: Bank0 bit 7-5 T_{THR2}:T_{THR0} Touch Thresholds

Bit	Selection	
000	40	(Most sensitive)
001	60	
010	100	
011	200	
100	360	
101	500	
110	700	
111	900	(Least sensitive)

6.6 CTRL_DIRECTION

The CTRL pin can be configured as an input (default) or as an output. If configured as input, the IC has an internal pull-up resistor enabled. See Section 6.1 for more information on functionality of CTRL as input.

If the CTRL pin is configured as an output it, cannot be used to control the filter or charge transfer operation.

The CTRL pin is activated upon the successful detection of a proximity condition. The pin will remain activated for the duration of the proximity detection as indicated in figure 7.3. If a proximity condition is detected in conjunction with a touch event, the pin will only be de-activated when the touch condition is no longer detected as indicated in figure below.

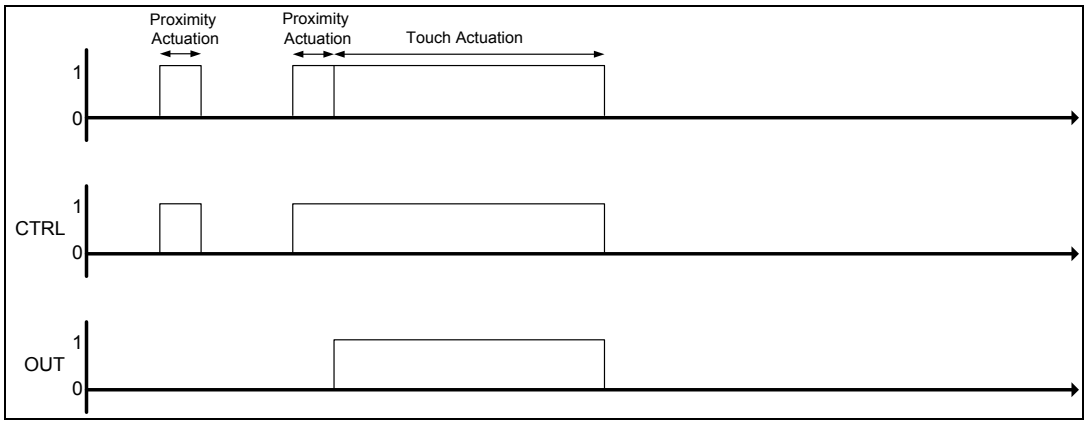


Figure 6.3 Proximity and Touch output

6.7 $T_{HALT[1:0]}$ Filter Halt

The LTA filter only executes while no proximity events are detected to ensure compensation only for environmental changes. Once a touch event is detected the filter will resume operation and will on longer be halted. The halt timing configuration settings determine how long the filter is halted.

Configuration: Bank1 bit 4-3 T_{HALT1}:T_{HALT0} LTA Halt timings for proximity events

Bit	Selection
00	ALWAYS
01	18 seconds
10	60 seconds
11	3 seconds

The presence of a proximity condition for a time exceeding the halt time will be deemed as a fault state which would trigger a reseed event where after the output state on the OUT pin will be reset to its original condition.

6.8 $LP_{[1:0]}$ Low Power Modes (IQS128L)

There exist 4 LP modes. The LP modes will decrease the sampling frequency of CS which will reduce the power consumption of the device. However, this will also increase the response time of the device.

Configuration: Bank1 bit 6-5 LP_1:LP_0 Low Power Modes

Bit	Selection
00	9.1ms (Boost Power Mode)
01	100ms (Normal Power Mode)
10	200ms (Low Power Mode 1)
11	300ms (Low Power Mode 2)

7 Streaming Mode

For a more complete description of the data streaming protocol, please refer to Application Note AZD017 on the Azoteq website.

The IQS128/IQS128L has the capability to stream data to a MCU. This provides the designer the ability to obtain the parameters and sensor data within the device in order to aid design into applications. Data streaming is performed as a 1-wire data protocol on the OUT pin. The output function of this pin is therefore lost when the device is configured in streaming mode. Data Streaming can be enabled as indicated below:

Configuration: Bank1 bit7: Streaming Mode

Bit	Selection
0	Disabled
1	Enabled

Figure 7.1 illustrates the communication protocol for initialising and sending data with the 1 wire communication protocol.

1. Communications initiated by a START bit. Bit defined as a low condition for T_{START}.
2. Following the START bit, is a synchronisation byte (T_{INIT} = 0xAA). This byte is used by the MCU for clock synchronisation.
3. Following T_{INIT} the data bytes will be sent. With short data streaming mode enabled, 5 bytes of data will be sent, otherwise 8 bytes will be sent after each charge cycle.
4. Each byte sent will be preceded by a START bit and a STOP bit will follow every byte.
5. STOP bit indicated by taking pin 1 high. The STOP bit does not have a defined period.

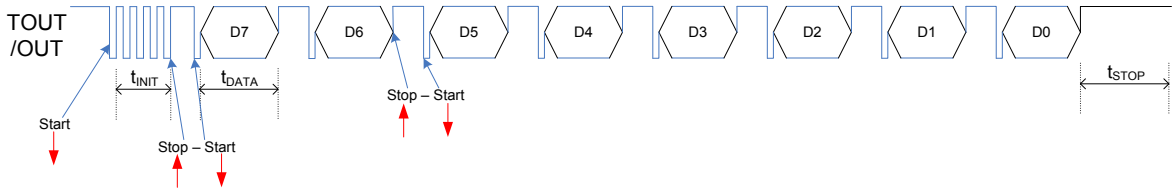


Figure 7.1 Debug: 1-wire streaming Debug Mode

The following table defines the bit definitions for the IQS128/IQS128L devices during Streaming Mode.

Byte Definitions for Streaming Mode

Byte	Bit	Value
0	7:0	CS High byte
1	15:8	CS Low byte
2	23:16	LTA High byte
3	31:24	LTA Low byte
4	39 38 37 36 35 34 33 32	ATI busy Proximity Event Detected Touch Event Dectected OUT State Indication *Not Used* Zoom active Not Used Not Used
5	47 46 45 44 43 42 41 40	ATI Multiplier (I) ATI Multiplier (S) ATI Multiplier (S) Compensation (P4) Compensation (P3) Compensation (P2) Compensation (P1) Compensation (P0)
6	55:54 53 52 51 50 49 48	*Not Used* Compensation (P5) Touch Threshold Bit 2 Touch Threshold Bit 1 Touch Threshold Bit 0 Proximity Threshold Bit 1 Proximity Threshold Bit 0
7	63:56	Counter

Azoteq provides a GUI (Graphical User Interface) application that can be utilised to capture and visualise the data streamed from the IQS128/IQS128L.

8 Automatic Tuning Implementation (ATI)

ATI is a sophisticated technology implemented in the latest generation ProxSense® devices that optimises the performance of the sensor in a wide range of applications and environmental conditions (refer to application note AZD0027 - Automatic Tuning Implementation).

ATI makes adjustments through external reference capacitors unnecessary (as required by most other solutions) to obtain optimum performance.

8.1 ATI

The IQS128/IQS128L implements an ATI algorithm. This algorithm adjusts the ATI parameters to optimise the sensing electrode's connection to the device.

The device will execute the ATI algorithm whenever the device starts-up and or when the CS are not within a predetermined range.

There are 2 important definitions to understand for ATI:

8.1.1 ATI Target

ATI adjusts internal circuitry according to two parameters, the **ATI multiplier** and the **ATI compensation**.

- The **ATI multiplier** can be viewed as a course adjustment of CS, used to achieve the ATI BASE value.
- The **ATI compensation** is a fine adjustment used to reach the ATI TARGET value.

With these two parameters the CS of the IQS128/IQS128L is tuned until an ATI target value of 1600 is achieved.

8.1.2 ATI_{BASE}: Significance of ATI Base

As mentioned above, the **ATI multiplier** is used to select a base value for the ATI. The ATI BASE value is important, as this determines the sensitivity of the device. The sensitivity can be defined as:

Sensitivity = ATI TARGET / ATI BASE

The ATI Target remains fixed at 1600 and it can thus be seen from this that a larger base value will result in a less sensitive device. The designer has the option to increase/reduce the sensitivity of the system through the ATI BASE value. For most applications the ATI BASE should be kept default.

The options for the ATI BASE is as follows:

IQS128

Configuration: Bank2 bit 2-1
ATI_{BASE1}:ATI_{BASE0} ATI BASE values

Bit	Selection	
00	200	(Most sensitive)
01	100	
10	150	
11	250	(Least sensitive)

IQS128L

Configuration: Bank2 bit 3-1
ATI_{BASE2}:ATI_{BASE0} ATI BASE values

Bit	Selection	
000	200	(Most sensitive)
001	250	
010	300	
011	350	
100	400	
101	550	
110	700	
111	850	(Least sensitive)

8.2 Sensitivity due to ATI

The adjustment of the ATI parameters will result in variations in the CS and sensitivity. Sensitivity can be observed as the change in CS as the result of a fixed change in sensed capacitance. The ATI parameters have been chosen to provide significant overlap. It may therefore be possible to select various combinations of ATI multiplier and ATI compensation settings to obtain the same CS. The sensitivity of the various options may however be different for the same CS.

8.3 ATI Procedure

While the ATI algorithm is in progress this condition will be indicated in the streaming data and proximity and touch events cannot be detected. The device will only briefly remain in this condition and it will be entered only when relatively large shifts in the CS has been detected.

The ATI function aims to maintain a constant CS, regardless of the capacitance of the sense electrode (within the maximum range of the device).

The effects of ATI on the application are the following:

- Automatic adjustment of the device configuration and processing parameters for a wide range of PCB and application designs to maintain a optimal configuration for proximity and touch detection.
- Automatic tuning of the sense electrode at start-up to optimise the sensitivity of the application.
- Automatic re-tuning when the device detects changes in the sensing electrode's capacitance to accommodate a large range of changes in the environment of the application that influences the sensing electrode.
- Re-tuning only occurs during device operation when a relatively large sensitivity reduction is detected. This is to ensure smooth operation of the device during operation.
- Re-tuning may temporarily influences the normal functioning of the device, but in most instances the effect will be hardly noticeable.
- Shortly after the completion of the re-tuning process the sensitivity of a Proximity detection may be reduced slightly for a few seconds as internal filters stabilises.

ATI can be implemented so effectively due to:

- Excellent system signal to noise ratio (SNR).
- Effective digital signal processing to remove AC and other noise.
- The very stable core of the devices.
- The built-in capability to accommodate a large range of sensing electrode capacitances.

9 DYCAL Specific settings

9.1 REL_T_{THR}: Release Threshold (IQS128L)

The IQS128L has the option to increase the release threshold when in TM. This helps that small variations caused by moving a finger/hand on a touch pad will not cause the IC to exit TM, making the solution more robust. The options available are shown below:

Configuration: Bank2 bit4: REL_T_{THR}

Bit	Selection
0	75%
1	87.5%

9.2 DYCAL_OUTPUT (IQS128L)

The IQS128L can be configured to activate the OUT pin with either a proximity event or a touch event.

Choosing a proximity event, will make the activation of OUT more sensitive.

Using a touch event to activate OUT will make the system less sensitive which is needed in some applications. The LTA will still halt with the detection of a proximity but will not have an influence on the OUT pin. The LTA will still re-calibrate once a touch condition is detected.

Configuration: Bank2 bit5:DYCAL_OUTPUT

Bit	Selection
0	Proximity
1	Touch

10 Electrical Specifications

10.1 Absolute Maximum Specifications

Exceeding these maximum specifications may cause damage to the device.

Operating temperature	-40°C to 85°C
Supply Voltage (V_{DDHI} – V_{SS})[3]	6.5V
Maximum pin voltage (OUT, CTRL)	V_{DDHI} + 0.5V
Pin voltage (Cx)	2.5V
Minimum pin voltage (VDDHI, VREG, OUT, CTRL, Cx)	V_{SS} - 0.5V
Minimum power-on slope	100V/s
ESD protection (VDDHI, VREG, V_{SS}, OUT, CTRL, Cx)	4kV

10.2 General Characteristics (Measured at 25°C)

Standard IQS128/IQS128L devices are rated for supply voltages between 2.95V and 5.5V.

Table 10.1 IQS128/IQS128L General Operating Conditions

DESCRIPTION	Conditions	PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage		V_{DDHI}	2.95		5.50	V
Internal regulator output	2.95 ≤ V_{DDHI} ≤ 5.5	V_{REG}	2.35	2.50	2.65	V
Boost Power operating current	2.95 ≤ V_{DDHI} ≤ 5.5	I_{IQS128_BP}		77		µA
Standby operating current[4]	2.95 ≤ V_{DDHI} ≤ 5.5	$I_{STANDBY}$		7		µA
Normal Power operating current	2.95 ≤ V_{DDHI} ≤ 5.5	I_{IQS128_NP}		31		µA
Low power 1 operating current	2.95 ≤ V_{DDHI} ≤ 5.5	$I_{IQS128L\_LP1}$		17		µA
Low power 2 operating current	2.95 ≤ V_{DDHI} ≤ 5.5	$I_{IQS128L\_LP2}$		10.5		µA

Table 10.2 Start-up and shut-down slope Characteristics

DESCRIPTION	IC	Conditions	PARAMETER	MIN	MAX	UNIT
POR	D/S	V_{DDHI} Slope ≥ 100V/s	POR	1.45	1.70	V
BOD	D/S		BOD	1.30	1.40	V

[3] Maximum voltage applied for OTP programming and not intended for operation.

[4] CTRL = Input and CTRL = HIGH (Charge halt).

10.3 Output Characteristics (Measured at 25°C)

Table 10.3 OUT Characteristics

Symbol	Description	I_{SOURCE} (mA)	Conditions	MIN	TYP	MAX	UNIT
V_{OH}	Output High voltage	1	V_{DDHI} = 5.5V		TBD		V
		1	V_{DDHI} = 3.3V		TBD		
		1	V_{DDHI} = 2.95V		TBD		
Symbol	**Description**	**I_{SINK} (mA)**	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
V_{OL}	Output Low voltage	1	V_{DDHI} = 5.5V	0.30	TBD		V
		1	V_{DDHI} = 3.3V	0.20	TBD		
		1	V_{DDHI} = 2.95V	0.20	TBD		

10.4 Timing Characteristics

Table 10.4 Main Oscillator[5]

SYMBOL	DESCRIPTION	Conditions	MIN	TYP	MAX	UNIT
F_{OSC}	IQS128/IQS128L Main oscillator	$2.95 \leq V_{DDHI} \leq 5.5$	0.9	1	1.1	MHz

Table 10.5 IQS128L Response Times

Power Mode	Conditions	DYCAL		
		Min**	Max	Unit
Boost Power Mode[6]	Detection	27.3	-	ms
	Release	27.3	-	ms
Normal Power Mode[7]	Detection	111	-	ms
	Release	123	-	ms
Low Power Mode 1	Detection	301	-	ms
	Release	313	-	ms
Low Power Mode 2	Detection	821	-	ms
	Release	832	-	ms

**Minimum time calculated as a user touching and exceeding the T_{THR}. Touch debounce is 2 and I/O is toggled after next charge transfer cycle, requiring 3 charge cycles for the minimum time of a decision to be made.

[5] All timings are derived from the main oscillator.

[6] Minimum Detection and Release times = 3 x t_{CHARGE}

[7] $Detection_{MIN}$ = 3 x t_{LP_CHARGE} + 2 x $t_{LP(max)}$ (t_{LP_CHARGE} is dependent on counts) (counts is short)

$Release_{MIN}$ = 3 x t_{LP_CHARGE} + 2 x $t_{LP(max)}$ (t_{LP_CHARGE} is dependent on counts) (counts is longer)

Maximum time = Dependent on speed at which user approaches electrode

Table 10.6 General Timing Characteristics for 2.95V ≤ V_{DDHI} ≤ 5.5V

SYMBOL	DESCRIPTION	Conditions	MIN	TYP	MAX	UNIT
t_{HIGH}	Output high minimum time		9			ms
t_{LOW}	Output low minimum time		9			ms
F_{CX}	Charge transfer frequency			250		kHz
t_{CHARGE}	Charge cycle duration	CS = 1600, fcx = 250kHz		6.4		ms
t_{SAMPLE}	Refer to section 4					ms
t_{BP}	Sampling period in BP	t_{CHARGE} - 2 ≤ t_{SAMPLE}		9		ms
t_{BP}	Sampling period in BP	t_{CHARGE} ≥ t_{SAMPLE}		t_{CHARGE}+2		ms
t_{LP_CHARGE}	Low Power Charging time			CS*(1/F_{CX})+t_{CHARGE}		
t_{NP}	Low Power Time between charges for LP1. Refer to section 4		18.9	27	35.1	ms
t_{LP1}	Low Power Time between charges for LP1. Refer to section 4		70	100	130	ms
t_{LP2}	Low Power Time between charges for LP1. Refer to section 4		210	300	390	ms
t_{START}	Refer to section 0		14.4	17	18.8	us
t_{INIT}	Refer to section 0			136		us
t_{DATA}	Refer to section 0			136		us
$T_{DYNACAL}$	Dynamic Calibration time	2.95 ≤ V_{DDHI} ≤ 5.5		250		ms
T_{EXT_HALT}	Halt Operation/Filter Halt time	2.95 ≤ V_{DDHI} ≤ 5.5		40		ms
T_{PULSE}	Pulse timing	2.95 ≤ V_{DDHI} ≤ 5.5	25	30	35	ms

Table 10.7 IQS128 Response Times

Power Mode	Conditions	DYCAL		
		Min*	Max	Unit
Boost Power Mode[8]	Detection	63.7	-	ms
	Release	63.7	-	ms

**Minimum time calculated as causing a proximity detection on the IQS128. Prox debounce is 6 and I/O is toggled after next charge transfer cycle, requiring 7 charge cycles for the minimum time of a decision to be made.

[8] IQS128 only available in Boost Power Mode. Minimum Detection and Release times = 7 x t_{CHARGE}

11 Packaging and Part-number Information

11.1 Packaging Information

11.1.1 TSOT23-6

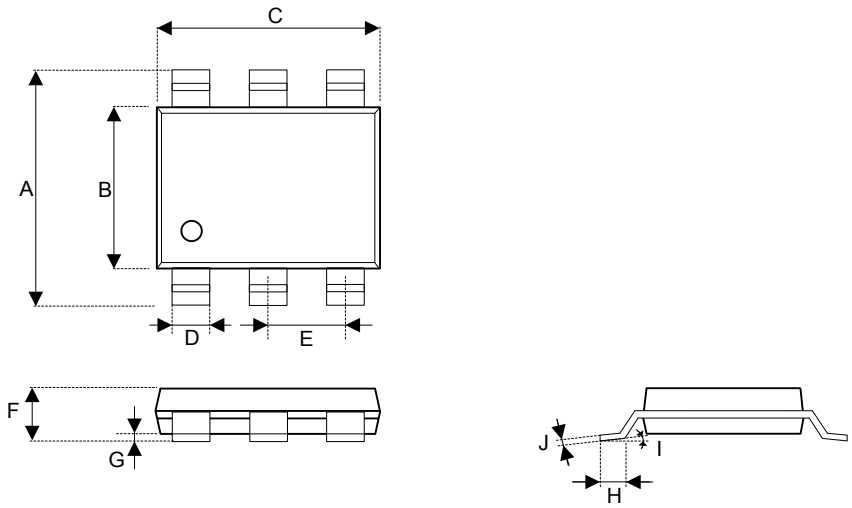


Figure 11.1 TSOT23-6 Packaging[9]

Table 11.1 TSOT23-6 Dimensions

Dimension	Min (mm)	Max (mm)
A	2.60	3.00
B	1.50	1.70
C	2.80	3.00
D	0.30	0.50
E	0.95 Basic	
F	0.84	0.90
G	0.00	0.10
H	0.30	0.50
I	0°	8°
J	0.03	0.20

[9] Drawing not on Scale

11.1.2 TSOT23-6 Tape

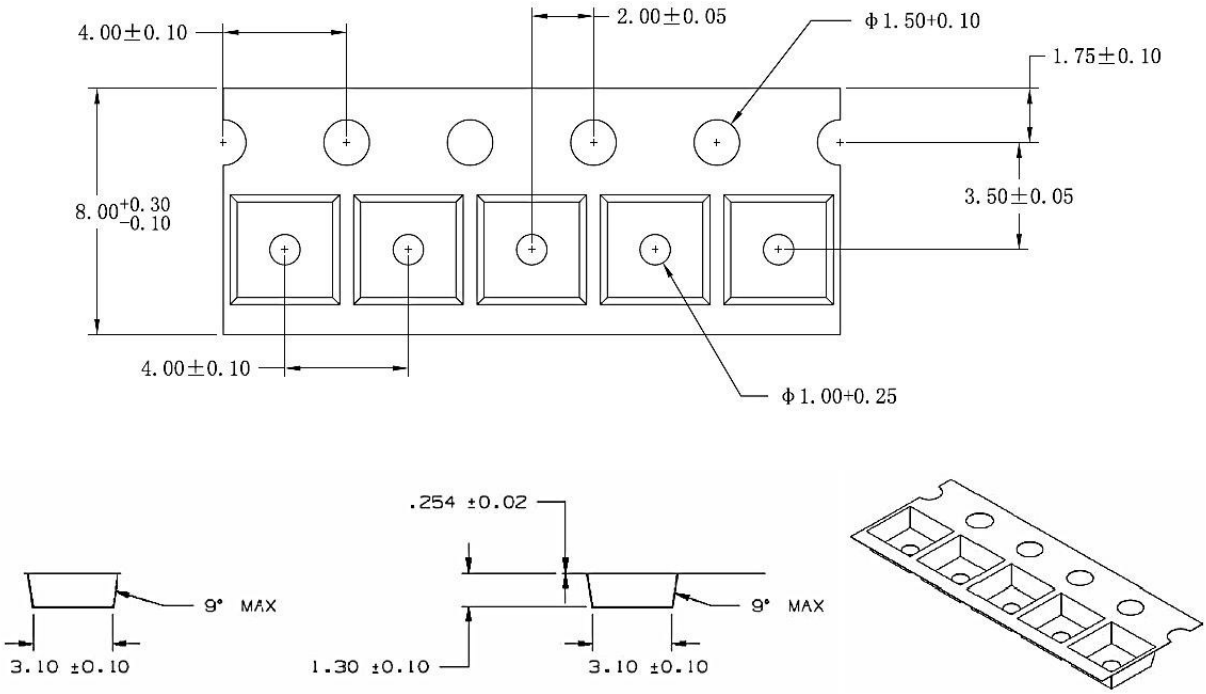
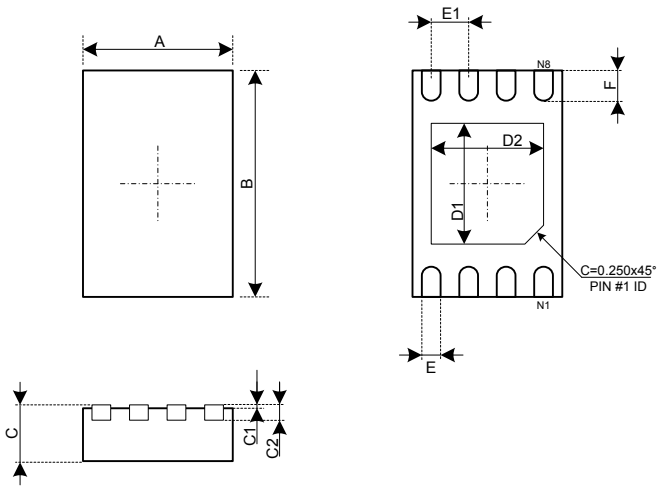


Figure 11.2 IQS128Tape Specification

11.1.3 DFN8 (2x3)



NOTE: Both Package length and width
do not include mold flash and burr

Figure 11.3 DFN8 (2x3) Packaging[10]

Table 11.2 DFN8(2x3) Dimensions

Dimension	Min (mm)	Max (mm)
A	2.0±0.1	
B	3.0±0.1	
C	0.70	0.80
C1	0~0.050	
C2	0.203TYP	
D1	1.60TYP	
D2	1.50TYP	
E	0.250TYP	
E1	0.500TYP	
F	0.400TYP	

11.1.4 DFN8 Tape

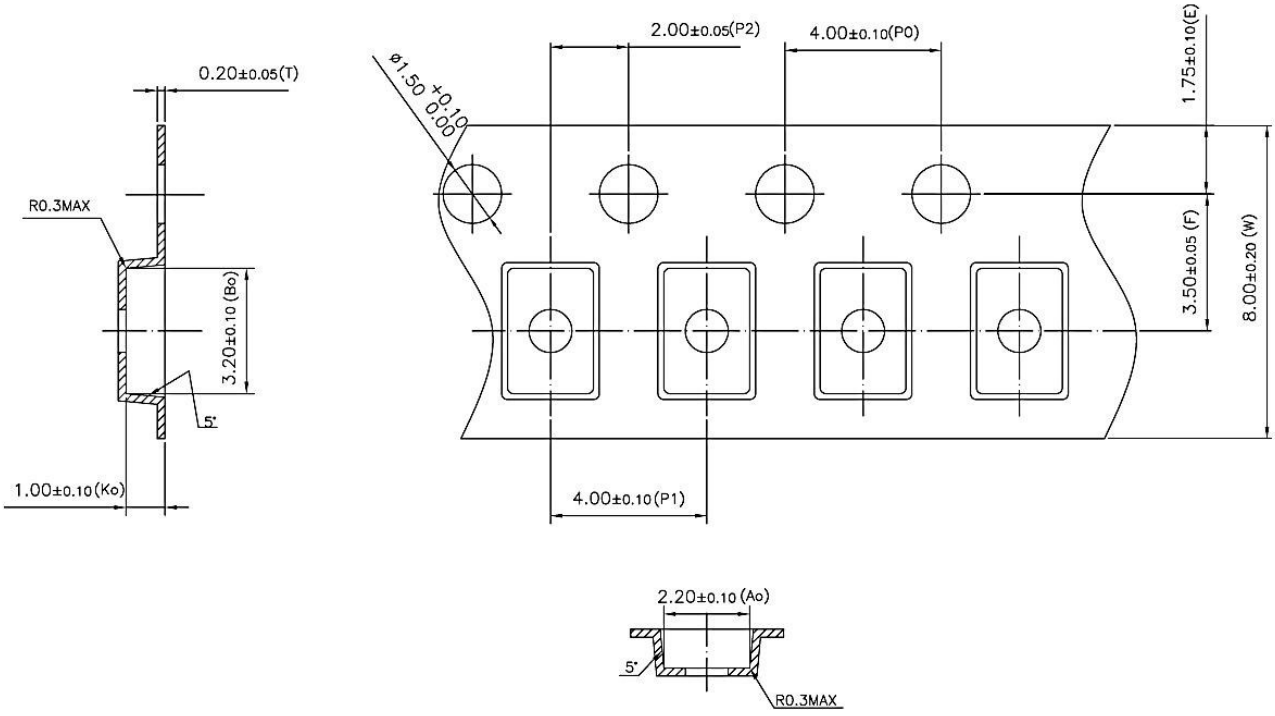


Figure 11.4 DFNTape Specification

[10] Drawing not on Scale

11.1.5 Moister Sensitivity Level (MSL)

Moisture Sensitivity Level relates to the packaging and handling precautions for some semiconductors. The MSL is an electronic standard for the time period in which a moisture sensitive device can be exposed to ambient room conditions (approximately 30°C/60%RH).

Increasingly, semiconductors have been manufactured in smaller sizes. Components such as thin fine-pitch devices and ball grid arrays could be damaged during SMT reflow when moisture trapped inside the component expands.

The expansion of trapped moisture can result in internal separation (delamination) of the plastic from the die or lead-frame, wire bond damage, die damage, and internal cracks. Most of this damage is not visible on the component surface. In extreme cases, cracks will extend to the component surface. In the most severe cases, the component will bulge and pop.

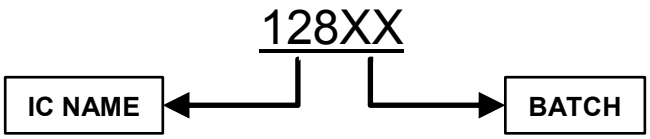
Table 11.3 IQS128 Packaging MSL Information

Package	Level (duration)
TSOT23-6	MSL1 (unlimited at ≤30 °C/85% RH)
DFN8 (2x3)	MSL 3 – 168 hours

11.2 Device Packaging Convention

11.2.1 IQS128

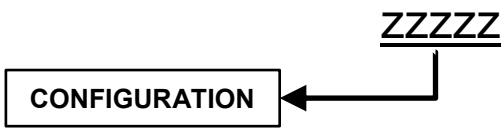
11.2.1.1 Top



11.2.1.2 Bottom

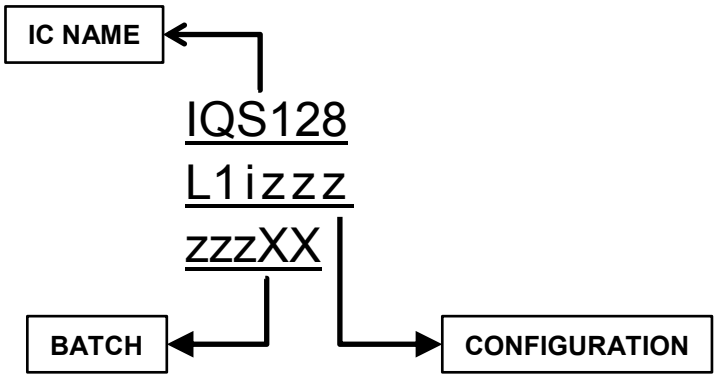
Some batches IQS128 will not have any bottom markings. These devices are configured after marking, and may have variations in configuration – please refer to the reel label.

Other batches will display the configuration set on the chip on the bottom marking.



11.2.2 IQS128L

11.2.2.1 Top



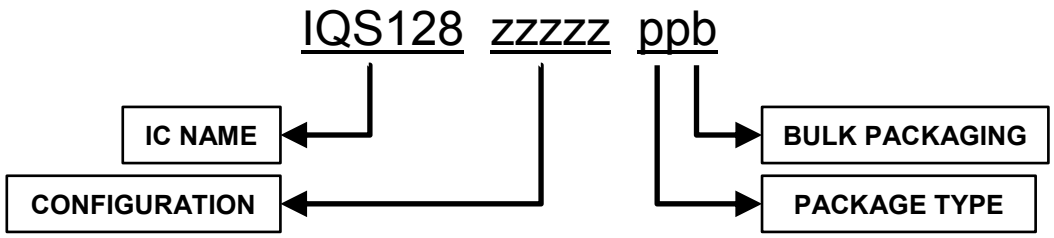
11.3 Ordering Information

Only full reels can be ordered and orders will be subject to a MOQ (Minimum Order Quantity) of a full reel. Contact the official distributor for sample quantities. A list of the distributors can be found under the "Distributors" section of www.azoteq.com.

For large orders, Azoteq can provide pre-configured devices.

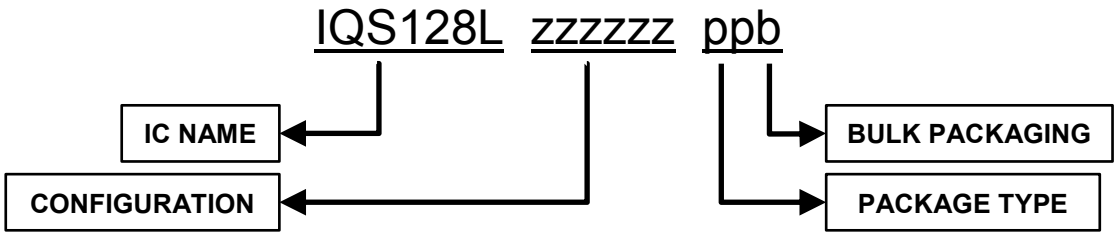
The Part-number can be generated by using USBProg.exe or the Interactive Part Number generator on the website.

11.3.1 IQS128



IC NAME	IQS128	=	IQS128
CONFIGURATION	zzzzz	=	IC Configuration (hexadecimal)
PACKAGE TYPE	TS	=	TSOT23-6
BULK PACKAGING	R	=	Reel (3000pcs/reel)
			MOQ = 1 reel.
			Mass production orders shipped as full reels.

11.3.2 IQS128L



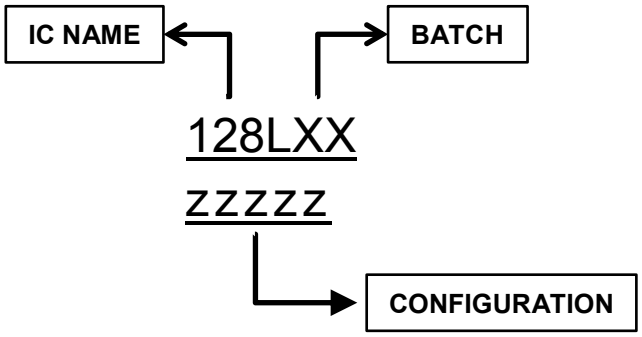
IC NAME	IQS128L	=	IQS128L
CONFIGURATION	zzzzzz	=	IC Configuration (hexadecimal)
PACKAGE TYPE	DN	=	DFN8 (2x3)
BULK PACKAGING	R	=	Reel (3000pcs/reel)
			MOQ = 1 reel.
			Mass production orders shipped as full reels.

12 Errata

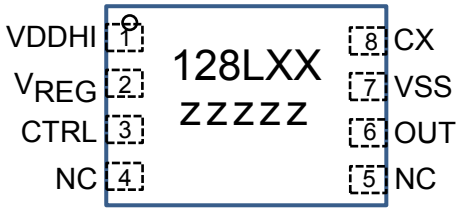
- Section 11.2.2:

  It must be noted that the previous packaging for the IQS128L is still being phased out and for this reason IC's can still be found with the below packaging convention and device markings.

  Packaging Convention:



  Device Markings:



13 Datasheet Revision History

Version 1.10 - Preliminary Release

Version 2.0 - Added IQS128L and its functional differences
- Added ATI BASE description
- Added ND feature description for IQS128

Version 2.1 - Updated aesthetics

Version 2.2 - Changed QFN to DFN
- Changed Power Mode names

Version 2.3 - Updated maximum operating voltage to 5.5 throughout document
- Updated Absolute Maximum Specification: Supply voltage to 6.5V. (Only intended for OTP programming!)

Version 2.4 - Updated POR and BOR table
- Updated packaging and part-number information
- Changed Current Sample references to Counts (CS)
- Changed Antenna references to Electrode
- Changed Auto-ATI references to ATI
- Changed Device Markings
- Added Tape/Reel Specification
- Moved Section On Packaging Information to Section 12
- Made Revision History a section on its own
- Added Tape Specification
- Added Errata to accommodate previous packaging

Version 2.5 - Improve images on front page
- Add bottom marking description
- Update contact information

14 Contact Information

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Postal Address	6507 Jester Blvd Bldg 5, suite 510G Austin TX 78750 USA	Rm1725, Glittery City Shennan Rd Futian District Shenzhen, 518033 China	PO Box 3534 Paarl 7620 South Africa
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IQS128-00000TSR IQS128-00100TSR IQS1280001BTSR