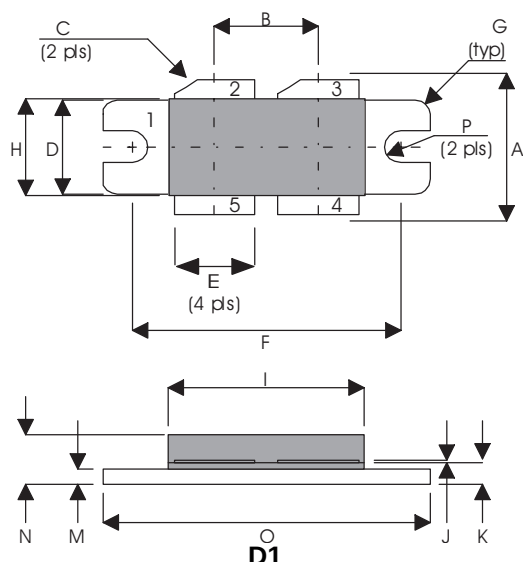


MECHANICAL DATA


PIN 1	SOURCE (COMMON)	PIN 2	DRAIN 1
PIN 3	DRAIN 2	PIN 4	GATE 2
PIN 5	GATE 1		

DIM	Millimetres	Tol.	Inches	Tol.
A	15.24	0.50	0.600	0.020
B	10.80	0.13	0.425	0.005
C	45°	5°	45°	5°
D	9.78	0.13	0.385	0.005
E	8.38	0.13	0.330	0.005
F	27.94	0.13	1.100	0.005
G	1.52R	0.13	0.060R	0.005
H	10.16	0.15	0.400	0.006
I	21.84	0.23	0.860	0.009
J	0.10	0.02	0.004	0.001
K	1.96	0.13	0.077	0.005
M	1.02	0.13	0.040	0.005
N	4.45	0.38	0.175	0.015
O	34.04	0.13	1.340	0.005
P	1.63R	0.13	0.064R	0.005

GOLD METALLISED **MULTI-PURPOSE SILICON** **DMOS RF FET** **300W – 50V – 175MHz** **PUSH-PULL**

FEATURES

- SUITABLE FOR BROAD BAND APPLICATIONS
- SIMPLE BIAS CIRCUITS
- ULTRA-LOW THERMAL RESISTANCE
- BeO FREE
- LOW Crss
- HIGH GAIN – 20 dB MINIMUM

APPLICATIONS

- VHF/UHF COMMUNICATIONS
from 1 MHz to 175 MHz

P_D	Power Dissipation	875W (438W -A Version)
BV_{DSS}	Drain – Source Breakdown Voltage *	125V
BV_{GSS}	Gate – Source Breakdown Voltage*	±20V
$I_{D(sat)}$	Drain Current*	18A
T_{stg}	Storage Temperature	–65 to 150°C
T_j	Maximum Operating Junction Temperature	200°C

* Per Side

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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PER SIDE					
BV_{DSS} Drain-Source Breakdown Voltage	$V_{GS} = 0$ $I_D = 100\text{mA}$	125			V
I_{DSS} Zero Gate Voltage Drain Current	$V_{DS} = 125\text{V}$ $V_{GS} = 0$			6	mA
I_{GSS} Gate Leakage Current	$V_{GS} = 20\text{V}$ $V_{DS} = 0$			6	μA
$V_{GS(th)}$ Gate Threshold Voltage*	$I_D = 10\text{mA}$ $V_{DS} = V_{GS}$	1		7	V
g_{fs} Forward Transconductance*	$V_{DS} = 10\text{V}$ $I_D = 3\text{A}$	4.8			mhos
$V_{GS(th)match}$ Gate Threshold Voltage Matching Between Sides	$I_D = 10\text{mA}$ $V_{DS} = V_{GS}$			0.1	V
TOTAL DEVICE					
G_{PS} Common Source Power Gain	$P_O = 300\text{W}$	20			dB
η Drain Efficiency	$V_{DS} = 50\text{V}$ $I_{DQ} = 1.2\text{A}$	60			%
VSWR Load Mismatch Tolerance	$f = 175\text{MHz}$	20:1			—
PER SIDE					
C_{iss} Input Capacitance	$V_{DS} = 50\text{V}$ $V_{GS} = -5\text{V}$ $f = 1\text{MHz}$			360	pF
C_{oss} Output Capacitance	$V_{DS} = 50\text{V}$ $V_{GS} = 0$ $f = 1\text{MHz}$			150	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 50\text{V}$ $V_{GS} = 0$ $f = 1\text{MHz}$			9	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle $\leq 2\%$

THERMAL DATA

$R_{THj-case}$	Thermal Resistance Junction – Case	Max. $0.2^{\circ}\text{C} / \text{W}$ $0.4^{\circ}\text{C} / \text{W}$ -A Version
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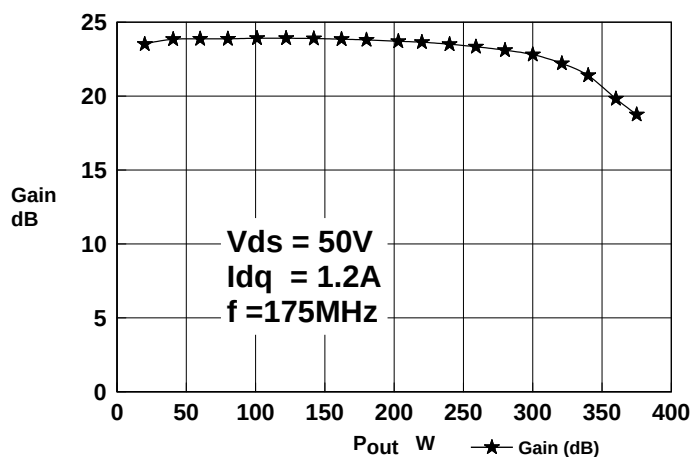


Figure 1 – Gain vs. Power Output.

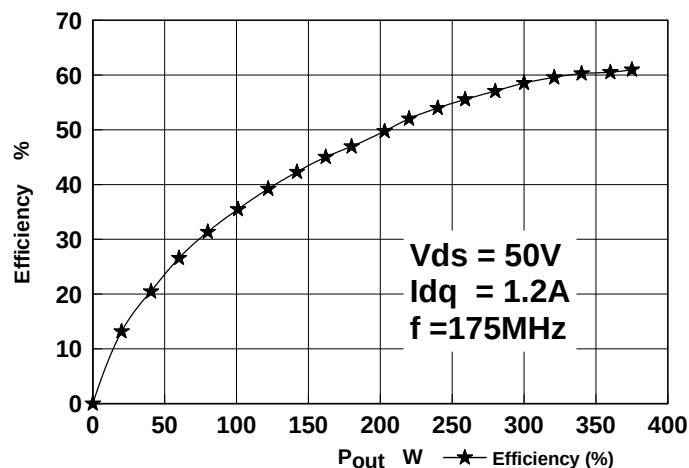


Figure 2 – Efficiency vs. Power Output.

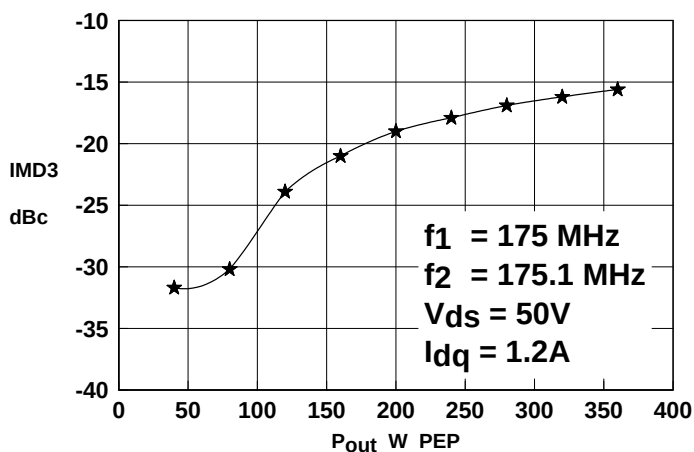


Figure 3 – IMD vs. Power Output

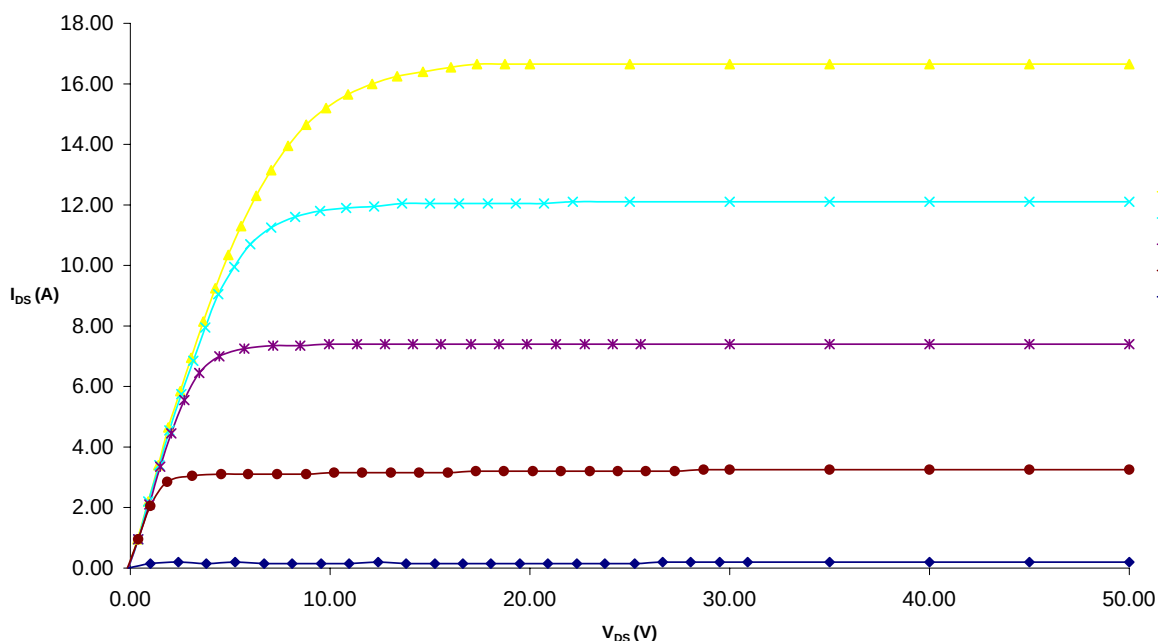


Figure 4 – Typical IV Characteristics.

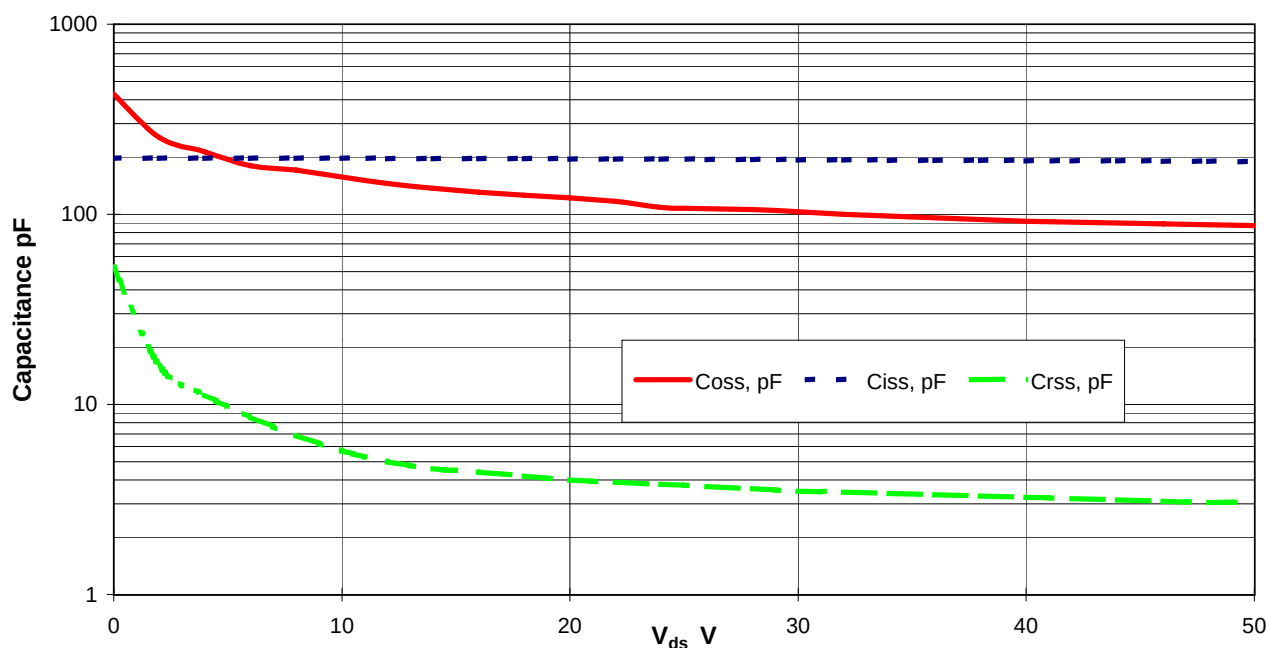
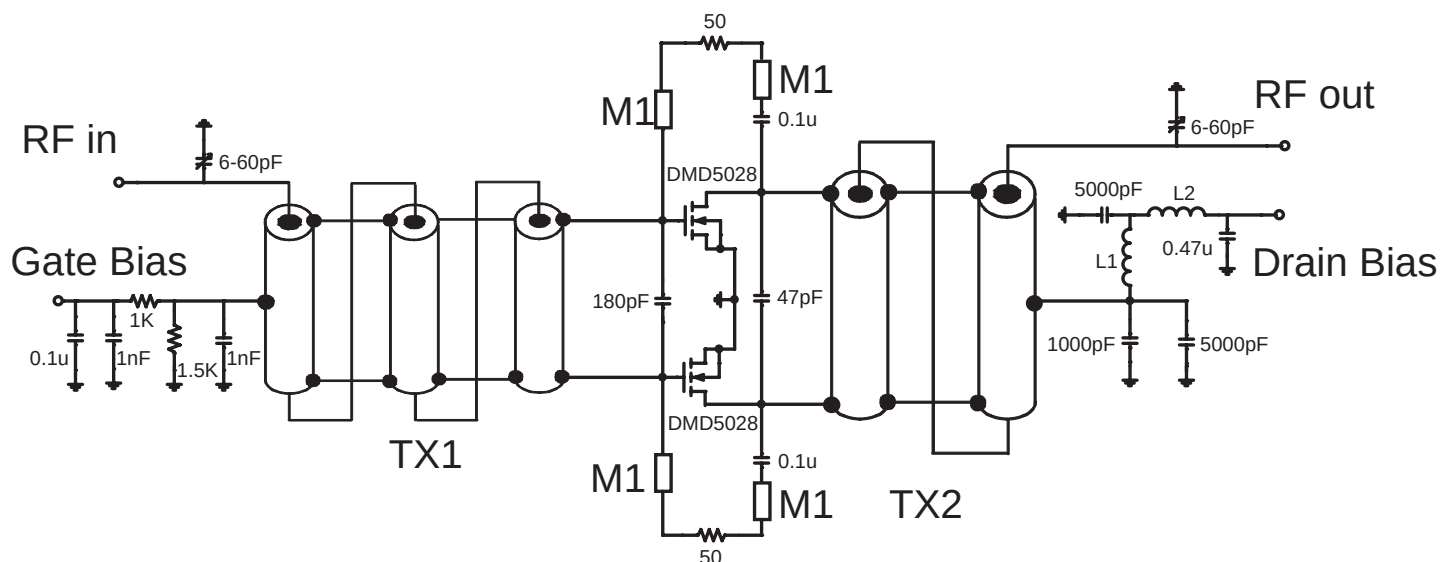


Figure 5 – Typical CV Characteristics.

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DMD5028 175MHz TEST FIXTURE

- TX1** 9:1 transformer. 3 turns of 062-25 semi-rigid coax around 75-26 powdered iron core
- TX2** 4:1 transformer. 2 turns of 090-25 semi-rigid coax around 100-8 powdered iron core
- L1** 10 turns 16awg enamelled wire, 5mm internal diameter
- L2** 0.5 turns 16 awg enamelled wire on A1 x 1 2-hole core
- M1** microstrip line, 20mm long, 1mm wide on 0.062in thick G10 substrate

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